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An Angledetector based on magnetic sensing

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ABSTRACT

An angledetector with a digital output is described. The component is ment as an alternative to the traditional slide potentiometer used as volume control in many hearing aid applications. The component is based on the use of magnetic sensitive MOSFET's (MAGFET's) detecting the position of a tiny bar magnet placed above a silicon chip. Because of the galvanic separation between the anglesetting bar magnet and the electrical circuit, this component is insensitive to the rather hostile environment hearing aids are exposed to. The lifetime of the component is thereby increased significantly. The electrical circuit contains a switched current A/D - D/A conversion system for offset compensating the MAGFET's and for converting the MAGFET signal currents into a digital output proportional to the input angle. It is implemented using a commercially available $1.5\ \mu\text{m}$ CMOS process.

INTRODUCTION

The volume control in hearing aid systems is often realized with a traditional slide potentiometer. Due to the hostile and humid environment in which it has to function and the galvanic contact between the metal pointer and the carbon slide, the lifetime of the component is rather limited. One way of avoiding the galvanic contact is letting magnetic sensitive transistors detect the position of a movable bar magnet as shown by Figure 1. An iron disk is placed beneath the chip to focus the magnetic field applied to the MAGFET's. The bar mag-

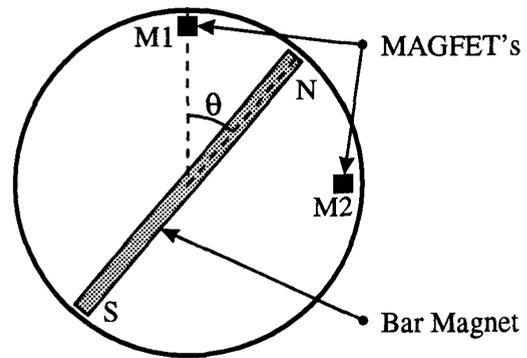


Figure 1. The Angledetecting system

net can make a 2π turn (there can be a physical stop to make only one turn possible) and two MAGFET's are used. One is placed at the angle $\theta = 0$ and one is placed at the angle $\theta = \pi/2$.

On the assumption that the differential output current of a MAGFET is proportional to the magnetic flux through it [3], a possible *Angle to Current*-transfer function is shown in Figure 2. $I_{D,M1}$ and $I_{D,M2}$ are the differential output currents of the two MAGFET's M1 and M2. The exact transfer function is a rather complex function of the dimensions of the bar magnet, the placement of the MAGFET's and the chosen materials.

From Figure 2 it is clear that any angle position unambiguously can be detected. This paper describes a

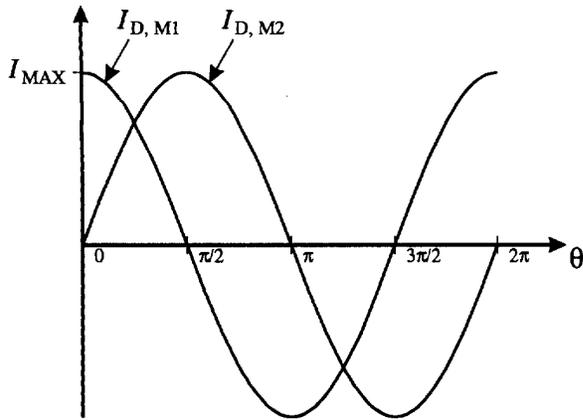


Figure 2. The MAGFET signal currents

solution where the angle position is to be represented by a 7 bit digital number proportional to the input angle. The two most significant bits (MSB) can be determined by simply reading the signs of the two MAGFET currents. This will divide the input angle into four equally sized intervals which can be represented by the two most significant bits. The third MSB can be provided by comparing the two currents numerically, $|I_{D,M1}| > |I_{D,M2}|$. The four least significant bits can be generated by A/D converting the numerical smallest current with the numerical largest current as a reference. This is in effect a division expressed by Eq. (1).

$$4 \text{ LSB} = f_{\text{dec}}(D_3 \dots D_0) = \frac{\min\{|I_{D,M1}|, |I_{D,M2}|\}}{\max\{|I_{D,M1}|, |I_{D,M2}|\}} \quad (1)$$

The f_{dec} function indicates that a decoding of the result is taking place. Simulations on the transfer function of the system indicate that an approximate linear *Angle to digital output*-transfer function indeed is achievable with a appropriate choice of dimensions and placement of the bar magnet and the MAGFET's and magnetic material. The simulations were based on the 'finite element' analysis method using the ANSYS program [1]. The dimensions of the entire chip is 2 mm \times 2 mm and the dimensions of the bar magnet is 0.5 mm \times 0.65 mm \times 2 mm (HWL). The MAGFET will be exposed to a magnetic field in the range of ± 0.25 T.

THE MAGFET TRANSISTOR

A MAGFET is a MOSFET transistor with multiple drain terminals (typically 2 or 3 drains) [2] [3]. Due to the implementation (See Figure 3) of the MAGFET the differential drain current is dependent on the magnetic field applied to it.

The dimensions, the biasing and the topology of the MAGFET will influent important values as sensitivity to

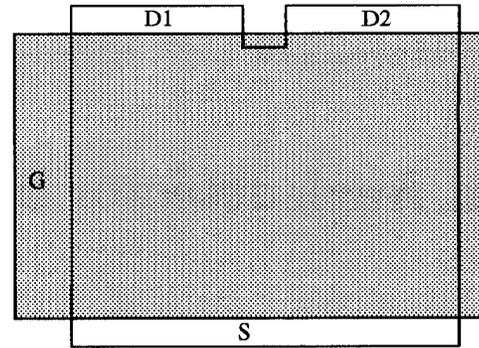


Figure 3. MAGFET Layout

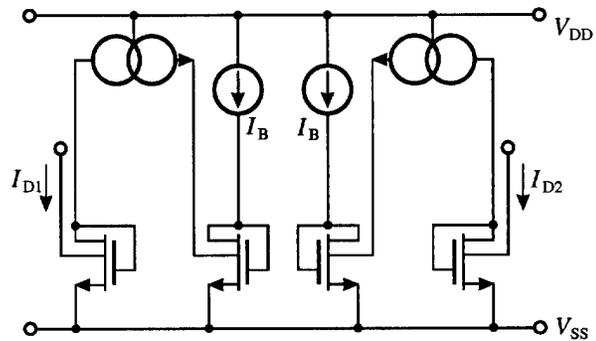


Figure 4. Cascade coupled MAGFET

magnetic field, linearity, noise, offset errors and the use of power and area. Measurements and the calculations can be seen in [4]. In this specific project the MAGFET has been implemented using four two-drain MAGFET's in cascade as shown in Figure 4. The dimensions of each MAGFET is $W/L = 62 \mu\text{m}/62 \mu\text{m}$ and there has been used a common centroid structure for the layout for lowering offset errors. The resulting MAGFET was found to have an approximate transfer function given by Eq. (2).

$$I_{D1} - I_{D2} = 0.32 \text{ T}^{-1} I_B B_{z, \text{MAG}}(\theta) + I_{\text{OFF}} \quad (2)$$

where $B_{z, \text{MAG}}(\theta)$ is the magnetic flux in the vertical direction at the given MAGFET.

The bias current was set to $I_B = 15 \mu\text{A}$ giving us a maximum differential signal current of $\pm 1.2 \mu\text{A}$. The cascade coupled MAGFET uses $120 \mu\text{A}$ and the offset current I_{OFF} is measured to be as high as 50 % of the maximum output current. This is mainly due to variations on the threshold voltage V_T . This large offset current cannot be accepted. An offset compensation is necessary to bring it to an acceptable level. For this purpose an 8 bit A/D - D/A system will be used.

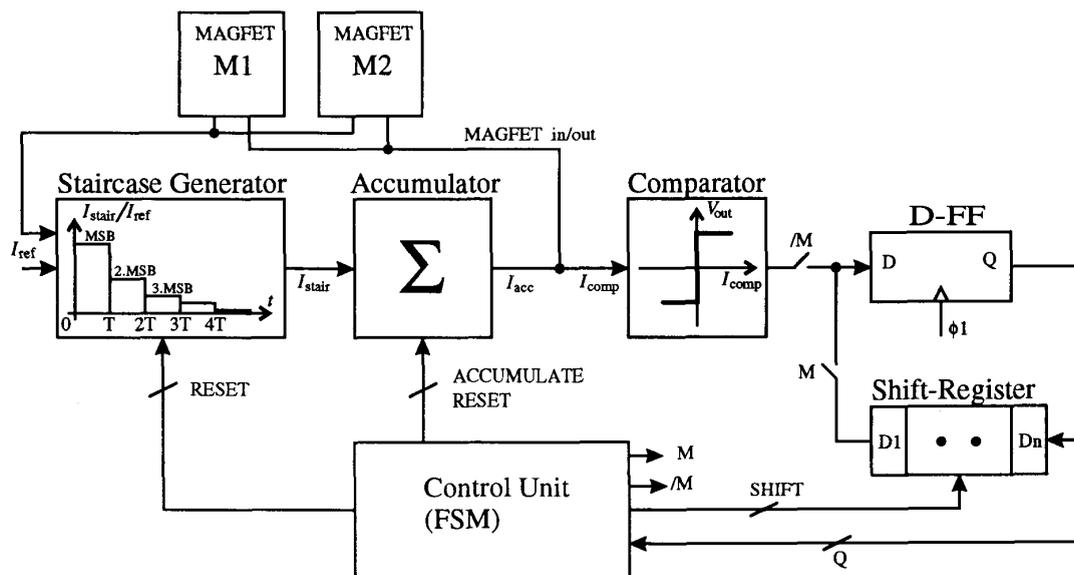


Figure 5. The AD/DA system

THE A/D - D/A SYSTEM

The A/D - D/A system must be able to measure the offset error by an A/D conversion and make a permanent digital storage of the offset error. The stored offset error is then to be D/A converted and subtracted from the MAGFET current. The measuring and storing of the offset errors has to be done without any magnetic field applied to the MAGFET, i.e. before the bar magnet is placed on the top of the chip. The D/A conversion and the subtraction of the stored error from the MAGFET current must be carried out before any processing on the MAGFET currents can take place. It was decided to use the *successive approximation method* for A/D conversion because this conversion is based on a D/A converter (DAC). By using the same DAC in both the A/D and the D/A conversion unwanted nonlinearities in the D/A transfer function will cancel out. Also it is an efficient solution in terms of minimizing area.

For the purpose a serial DAC, which generates the MSB first and the LSB last, has been developed. The advantage of this solution, compared to a parallel DAC, is less use of area and no use of a *successive approximation register*. The D/A converter has been realized with the use of *switched current* technique and is described in detail in [4]. A block diagram of the entire system is shown in Figure 5.

The system is controlled by a finite state machine realized with a PLA. It works in two different modes. In **Mode 1** the two offset currents is measured (A/D converted) and stored digitally. In **Mode 2** the stored er-

ror signals are D/A converted and subtracted from the MAGFET currents and the position of the bar magnet is determined from the two offset compensated MAGFET currents. The sequences are shown schematically below.

Mode 1 : Storage of offset errors (No magnetic field applied)

1. 8 bit A/D conversion of $I_{M1,OFF}$
2. Storage of $I_{M1,OFF}$
3. 8 bit A/D conversion of $I_{M2,OFF}$
4. Storage of $I_{M2,OFF}$

Mode 2 : Position detection (Magnetic field applied)

1. 8 bit D/A conversion of $I_{M1,OFF}$
 $I_{M1,SIGNAL} = I_{M1} - I_{M1,OFF}$
2. 8 bit D/A conversion of $I_{M2,OFF}$
 $I_{M2,SIGNAL} = I_{M2} - I_{M2,OFF}$
3. $I_{M1,SIGNAL} > 0 ? ; I_{M2,SIGNAL} > 0 ?$
 $|I_{M1,SIGNAL}| > |I_{M2,SIGNAL}| ? \Rightarrow 3 \text{ MSB}$
4. 4 bit A/D conversion : $\frac{\min\{|I_{D,M1}|, |I_{D,M2}|\}}{\max\{|I_{D,M1}|, |I_{D,M2}|\}} \Rightarrow 4 \text{ LSB}$

A/D conversion : The A/D conversion of **Mode 1** utilizes all of the building blocks of Figure 5. The staircase generator is generating a sequence of MSB followed by 2.MSB etc. ending with LSB. When the output is MSB the output of the accumulator (MSB as well) is subtracted from the MAGFET current that is to be measured and the sign of the resulting current is shown on the output of the comparator. This sign signal is both shifted into the shift register and passed to the control

unit. Depending on the sign the control unit decides whether the accumulator should accumulate the output from the staircase generator (sign is positive) or not (sign is negative). The same scheme now is repeated for 2.MSB and so on, and the staircase outputs are only accumulated when the output of the comparator is positive. The digital number representing the offset error is now stored in the shift register and is ready for D/A conversion of Mode 2.

D/A conversion : In this mode the operation of the staircase generator and the accumulator is the same but the comparator is not used. Instead the "sign signal" now is shifted out from the shift register to control the accumulation. The resulting output of the accumulator is now subtracted from the uncompensated MAGFET current and stored in a current copier.

The compensating subtraction and inversion of current signals are carried out with the use of the basic building blocks of the switched current circuitry, the *current copiers* [5]. The current copiers are implemented with the use of an inverting transconductance amplifier, a capacitor for storage and three switches. The switches are controlled by the non-overlapping clock phases $\phi 1$ and $\phi 2$. When the clock phase $\phi 1$ is high (logical 1) the current copier will read the input current, I_{in} , and the corresponding voltage ($V_{gs} = I_{in}/g_m$) will be stored on the input capacitance of the transconductance amplifier. When $\phi 2$ is high the output current will become $I_{out} = -g_m V_{gs} = -I_{in}$ (See Figure 6).

Because of the large current consumption of the MAGFET, a current copier is used to sample and hold the MAGFET current. The MAGFET now only has to be turned on for one clock cycle for measuring the MAGFET current. The operating clock frequency for the switched current system is 25 kHz. An angledetection has to be done at every 100 ms meaning that the *turn on* dutycycle for the MAGFET is less than 0.1%. The circuit has been optimized to work with a supply voltage down to 2.2 V and with a static current consumption of 40 μ A. The total process of Mode 2 is carried out in 32 clock cycles making the *turn on* dutycycle for the entire circuit (including all digital operations) less than 2%.

EXPERIMENTAL RESULTS

The circuit has been laid out in an industry standard 1.5 μ m CMOS process. The chip size is 2 mm \times 2 mm and the circuitry uses approximately 60 % of this area. The reason for the chip size to be this big is that it should fit to the bar magnet, which for practical reasons could not be made smaller.

All the described operations of the A/D - D/A system and of the MAGFET's have been tested. Measurements show that the system could function with supply voltages down to 2.3 V and with a static current consumption of 38.5 μ A. The system was found to operate correctly

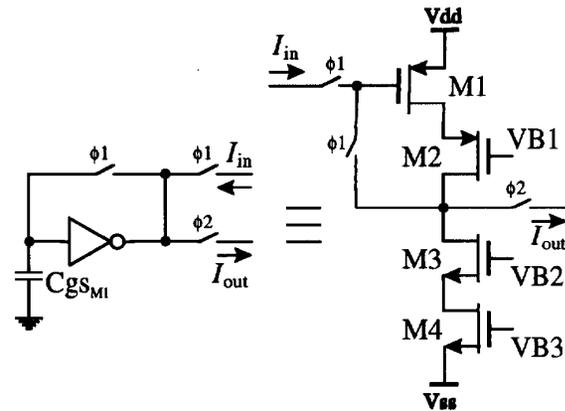


Figure 6. The current copier

within the clock frequency range of 5 Hz to 25 kHz.

CONCLUSION

An angledetector with 7 bit digitally output has been described. It is ment as an alternative to the traditional slide potentiometer used as volume control in many hearing aids systems. Because of the absence of galvanic contact between the anglesetting device and the electrical circuitry the component is expected to increase lifetime of the component significantly. The analog part of the system has got a static current consumption of approximately 40 μ A and because of the small turn on dutycycle the overall current consumption is less than 1.5 μ A. It works with a supply voltage down to 2.2 V.

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