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LC QUADRATURE GENERATION IN INTEGRATED CIRCUITS

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ABSTRACT

Today quadrature signals for IQ demodulation are provided through RC polyphase networks, quadrature oscillators or double frequency VCOs. This paper presents a new method for generating quadrature signals in integrated circuits using only inductors and capacitors. This LC quadrature generation method enables significantly reduced noise and power consumption.

1. INTRODUCTION

A number of different topologies exist that can be used for complex modulation and demodulation in radio frequency communication systems. Some of these topologies are shown in figure 1 and figure 2. The topologies shown in figure 1 use either the RF or the LO signal in quadrature [3] and the double quadrature topology [4] shown in figure 2 uses both the RF and the LO in quadrature either to loosen the requirements of the quadrature generating circuits or to improve the accuracy of the down converted signals.

Common to these topologies is the need to have one or more of the high frequency signals in quadrature i.e. one version *In-Phase* and one version in *Quadrature* i.e. shifted 90 degrees and if the circuit uses differential signalling which is typically the case this translates to the need for four identical signals each shifted by 90 degrees.

Such four quadrature signals can be generated in a number of different manners. The local oscillator signal (LO) can be generated in quadrature with a quadrature VCO or by dividing a double frequency VCO. Alternatively it can be generated with an RC polyphase filter. For the RF signal the only method that is used at present to generate quadrature signals is the RC polyphase filter.

All of these methods have their drawbacks. The Quadrature VCO and the double frequency VCO with dividers are fairly power hungry solutions and the resistors in RC polyphase filters introduce significant thermal noise and loss which results in a need for more high frequency amplification and thus added power consumption. Due to the noise-power implications of the RC polyphase filter the topology in figure 1 - b is by far the most common today [3].

In order to reduce the power consumption needed for the topology in figure 1-b and in order to make the other two topologies more feasible what is needed is a quadrature generating circuit that introduces negligible noise and power consumption of its own. Such a circuit is presented in this paper. It eliminates the thermal noise and loss of the RC polyphase filter by using only capacitors
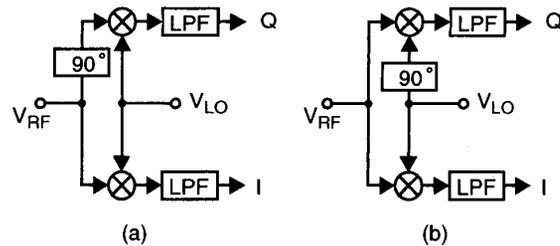

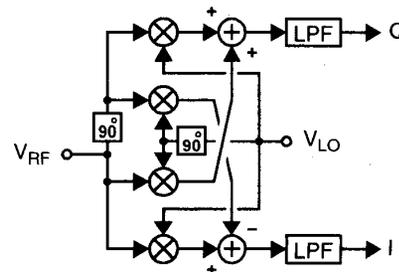**Figure 1.** Quadrature mixing with quadrature generation in (a) RF path, (b) LO path.

Figure 2. Double quadrature downconversion.

and inductors and it may be considered very low power because it can be integrated as part of a high frequency buffer that may be needed in any case.

2. ALLPASS FILTERS

When designing classical filter structures like Butterworth, Chebyshev or elliptical filters, synthesis is made without consideration of the phase response given by the network. In some cases a nonlinear phase response is of minor importance but other cases such as in digital communication systems that use phase modulation the signal may be seriously distorted by a nonlinear phase response. In order to get a linear phase or equivalently a constant group delay it is often necessary to use phase linearizers. Typically such circuits should not change the filters magnitude response but only affect the phase response. This means that they must have a unity gain independent of frequency i.e. that $|H(j\omega)| = 1$. Because phase linearizers pass signals at all frequencies they are usually called allpass filters. Because the sole purpose of allpass filters is to change the phase of a signal they are a natural place to start our search for a suitable quadrature generating circuit.
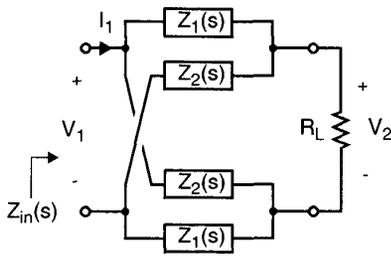
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Figure 3. Symmetrical resistance reciprocal network

Allpass filters can be realized in a number of different manners. These include single ended LC networks using ideal transformers or center tapped inductors, active circuits exploiting negative feedback and symmetrical cross coupled resistance reciprocal networks. The latter requires a well balanced differential input signal, good matching between circuit elements and more reactive components than what would be needed for some of the other methods. In a discrete realization all of these three requirements may be problematic but on an integrated circuit well balanced differential signals and good component matching is readily available and the differential structure does not double the cost of the IC. The fact that the cross coupled resistance reciprocal network (figure 3) exploits the nature of the differential signal makes the circuit especially attractive for an integrated circuit where absolute component tolerances are usually fairly high. For these reasons we will take a closer look at this structures usability as a quadrature generating network.

It can be shown [2] that for the circuit in figure 3 to behave as an allpass filter it must be resistance reciprocal i.e. satisfy (EQ 1) and $Z_1(s)$ and $Z_2(s)$ must both be LC reactance networks.

$$\frac{Z_1(s)}{R_L} = \frac{R_L}{Z_2(s)} \qquad \text{(EQ 1)}$$

If this is the case the circuit will have unity gain and an input impedance $Z_{in}(s)$ that is equal to the load resistance R_L. Therefore the source impedance R_S must be equal to the load impedance to ensure maximum power transfer (EQ 2).

$$R_S = Z_{in}(s) = \frac{V_1}{I_1} = R_L \qquad \text{(EQ 2)}$$

If $Z_1(s)$ and $Z_2(s)$ are made out of one reactive element each the network is called a first order passive allpass filter. If instead they are each made out of a series or a parallel combination of an inductor and a capacitor the network is called a second order allpass filter. Because these allpass networks have unity gain and an input impedance that is equal to the load impedance they can be cascaded without loosing their allpass nature. Therefore allpass filters with an arbitrary order can be made by cascading a number of first and second order allpass filter stages.
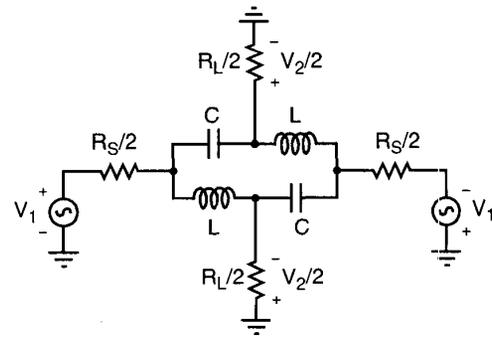

Figure 4. Four phase network made from a first order LC allpass filter.

3. QUADRATURE PHASES

The whole point of considering phase shifting networks is the target of generating quadrature phases i.e. four signals with equal amplitude and phases separated by 90 degrees. In order to minimize complexity we will start by considering first order allpass structures i.e. $Z_1(s) = sL$ and $Z_2(s) = 1/sC$ or vice versa (Figure 4).

For a cross coupled first order allpass network it can be shown [1] that if $\omega_0 L = 1/\omega_0 C$ i.e. at the resonance of an LC tank (EQ 3) the output will have a phase that is exactly the average of the two driving phases so if the driving signal is a perfect differential signal (180 degrees) the output is turned 90 degrees compared to the input.

$$\omega_0^2 = \frac{1}{LC} \qquad \text{(EQ 3)}$$

To get from the structure shown in figure 3 to the circuit shown in Figure 4 a few extra considerations needs to be made. Because the driving signal is expected to be a perfect differential signal the source including the source resistance can be split in two. Likewise the load resistance can be split in two for symmetry reasons. It is now more intuitive how four different phases with equal amplitude are generated.

In order to get unity gain, maximum power transfer and quadrature phases (EQ 1), (EQ 2) and (EQ 3) must be fulfilled. Further because we are considering a first order allpass structure $Z_1(s) = sL$ and $Z_2(s) = 1/sC$ or vice versa. This enables us to formulate a set of simple design equations that guarantee quadrature signals.

$$C = \frac{1}{2\pi f_0 R_L} \qquad \text{(EQ 4)}$$

$$L = \frac{R_L}{2\pi f_0} \qquad \text{(EQ 5)}$$

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4. NORTON TRANSFORMATION

We are not yet completely satisfied with the quadrature generating network shown in figure 4. It does generate quadrature phases but if subsequent signal processing stages are to benefit from the quadrature signals they need to present an infinite impedance to the input of the allpass network because otherwise the quadrature relation is not maintained. Further matching the source impedance R_S to the load impedance R_L is not trivial when these impedances arise from different physical effects.

By transforming the source to its Norton equivalent (figure 5) it becomes apparent how these problems can be solved. If the signal is injected as a current from a source with an infinitely high impedance $R_S/2$ and $R_L/2$ can *both* be implemented as well matching resistors or as identical resistive loads from subsequent stages.

The differential current mode source can be implemented with a classical integrated circuit component - the basic differential pair with or without a tail current. figure 6 shows the resulting circuit which is much more satisfying and practical than the circuit shown in figure 4 because it uses standard integrated circuit components and ensures good matching between the loads.

5. COMMON GATE AMPLIFIER LOAD

Despite the fact that the circuit in figure 6 is satisfying as it is there are still a number of issues that may be resolved or improved. If each resistive load is replaced by a common gate amplifier (figure 7) with gm = $2/R_L$ several benefits can be achieved.

Most important is the common gate amplifiers buffering effect. With a common gate amplifier the quadrature generation becomes independent of the subsequent stages input impedance. Almost equally important is the common gate amplifiers impedance transforming capabilities. At the lower GHz range it may be necessary to reduce the load impedance seen by the allpass network to 50Ω or less to avoid getting too large inductances. Similarly in many cases it is beneficial to have a higher output impedance e.g. 100Ω or more in each branch which can easily be accommodated by a common gate amplifier. In short the common gate amplifier makes the impedance matching much easier to handle. An additional benefit of this structure is that the load impedance seen by the allpass structure $R_L/2$ = 1/gm can now be tuned by simply adjusting the bias current.

As a final note it can be pointed out that center tapped inductors (top of figure 7) can be used for biasing and thereby completely eliminate the need for lossy and noisy resistors in the quadrature generating network. The preceding stage can then use a shunt and/ or a series capacitor to achieve the appropriate tuning.

6. PARASITICS

Naturally passive components on an integrated circuit are not ideal components therefore we must take a look at how these non-idealities affect the quadrature generating network and possibly how they can be circumvented.
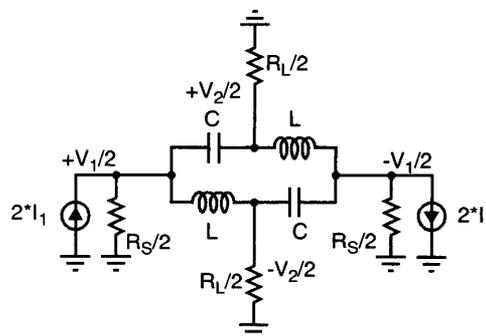

Figure 5. Current mode four phase network based on a first order LC allpass filter with matching resistive loads.
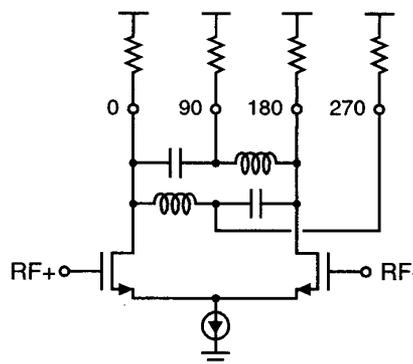

Figure 6. Quadrature generating RLC network with a basic differential pair and matching resistive loads.

Perhaps the most obvious non-ideality is the poor quality of on-chip inductors. At present inductors with Q-values of 6-7 can be achieved on EPI substrates and Q-values of 14-16 can be achieved on bulk substrates in the lower GHz range, but much better Q-values (up to 35) are expected with upcoming semiconductor technologies. In the meantime we need to address this issue. A low Q-value implies that the allpass circuit can not be considered lossless and therefore it does not behave as an ideal allpass filter. The inductor loss introduces small but significant phase and amplitude errors. It can be shown [1] that for the first order allpass structure the amplitude and phase errors can be completely out compensated by introducing an equal amount of loss in the capacitance branch e.g. as a series resistance R_C.

$$C = \frac{(Q^2 + 1)}{2\pi f_0 R_L (Q^2 - Q)} \qquad \text{(EQ 6)}$$

$$L = \frac{R_L(Q^2 - Q)}{2\pi f_0 (Q^2 + 1)} \qquad \text{(EQ 7)}$$

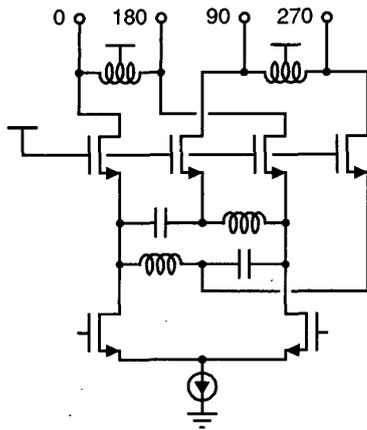$$R_C = \frac{2\pi f_0 L}{Q} \qquad \text{(EQ 8)}$$

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Figure 7. Quadrature generating circuit with common gate amplifier load.

Also the design equations need to be modified as specified in (EQ 6), (EQ 7) and (EQ 8).

Another well know parasitic element of on-chip inductors is the parasitic capacitance across the terminals of the inductor. All on-chip inductors with reasonable Q-value will have a small but noticeable amount of parasitic capacitance (e.g. 10% of C). This capacitance can be considered an expansion of the first order allpass network to a second order allpass network. Therefore the effect of the parasitic inductor capacitance can be compensated for by simply adding a small series inductance to the capacitor C. Strictly speaking this is fortunate because a capacitor can not be realized without some parasitic series inductance of its own. These allpass quadrature generating circuits provide a good quadrature output over a relatively narrow frequency band. Therefore it is important that the absolute values of L, C and R_L are well controlled. Fortunately on-chip inductors have very low process variation (<1%) and capacitors when implemented as lateral flux capacitors [5] also have low process variation (<3-5%). This means that the center frequency can be made with only 2-3% process variation. R_L will have higher process variation but this parameter may be calibrated either by using a switched resistor array or by adjusting the bias current when the common gate amplifier load is used. Therefore it should be possible to achieve sufficient accuracy for several narrow band and low cost applications like for instance GPS, ISM and DECT - especially when used with a double quadrature topology (figure 2).

7. EXAMPLE

A short example is given here to demonstrate how these design formulas can be used. We want to design a quadrature generating circuit like the one in figure 6 with a perfect quadrature output at 2.0 GHz. It is assumed that $R_L/2 = 100\Omega$ that the transistors are ideal and that the inductors have a Q-value of 8. Now (EQ 6) - (EQ 8) are used to find that C = 0.462pF, L = 13.7nH and R_C = 21.5Ω where the latter is the series resistance that is added to the capacitive branches in the first order allpass network.
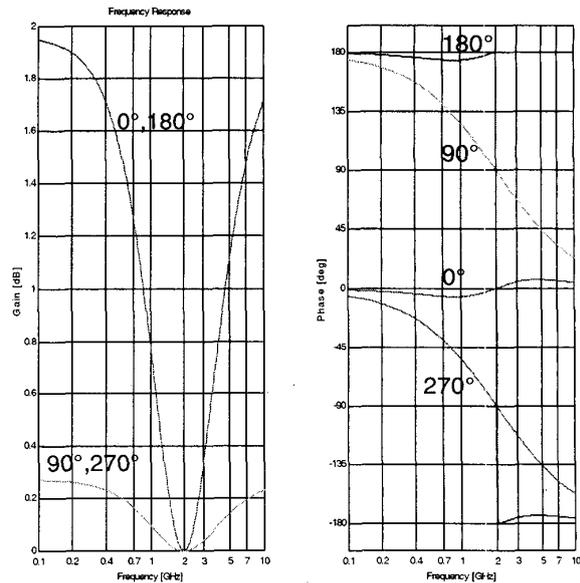

Figure 8. Simulated RLC quadrature generating circuit.

Figure 8 shows the amplitude and phase response of the resulting circuit. Notice that the circuit as expected has a relatively narrow band in which it provides 90 degrees phase shift and an excellent amplitude match over a very wide frequency range. This is opposite to the behavior of RC polyphase filters that only have a relatively narrow frequency band in which the amplitudes are well matched.

8. CONCLUSION

This paper presents a new quadrature generating circuit based on LC allpass networks. Because the circuit does not use resistors to achieve the phase shift it does not have the same thermal noise, loss and power consumption problems that RC polyphase filters do. Therefore this circuit enables considerable reduction in power consumption. Also it makes the double quadrature down-conversion scheme [4] much more attractive due to reduced noise in the RF path. The paper discusses the functionality of the circuit and finally a loss compensation method is presented that enables compensation of the on-chip inductor losses.

9. REFERENCES

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