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Analysis of the Effects of Time Delay in Clock Recovery Circuits Based on Phase-Locked Loops

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Introduction

In high-speed optical communication systems operating at 160 Gb/s and above, the clock extraction may be performed using an Optoelectronic Phase-Locked Loop (OPLL). In an OPLL, a considerable time delay is very likely to occur. Time delays in an OPLL may typically arise from the presence of a fiber amplifier (EDFA) and/or a pulse compression stage in the loop. It was shown in references [1-2] that intra-loop delays destabilise the loop. Based on a linearised PLL model, the trade-off between delay and bandwidth was determined [2]. However, for large values of the loop gain a non-linear Delayed Differential Equation (DDE), describing the OPLL, needs to be solved in order to accurately quantify the stability of the loop in terms of bandwidth, time delay and loop gain, in the presence of a time delay.

In this paper, the influence of time delay in a balanced OPLL [3] with a Proportional Integrator (PI) filter is investigated using a DDE. The limitations, which a time delay imposes on the PI filter bandwidth, at increasing values of loop gain, are investigated by numerical simulations. Furthermore, simple expressions governing the stability properties of the loop, in the presence of time delay, are derived. For this purpose, three standard loop filters are considered: a PI filter, a Low Pass (LP) filter and an Active Lag (AL) filter. The derived expressions are used to perform an optimisation in terms of the selected loop filters.

Model set-up

The model set-up of the balanced OPLL-based clock recovery is shown in Figure 1. Based on this model, a general non-linear DDE is derived.

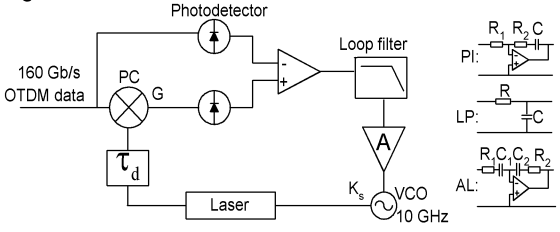

Figure 1. *Schematic set-up.*

The total accumulated time delay is schematically indicated to occur between the optical clock generating laser and the phase comparator (PC).

The phase comparator mixes the optical OTDM data signal (160 Gb/s) with the locally generated optical clock signal at the base rate (10 GHz), producing an error signal. The mixing process corresponds to a mathematical multiplication with a mixer gain, G. In practise, non-linear processes like FWM in SOAs can be used to achieve the mixing, as in the experimental realisation that this model is based on [4]. The error signal is an offset sinusoidal with frequency Δf, given by the difference between the 16'th frequency component of the clock signal and the line rate of the data. The amplitude of the error signal is s_1c_{16}, which is a harmonic product between the 1'st and 16'th Fourier frequency component of the corresponding data and clock signal. The balanced photodetection (BW 100 MHz) provides the subtraction of the DC level from the error signal, which results in a bipolar error signal. This subtraction also helps stabilise the error signal against fluctuations in the input powers. The signal is then low pass filtered and fed back to the VCO, which controls the optical clock generating laser. The data signal is a 160 Gb/s PRBS modulated (2^9-1) pulse train (FWHM 2.5 ps). The FWHM of the clock signal pulses T^{clk} is in the order of 1 ps, since this results in an optimum value of the harmonic product [5].

Numerical results

In this section, PI filter bandwidth limitations are determined as the loop gain, K, is increased from relatively small to large values. In Figure 2 and 3, the lock-in time is calculated as a function of time delay (τ_d) in the loop for PI filter bandwidths ranging from 500 kHz to 5 MHz. K is defined as the product between the gain of the VCO (K_s), the gain of the electrical amplifier (A), the responsivity of the photodiode (R) and the mixer gain (G).

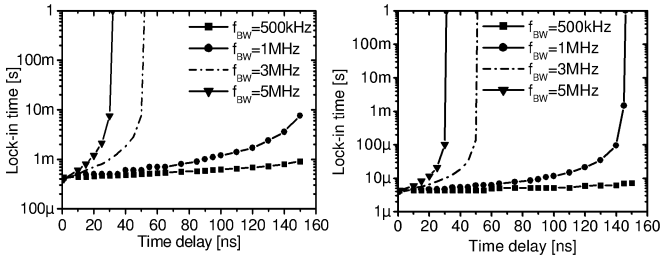

Figure 2. *Lock-in time as a function of increasing time delay. (a) K=70 MradA/sVW. (b) K=700 MradA/sVW*

Several results, in Figure 2, are worth noting. First, there exists a critical value of time delay for a specific PI filter bandwidth above which the lock-in time goes to infinity (the loop does not lock). Secondly, for low values of K, Figure 2(a), the loop can obtain a lock as long as $\tau_d<1/2\pi f_{bw}$. This requirement is similar to the one obtained by the linearised PLL model [2]. When the loop gain is increased to 700 MradA/sVW, Figure 2(b), the critical value of time delay for PI filter bandwidths of 3 MHz and 5 MHz remains unchanged. However, the condition $\tau_d<1/2\pi f_{bw}$ does not in this case secure

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locking for the bandwidth of 1 MHz. In Figure 3, the loop gain is increased to a relatively large value: 70 GradA/sVW. A general decrease in critical value of time delay is observed and $\tau_d<1/2\pi f_{bw}$ does not secure locking for any of the considered bandwidths. Figures 2 and 3 indicate that the loop dynamics change drastically as the loop gain is increased.

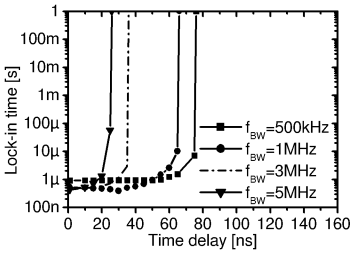

Figure 3. *Lock-in time as a function of increasing time delay. K=70 GradA/sVW.*

Small signal analysis

The numerical model is quite complex and requires numerical integration. In many cases, it is therefore of significant practical value to have simple, albeit approximate, analytical results by which the overall behaviour of the loop can be evaluated. We have therefore, as an alternative approach, performed a Small Signal Analysis (SSA) of the OPLL with selected standard loop filters: a PI, an LP and an AL filter.

For small values of time delay the eigenvalues, $\lambda_{1,2}$ of the OPLL with a PI filter can be approximated as:

$$\lambda_{1,2} = \frac{(\tau_d - \tau_2)\xi}{2\tau_1 - 2\tau_2\xi\tau_d} \pm \sqrt{\frac{(\tau_2 - \tau_d)^2\xi^2 - 4(\tau_1 - \tau_2\xi\tau_d)\xi}{2\tau_1 - 2\tau_2\xi\tau_d}} \qquad (1)$$

where $\xi=2Ks_1c_{16}$, $\tau_2=1/2\pi f_{bw}$ is the integration time and τ_1 is inversely proportional to the PI filter gain. If the eigenvalues are real, both eigenvalues need to be negative in order to obtain a stable locking. Otherwise, the loop will not obtain a lock. However, if the eigenvalues are complex, the real part of both eigenvalues needs to be less than zero in order to obtain stable locking. For relatively small values of the loop gain (K≤70 MradA/sVW), the eigenvalues are complex and the locking can be obtained as long as $\tau_d<\tau_2$. This is in accordance with Figure 2(a).

Until now an OPLL with a PI filter has been investigated. We have seen that the time delay limits the performance of the loop and are therefore encouraged to investigate the dynamics of the OPLL with an LP and an AL filter, in the presence of time delay. Performing the SSA for the OPLL with an LP filter, the eigenvalues are approximated as:

$$\lambda_{1,2} = \frac{-1 + \tau_d\xi}{2\tau_1} \pm \sqrt{\frac{(1 - \tau_d\xi)^2 - 4\tau_1\xi}{2\tau_1}} \qquad (2)$$

where $\tau_1=1/2\pi f_{bw}$. If the eigenvalues are complex, the locking condition for the OPLL with a LP filter becomes: $\tau_d<1/\xi$. This implies that by decreasing the loop gain the performance of the OPLL improves.

Similarly, the eigenvalues when the loop filter is an AL become:

$$\lambda_{1,2} = \frac{-1 + (\tau_d - \tau_2)\xi}{2\tau_1 - 2\tau_2\xi\tau_d} \pm \sqrt{\frac{(1 - (\tau_d - \tau_2)\xi)^2 - 4(\tau_1 - \tau_2\xi\tau_d)\xi}{2\tau_1 - 2\tau_2\xi\tau_d}} \qquad (3)$$

where τ_1 and τ_2 are inversely proportional to the bandwidth and stopband of the AL filter, respectively. If the eigenvalues are complex, it can be observed by examining equation (3) that the locking condition, in the presence of time delay, is: $\tau_d<\tau_1/\tau_2\xi$. By decreasing the AL filter bandwidth, increasing the stopband and decreasing the loop gain the locking condition can be improved.

Optimization of the loop

In the presence of time delay, the dynamics of the OPLL are strongly influenced by the loop filter. For practical applications, we would like to determine the loop filter, which minimises the limitations imposed by the presence of time delay. Using equations (1), (2) and (3) we have calculated, in Table 1, the maximum allowed value of time delay in the loop, which ensures stable locking for three selected bandwidths of PI, AL and LP filters.

BW	PI filter	AL filter	LP filter
1 MHz	155 ns	125 ns	96 ns
5 MHz	31 ns	28 ns	22 ns
10 MHz	15.5 ns	12.5 ns	9.6 ns

Table 1. *Critical value of time delay for selected values of bandwidth for the three loop filters.*

It can be seen from Table 1, that the allowed value of time delay in the loop is maximised when the loop filter is a PI filter. The lowest value of allowable time delay is obtained when the loop filter is a LP filter.

Conclusion

Numerical simulations have shown that for large values of loop gain, the OPLL operates in a non-linear regime. As the loop gain is increased, the PI filter bandwidth requirements become more stringent than was predicted by the linearised model. Using analytical expressions, obtained by small signal analysis, we have compared bandwidth requirements for the three standard loop filters, in the presence of time delay. By choosing a PI filter as a loop filter, the bandwidth can be maximised.

Acknowledgements

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