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AN IMPLANTABLE CMOS SIGNAL CONDITIONING SYSTEM FOR RECORDING NERVE SIGNALS WITH CUFF ELECTRODES

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ABSTRACT

In this paper, we propose a system architecture for recording nerve signals with cuff electrodes and we develop the key component in this system, the small-input, low-noise, low-power, high-gain amplifier. The amplifier is implemented using a mixture of weak- and strong-inversion transistors and a special off-set compensation technique; it's performance is validated using Spice simulations.

1. INTRODUCTION

Every year thousands of individuals sustain a spinal cord injury, with a significant impact on the patient's life. Recent efforts in biomedical engineering address the issues of electronically monitoring and stimulating paralysed extremities [1, 2, 3, 4]. These techniques are already used in volunteers to regain foot control of early multiple sclyroses patients and to assist the hand grip of tetraplegic persons [2].

Our involvement in this research is to develop implantable devices which will minimise the risk of infections by ensuring skin continuity [5]. In that way a bidirectional inductive link transmits power, control signals and feedback between the external control unit and the damaged nerve. This paper reports a subthreshold approach to biomedical signal amplification and nerve signal recording. An alternative approach to offset cancellation, with minimal impact at the input node, is presented which may find use in other amplifying schemes.

2. IMPLANTED SYSTEM

A special electrode is used in order to establish the necessary electrical contact with the nerve. This so called *cuff electrode* (figure 1) has a length of $10 - 20mm$ and physically connects the nerve to the implanted electronic device [1]. The electrodes are placed around the nerve by the use of local anaesthesia. The contact resistance after implantation is about $1k\Omega$; the nerve however gradually builds up a protective layer, which increases the resistance to $5k\Omega$ [1] (aging process). The implanted device (figure 1) consists of an inductive loop around a silicon chip and some discrete components. The control signals and the power needed to operate the circuit are provided by an external control unit through the skin, by the use of an inductive link.

The implanted nerve stimulator has been reported elsewhere [5]. The feedback path must record very small ($\pm 10\mu V$), noisy nerve signals with very tight power requirements ($100\mu A$) posed by the induced power supply. The recording circuit facilitates the identification of the exited nerve state, by comparing the nerve signal to the background activity. Because we are not interested at the absolute value
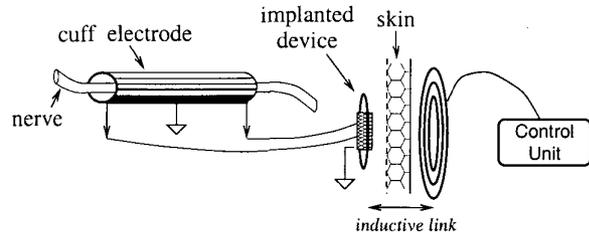

Figure 1. The overall implanted system

of the input signal, a 10%-15% variation of the gain or harmonic distortion can be tolerated.

Even if it was possible to record the nerve signals with large accuracy, essentially we would be monitoring the thermal noise introduced by the cuff electrode. It therefore makes sense to perform some local signal processing in order to reduce the noise:

3. NOISE AVERAGING

The signal recovery technique [1, 2] is similar to demodulating an amplitude modulated signal. The input is amplified, antialiased and sampled at $10kHz$. The digitised signal is rectified, low-pass filtered and downsampled thus the output results at a frequency of $20Hz$, giving the envelope of the input nerve signal.

The variance of the nerve signal is:

$$\sigma_n^2 = Var(V_n^*) = E\{(V_n^* - E\{V_n^*\})^2\} = E\{(V_n^*)^2\}$$

where V_n^* and $\mu_n = E\{V_n^*\} = 0$ are the (stochastic) nerve signal and its mean respectively.

The rectified signal Y^* is given by the equation:

$$Y^* = \sqrt{V_n^{*2}} \quad and \quad E\{Y^*\} = E\{\sqrt{V_n^{*2}}\} = \mu_y$$

were μ_y is the mean of the rectified signal. The variance of Y^* is given by the equation:

$$\sigma_y^2 = E\{(Y^* - E\{Y^*\})^2\} = E\{(\sqrt{V_n^{*2}} - \mu_y)^2\}$$
$$= E\{V_n^{*2} + \mu_y^2 - 2\mu_y\sqrt{V_n^{*2}}\}$$
$$= \sigma_n^2 + \mu_y^2 - 2\mu_y^2 = \sigma_n^2 - \mu_y^2$$

If the nerve signal is assumed to be Gaussian then we can find $\mu_y = \sqrt{2/\pi} \cdot \sigma_n$ and $\sigma_y^2 = (1 - 2/\pi) \cdot \sigma_n^2$.

After averaging the rectified signal the variance is reduced by $10kHz/20Hz$ and the overall output has a mean value

and spread given b y:

$$\mu_y = 0.798 \cdot \sigma_n , \quad \sigma_y = 0.027 \cdot \sigma_n$$

where we have assumed uncorrelated samples and that the variance does not change during the 500 samples. Thus we have a signal to noise ratio from the envelope detection procedure of $29dB$. Such a resolution might seem small for signal processing tasks, how ev er it is adequate to evaluate the state of a h uman nerve.

4. THE PROPOSED ARCHITECTURE

The overall system architecture is shown in figure 2. A C coupling is used to minimise an y DC offsets at the input (which can be hundreds of millivolts from the electrode). The $\pm 10\mu V$ input signal is subsequently amplified $10k$ times to a $\pm 100mV$ signal, whic hwill be antialiased by the use of a low-pass filter with a cut off frequency of $5kHz$. An *Analogue to Digital Converter* (ADC) is used to digitise the signal and the digital post-processing will include band-pass filtering [2], rectifying and averaging. The resultant samples will be transmitted by changing the load of the inductive link [6].
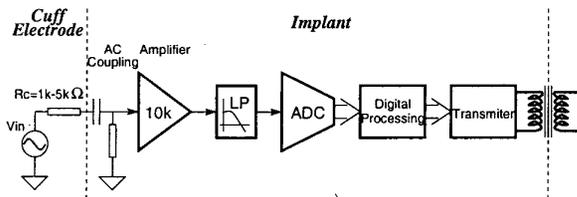

Figure 2. Overall circuit schematic

5. ANTIALIASING

As an antialiasing filter, w e use a single capacitor in conjunction with either the cuff electrode resistor or the second amplifier output resistance to achiev e a cut-off frequency of $5kHz$ (se section 6.2.). Oversampling is used to suppress high frequency noise folded down in the signal band. From a power point of view, it often makes sense to k eep low signal-to-noise ratio signal processing in the analogue domain [7]; how ever the signal processing done after the anti-aliasing filter can be made using very simple digital circuits, so in our case it makes sense to do the A/D conversion here. This also adds to the flexibility of the system.
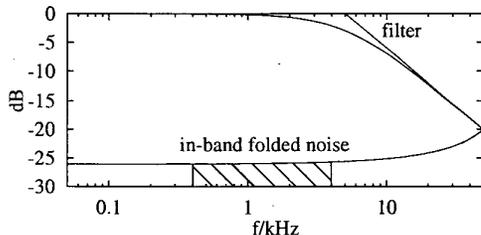

Figure 3. Aliasing effects

Our single pole, one capacitor filter has a $20dB/Dec$ response. Assuming a sampling frequency of $100kHz$ (10 times the Nyquist frequency), the normalised signal will be similar to that of figure 3. A t frequencies abov e $10kHz$ only the thermal noise of the input amplifier is present, because the

nerve signals are negligible [8, 2] and the device is shielded by the surrounding tissue [8]. The aliased thermal noise which is folded down in the signal bandwidth ($400Hz$ to $4kHz$) is atten uated more than $25dB$ compared to the in-band noise, and is therefore not important.

6. AMPLIFIER

The noise introduced by the amplifier is of prime importance to signal integrit y. Because of the minute signal from the electrode, it is crucial that it is amplified a lot immediately, using very few transistors (as these generate noise). The gate referred noise spectral densities of MOSFETs is approximately given by the equation:

$$\frac{v_i^2}{\Delta f} = 4kT\frac{2}{3}\frac{1}{g_m} + \frac{K_f}{WLC_{ox}f}$$

It is clear that the thermal noise can be reduced by increasing the transconductance (g_m) of a transistor and that the flicker ($1/f$) noise can be reduced by increasing the transistor area (WL). The transconductance of a MOSFET for the different modes of operation is given by:

$$\text{subthreshold} : \quad g_m = I_d/(n \cdot U_T)$$
$$\text{strong in version saturation} : \quad g_m = 2 \cdot I_d/V_{eff}$$

Where $U_T = 26.7mV$ at $37°C$ (the typical body temperature), $n \simeq 1.2$, and the typical effectiv e voltage $V_{eff} = V_{GS} - V_{T0} = 200mV$. Thus the transconductance to drain current ratio for a MOSFET is maximised in subthreshold operation and in our case it is about 3 times larger. F urthermore flicker noise is linked to surface effects in MOSFETs; therefore the transistor should exhibit low er $1/f$ noise (smaller K_f) because subthreshold operation is dominated by diffusion current deep in the substrate [9, 10].
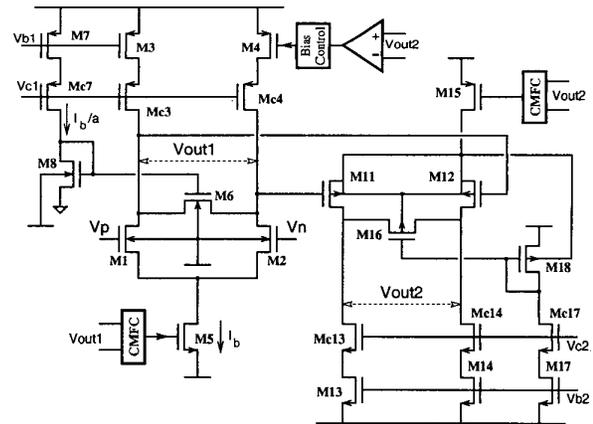
Figure 4. Amplifying stage

Ha ving these noise considerations in mind, we propose the amplifier sho wn in figure 4. The signal from the cuff electrode is AC coupled to the input transistors (M_1, M_2) of the first stage to eliminate the DC offset in the electrode. The input transistors operate in subthreshold. The current needed to ensure low thermal noise is $35\mu A$, a v ery large current for subthreshold operation; for this reason the NMOS input transistors should be designed to be very wide. The biasing current is supplied by the cascoded current sources M_3, M_{c3}

and M_4, M_{c4}. Those transistors operate in saturation to ensure good operation as current sources and to minimise their contribution to noise [11]. A *Common Mode Feedback Circuit* (CMFC) is used to bias M_5 to stabilise the output common mode voltage to zero. M_6 operates in subthreshold and forms the load resistor which controls the gain of the amplifier.

This gain is given by the equation:

$$A_{v1} = g_{m1} \frac{r_{ds6}}{2} = \frac{W_1/L_1}{W_6/L_6} \cdot \frac{1}{2 \cdot n} = 100 \qquad (1)$$

where W_i, L_i the transistor width and length, n expresses the bulk effect and is given by:

$$\frac{1}{n} = 1 - \frac{\gamma}{2\sqrt{V_G - V_{T0} + (\gamma/2 + \sqrt{\Phi_o})^2}} \simeq \frac{1}{1.2}$$

were all the voltages are given with respect to the bulk voltage. Most of the A_{v1} mismatch in equation (1) is due to n variations. However if a maximum 30% variation in all γ, V_{T0} and Φ_o is assumed n varies only by 5%; well within a tolerable variation.

Equation (1) is valid provided that $V_{G1}/nU_T - V_{S1}/U_T = V_{G6}/nU_T - V_{S6}/U_T$. The transistors M_7, M_8 generate V_{G6} to ensure that this assumption is valid:

$$I_{d3} = I_{d7} \Longrightarrow I_{d01} \cdot e^{\frac{V_{G1}-nV_{S1}}{nU_T}} = I_{d08} \cdot e^{\frac{V_{G8}-nV_{S8}}{nU_T}}$$

where $V_{G,Si}$ the gate, source voltage of transistor i with respect to the bulk, $I_{d01} = I_{d08}$ is given in [7]. The CMFC ensures that $V_{S8} = V_{D,S6} = 0V$ and $V_{G8} = V_{G6}$ thus the assumption is valid and A_{v1} is given by (1). In practice I_{d8} is a scaled down version of I_{d1}, to reduce power consumption.

The second amplifier has a similar topology with the first one, though all transistors operate in strong inversion because the signal levels here are too big for the subthreshold version. M_{16} operates in the linear region and its effective voltage defines the dynamic range of the amplifier. The noise of this amplifier referred to the input is divided by the gain A_{v1}^2 therefore the bias current can be significantly reduced to $1\mu A$. The gain of the second amplifier is and is given by the equation:

$$A_{v2} = g_{m11} \frac{r_{ds16}}{2} = \frac{W_{11}/L_{11}}{2 \cdot W_{16}/L_{16}} = 100 \qquad (2)$$

A C coupling between the two amplifiers maybe considered, in order to minimise the effect that offsets might have at the output. In that way an overall gain of 10k is realized in two stages with a gain of 100 each. Therefore the input signal is amplified from $\pm 10\mu V$ to about $\pm 100mV$.

6.1. Offset cancellation

Offsets at the output of the amplifier can be easily removed, since we are only interested at the AC component of the nerve signal. However the task of cancelling the offset of the first stage is critical. The typical V_{T0} mismatch for a centroid layout of the input transistors, in the process used, is more than an order of magnitude larger than the maximum input signal. Such an offset will force the input transistors out of weak inversion in to saturation due to the high gain.

Switching the input will introduce charge feedthrough which will be much larger than the input voltage and couple charge back to the nerve which can easily be damaged. Therefore an alternative offset cancellation technique must be employed. Instead of using switches tuning the current

I_{d4} is proposed. A continuous time bias control is applied to regulate the bias current by ensuring that the output of the second amplifier 4 is zero. In this case if the feedback loop is slow, the AC signal component is effectively high-pass filtered. An alternative approach would require a current *Digital to Analogue Converter* (D A C) and a reset cycle to set the bias current in regular (relatively long) intervals to ensure zero output. This approach offers extended flexibility to the circuit. This offset cancellation has an effect of introducing current mismatches,

$$\Delta I_{1,2} = 1 - \frac{I_1}{I_2} = 1 - e^{\frac{V_{G1}-V_{G2}}{n \cdot U_T}} = 3\% \qquad (3)$$

However such a current mismatch will only generate offsets and will not affect the gain to a first order approximation.

Following the method presented above it is possible to realize accurate offset cancellation, without the use of switches which will introducing dynamic input offsets. It is this offset scheme that makes the implementation of such a subthreshold amplifier possible.

6.2. Reducing power consumption

The power is provided by the inductive link, therefore reducing the power consumption if of a prime importance. The most energy hungry device is the subthreshold amplifier, which uses 90% of the overall current to suppress the input noise. There are two ways of reducing power consumption of this amplifier

The first is to lower the power supply voltage for the first amplifier. This amplifier can operate with very low supply voltage: because the input transistors operate in subthreshold and the signal levels are very small, the overall $V_{dd} - V_{ss} \geq V_T - 100mV + 2V_{eff} \simeq 1V$.
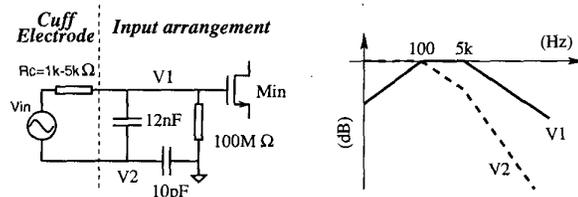

Figure 5. Input filter to reduce switching noise

An alternative and more power efficient way, is to lower the biasing currents of the subthreshold amplifier in between the sampling intervals. The amplifier needs $1\mu s$ to settle down, therefore a small 5% duty cycle may be used, reducing the overall power consumption.Nevertheless, when the biasing current on M_1,M_2 increases (to suppress the input thermal noise), $V_{S1} = V_{S2}$ must decrease (because $V_{G1} \simeq V_{G2} \simeq 0V$), introducing charge feedthrough (through the relatively large parasitic capacitors C_{GS1}, C_{GS2}) and coupling charge back in the nerve.

The differential input scheme should minimise charge feedthrough effects and a modified input filter arrangement (figure 5) will significantly reduce this noise. This bandpass filter used for AC coupling and antialiasing, ensures that the relatively large antialiasing capacitance ($12nF$) provides a large charge reservoir, which holds the gate voltages at the gate of V_{GS1}, V_{GS2} constant. (Note that when switching the bias current in the amplifier, the antialiasing filter must be placed before the amplifier; external components are necessary for this solution).

7. SIMULATION RESULTS

A subthreshold amplifier has been simulated using the models of a $0.5\mu m$ process. Those simulations demonstrate the applicability of the o verall design, with a view to do the layout of a chip to test the circuit. The biasing currents $I_{d3} = I_{d4}$ w ere designed to be 33 .5μA with an effective voltage of $300mV$; this enables the current sources to be switched down to $1\mu A$, for sa ving power, with an effective voltage of about $50mV$. $I_6 = 250nA$ for a maximum input voltage. The gain of the amplifier is 103 and the frequency response is shown in fig- ure 6. The amplifier has a $3dB$ cut-off frequency at $1.5MHz$. This is due to the large bias currents whic hare needed for thermal noise suppression.
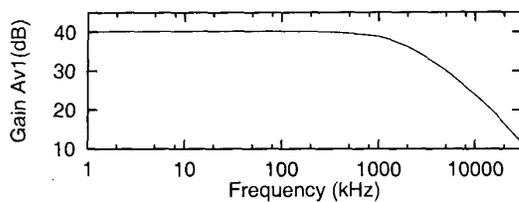

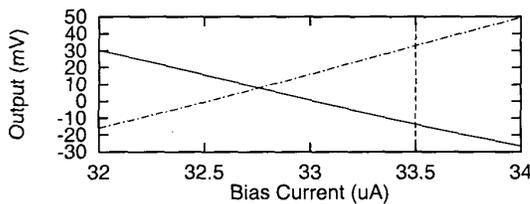
Figure 6. Subthreshold amplifier frequency response

Figure 7. Current tuning for offset cancellation

The offset cancellation is shown in figure 7. A worst case $\Delta V_{T0} = 1mV$ between M_1, M_2 was introduced. This forces the output to become 50mV. If the current I_{d4} is reduced to $32.7\mu A$ then this offset is cancelled. One can observe that the this cancellation can be made very accurate, as long as the bias con trol has a sufficient resolution. The current mismatch $\Delta I_{3,4} = 2.4\%$. Because te signal levels are so small, if the offset cancelling scheme is capable of keeping the amplifier at the correct bias point, distortion is much low er than what we can tolerate.

8. CONCLUSIONS

In this paper an implantable CMOS system for recording nerv e signals w as investigated. This device will find use in restoring the mobility of human paralysed extremities. Be- cause the signals are very small ($\pm 10\mu V$), the most critical component of the circuit is the amplifying stage. The use of subthreshold circuits, with large transconductance to current ratio, improv ed noise c haracteristics and low-v oltage proper- ties, operating in a constant temperature environment ($37^\circ C$ body temperature), make our approach feasible for the ex- tremely tight pow er requiremerts posed by the nature of the implantable device.

Relatively large offsets, distortion, or mismatches can be cancelled by the digital post processing algorithm. Neverthe- less the implementation of such a subthreshold amplifier was made possible by ensuring that an accurate threshold v olt- age offset cancellation (without the use of switches which will introducing dynamic input offsets) was available. A similar bias current tuning approach may be used for offset cancel- lation in different amplifying schemes.

The authors finally propose tw o curren t reducing tech- niques, to further reduce power consumption. In that w ay more than one recording circuits may be used in an im- plantable device to enhance the flexibility of the device.

Presen tly test chips are being fabricated to experimentally verify the designs proposed in this paper.

REFERENCES

[1] M. Thomsen, *Char acterisation and optimisation of whole nerve recording cuff electrodes*. PhD thesis, Center F or Sensory-Motor In teraction, University of Aalborg, 1998.

[2] A. Lickel, *R estontion of Lateral Hand Gr asp in a T r- traplegic Patient Applying Natural Sensory F eedb ack* PhD thesis, Center For Sensory-Motor Interaction, Uni- versity of Aalborg, 1998.

[3] D. B. Popovic, R. B. Stein, K. L. Jo vano vic,R. Dai, A. Kostov, and W. W. Armstrong, ."Sensory nerv e recording for closed-loop control to restore motor func- tions," *IEEE T ransactions on Biomedical Engineering*, vol. 40, no. 10, pp. 1024–1031, 1993.

[4] C. Enokawa, Y. Y oneza w a,H. Maki, and M. Arit- omo, "Microcontroller-based implantable telemetry sys- tem for sympathetic nerve activity and ECG measure- ment," in *A nnual International Confeence of the IEEE Engineering in Medicine and Biology*, vol. 5, pp. 2232– 2234, IEEE, 1997.

[5] G. Gundason, E. Brunn, and M. Haugland, "An im- plan table mixed analog/digital neural stimulator cir- cuit," in *International Symposium on Circuits and Sys- tems*, vol. 5, (Orlando), pp. 375–8, IEEE, 1999.

[6] Z. T ang, B. Smith, J. H. Schild, and P . H. P eckham, "Data transmission from an implantable biotelemeter by load-shift keying using circuit configuration modulator," *IEEE Transactions on Biomedical Engineering*, vol. 42, no. 5, pp. 524–8, 1995.

[7] C. C. Enz and E. A. Vittoz, "CMOS low-pow er ana- log circuit design," in *Emerging T echnolo giesDesigning L ow Power Digital Systems* (I. R. K. Cavin and W. Liu, eds.), pp. 79–133, IEEE, 1996.

[8] Q. Huang and M. Oberle, "A 0.5-mW passive telemetry IC for biomedical applications," *IEEE Journal of Solid- State Circuits*, pp. 937–46, 1998.

[9] J. Chang, A. A. Abidi, and C. R. Viswanathan, "Flicker noise in CMOS transistors from subthreshold to strong in version at v arious temperatures,"*IEEE Transactions on Electron Devices*, vol. 41, no. 11, pp. 1965–71, 1994.

[10] M. Aoki, H. Katto, and E. Yamada, "Low-frequency 1/f noise in MOSFETs at low curren t levels," *Journal of Applied Physics*, vol. 48, no. 12, pp. 5135–40, 1977.

[11] K. G. Lamb, S. J. Sanchez, and W. T. Holman, "A low noise operational amplifier design using subthreshold op- eration," in *Pro ceedings of Midwest Symposium on Cir- cuits and Systems*, pp. 35–8 vol.1, IEEE, 1998.