High-Bandwidth, High-Efficiency Envelope Tracking Power Supply for 40W RF Power Amplifier Using Paralleled Bandpass Current Sources

Høyerby, Mikkel Christian Wendelboe; Andersen, Michael Andreas E.

Published in:
IEEE 36th Conference on Power Electronics Specialists, 2005

Link to article, DOI:
10.1109/PESC.2005.1582030

Publication date:
2005

Document Version
Publisher's PDF, also known as Version of record

High-Bandwidth, High-Efficiency Envelope Tracking Power Supply for 40W RF Power Amplifier Using Paralleled Bandpass Current Sources

Mikkel C. W. Høyerby
Technical University of Denmark
Building 325
Dk-2800 Lyngby
Denmark
mwh@oersted.dtu.dk

Michael A. E. Andersen
Technical University of Denmark
Building 325
Dk-2800 Lyngby
Denmark
ma@oersted.dtu.dk

Abstract - This paper presents a high-performance power conversion scheme for power supply applications that require very high output voltage slew rates (dV/dt). The concept is to parallel 2 switching bandpass current sources, each optimized for its passband frequency space and the expected load current. The principle is demonstrated with a power supply, designed for supplying a 40W linear RF power amplifier for efficient amplification of a 16-QAM modulated data stream.

I. INTRODUCTION

Power conversion through paralleled converters is useful when an application calls for higher performance than can be achieved with a single converter. Examples are the combination of a buck converter and a linear power stage where improved load step performance is required in a DC-DC converter [1] and the combination of a class-D and a linear power stage for audio amplification with both high efficiency and low distortion [2]. In both these applications, the linear power stage supplies very little average power.

The combination of 2 or more identical switching converters is frequently seen in form of the multi-phase buck converters used for microprocessor power supplies.

In applications where both significant DC and high-frequency AC currents must be supplied, exchanging the fast, linear converter used in [1] with a high-bandwidth switching converter offers an opportunity for increasing efficiency, since a switching converter is substantially more efficient than a linear converter at high load currents.

An emerging application for DC+AC supplies is envelope tracking power supplies for RFPAs (Radio Frequency Power Amplifiers), where QAM (Quadrature Amplitude Modulation) is used.

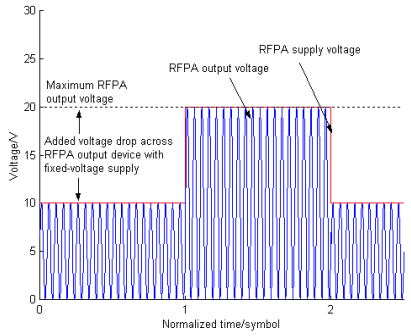

Figure 1 Idealized example of envelope tracking supply voltage for an RFPA for 16-QAM signal amplification.

The concept of using an envelope tracking power supply for an RFPA has been well known for a number of decades [3]. The basic idea is to maximize the efficiency of a linear RFPA by supplying only the minimum necessary supply voltage an any given time, as illustrated in Figure 1. Recently, the use of switch-mode techniques [4], [5] has resulted in small and efficient envelope tracking power supplies for low-power QPSK (Quadrature Phase Shift Keying) cellular mobile telephony applications.

The increasing use of QAM over QPSK, to increase bandwidth efficiency potentially imposes higher demands on power supply output voltage slew-rate (dV/dt) due to fundamental differences between these modulation schemes. The UMTS (Universal Mobile Telecommunications System) standard for next-generation mobile telephony systems incorporates QAM in some of its higher-speed data transmission modes.

This paper examines a possible solution to designing high-efficiency envelope tracking power supplies, based on using paralleled switching power converters. The 3 main issues discussed in this paper are:

- Comparison between a single converter and the parallel configuration.
- Derivation of a suitable control method.
- Experimental verification.

II. DESIGN SPECIFICATIONS

The practical design problem considered concerns the design of an envelope tracking power supply for an X-band 40W RFPA for a satellite telephony system. The RFPA amplifies a 16-QAM modulated data stream with 150kHz symbol rate, thus requiring the power supply to effectively track a 75kHz square envelope. The following design parameters are obtained:

Table 1 Considered design specifications.

Input voltage (V_{in})	30V
Output voltage (V_{out})	Between $1/3 \cdot V_{in}$ and $2/3 \cdot V_{in}$
Output current	Up to 2A
Equivalent load resistance	$\approx 10\Omega$
Output transition time	Less than 2µs
Output ripple voltage	As low as possible

Where the requirement for a 2µs transition time is set as a compromise between maximizing RFPA efficiency and minimizing the required power supply bandwidth.

III. PROPOSED POWER CONVERSION SCHEME

In high dV/dt applications, high control bandwidth is required. In the considered example, around 300kHz of closed-loop bandwidth is required, leading to a minimal switching frequency of around 1.5MHz if a single buck converter is used. In the voltage range considered, switching losses will be the dominant source of power loss, so by minimizing the current delivered by the fast switching buck converter, its efficiency can be maximized. This can be accomplished by diverting the DC load current to a slower, more efficient buck converter (see Figure 4). However, the slow converter must have a non-zero bandwidth, since the average (past to future) output current, logically enough, is unknown. It must therefore adapt to the current load current, which it should do as quickly as possible to minimize loading of the fast converter. In a proper design, the slow converter output voltage large-signal control bandwidth will be limited by inductor current slew rate, which thus provides a suitable 'adaptation' time constant. The impact of having non-zero control bandwidth, limited by slew-rate is shown in Figure 4.

Note that the inductor currents shown are averaged over one switch cycle (no ripple) and that output capacitor charging/discharging currents are disregarded.

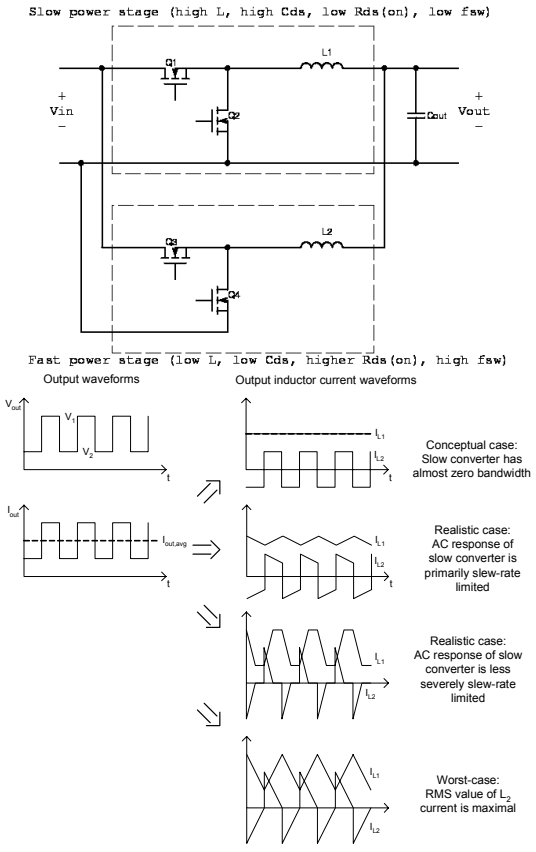

Figure 2 Principal illustration of the proposed power conversion scheme.

Comparison between a single-converter and a dual-converter solution is made based on the conceptual function of the paralleled converters, since RMS inductor currents are otherwise dependent on both inductor values (slew-rate) and square-signal frequency. The worst-case L_2 RMS current is a factor of $2(\sqrt{3})^{-1}\approx 1.15$ times higher than in the conceptual case, so the error made cannot seriously affect the outcome of the comparison.

The following expressions apply for the RMS values of the shown (averaged) conceptual inductor currents:

$$I_{L1,RMS} = \frac{V_1 + V_2}{2R_{load}} \qquad I_{out,RMS} = \sqrt{\left(\frac{V_1 + V_2}{2R_{load}}\right)^2 + \left(\frac{V_1 - V_2}{2R_{load}}\right)^2}$$

$$I_{L2,RMS} = \frac{V_1 - V_2}{2R_{load}}$$

If V_1=20V and V_2=10V (worst-case condition in the considered application), L_1 carries 3 times the RMS current of L_2, and the RMS current in L_2 is thus reduced by a factor of $\sqrt{10}$, when comparing to a single buck converter. This reduction in RMS current is reflected directly to the MOSFETs, allowing the $R_{ds(on)}$ of Q_3, Q_4 to be 10 times higher for a fixed conduction loss. This leads to approximately 10 times lower gate charge, and thus, switching losses. The decrease in switching losses in the fast converter should then be able to accommodate the extra losses associated with adding the slow buck converter.

Reducing the RMS switch current in the fast converter also causes reduced switching (peak) currents, directly contributing to further reduction of switching losses.

In a comparable 2-phase interleaved buck solution, each converter will deliver half the output current. This enables the use of MOSFETs with 2 times higher $R_{ds(on)}$ and thus 2 times lower Q_g for fixed conduction losses, compared to a single buck solution. The FETs in the 2-phase buck will thus switch twice as fast and at half the current, reducing switching losses by a factor of 4. So, provided that efficiency of the slow converter in the proposed scheme is high enough, efficiency will be superior to that of a 2-phase interleaved buck solution.

IV. PROPOSED CONTROL SCHEME

The initial idea for controlling the paralleled converters is to operate the 2 output inductors as current sources, since current sources can be paralleled without problems. This requires each inductor current to be controlled individually. The Laplace-domain block diagram model of the paralleled, current-controlled buck converters is shown in Figure 3. This model is an extension of the single buck converter model utilized in [6].

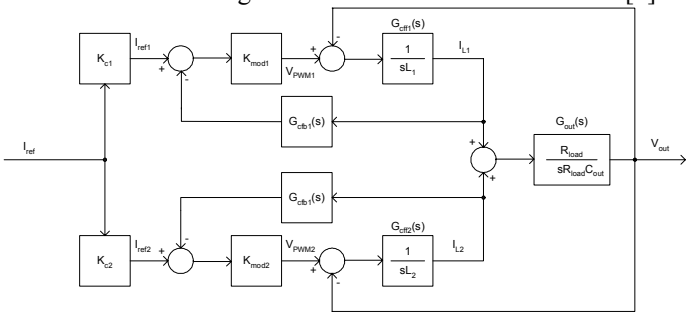

Figure 3 Block diagram of paralleled, current controlled buck converters.

The following transfer function expressions are found:

$$G_{c1}(s)=\frac{V_{out}(s)}{I_{ref1}(s)}=K_{\mathrm{mod}1}G_{out}(s)\frac{G_{cff1}(s)}{1+G_{cff1}(s)(K_{\mathrm{mod}1}G_{cfb1}(s)+G_{out}(s))}$$

$$G_{c2}(s)=\frac{V_{out}(s)}{I_{ref2}(s)}=K_{\mathrm{mod}2}G_{out}(s)\frac{G_{cff2}(s)}{1+G_{cff2}(s)(K_{\mathrm{mod}2}G_{cfb2}(s)+G_{out}(s))}$$

$$G_{c}(s)=\frac{V_{out}(s)}{I_{ref}(s)}=K_{c1}G_{c1}(s)+K_{c2}G_{c2}(s)$$

$G_c(s)$ can be computed numerically using these expressions. In order to minimize measurement problems, current estimation via inductor voltage integration is utilized. As discussed in [6], this method causes the current loop to transit to voltage mode when the inevitable estimator low-frequency cut-off is reached. The transition into voltage mode has the benefit of lowering output impedance [7], and is the logical reason behind calling the closed current loop around L_1 a 'bandpass' current source. It is obvious that at least *one* of the inductor current loops has to operate down to DC, since paralleling voltage sources would be disastrous. Therefore, current estimation is only used on L_1, which carries the highest RMS current. In order to ensure that the DC current in L_2 is exactly 0, proportional-integral (PI) feedback is used in the current loop around L_2. Thus the closed current loop around L_2 is also a bandpass current source, with zero DC gain.

The derived current control scheme shown in Figure 4.

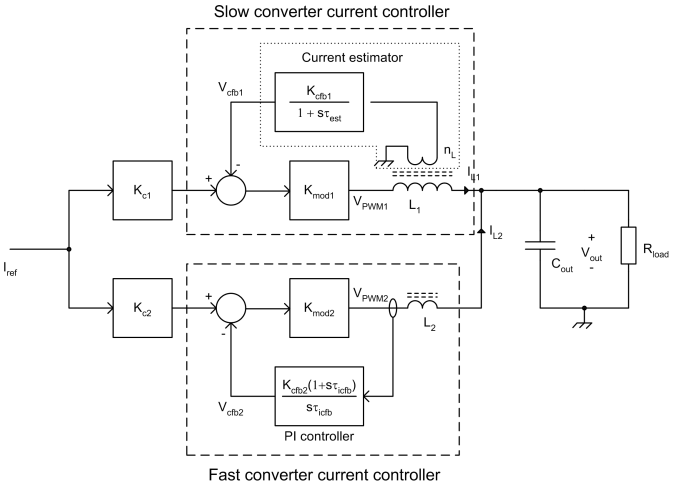

Figure 4 Principal illustration of the proposed current control scheme.

Table 2 Parameters used in current control loop design.

Output filter capacitor	C_{out}	200nF
Slow buck inductor	L_1	50µH
Fast buck inductor	L_2	2.2µH
Current estimator time constant	τ_{est}	300µs
Current estimator gain	K_{cfb1}	1
Inductor sense winding ratio	n_L	1:1
PI current compensator time constant	τ_{icfb}	300µs
Slow PWM modulator gain	K_{mod1}	100
Fast PWM modulator gain	K_{mod2}	100
Slow current loop gain	K_{c1}	1
Fast current loop gain	K_{c2}	1

The transfer function from current reference to output voltage, $G_c(s)$ is plotted for various values of R_{load} in Figure 5, using the parameters shown in Table 2.

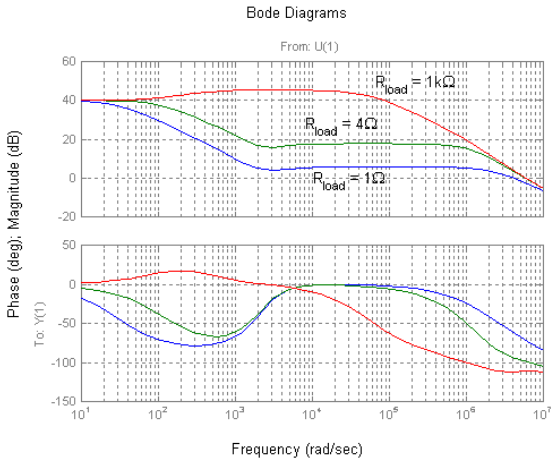

Figure 5 Combined closed-loop current controller transfer functions ($G_c(s)$) with different loads.

Using the selected parameters, the current controller transfer function is well behaved, and all transfer function complex pole/zero pairs have a damping factor > 1 for loads above 1Ω. Voltage control loop design is thus relatively straightforward. In order to increase mid-band loop gain (which is low at 1Ω), lag compensation is used, although this has the effect of decreasing phase margin at higher load resistances. No acceptable design is found suitable for the entire load range above 1Ω but fortunately, the converter aims for applications with load resistances above the 4-8Ω range. The problem observed is general for current controlled designs.

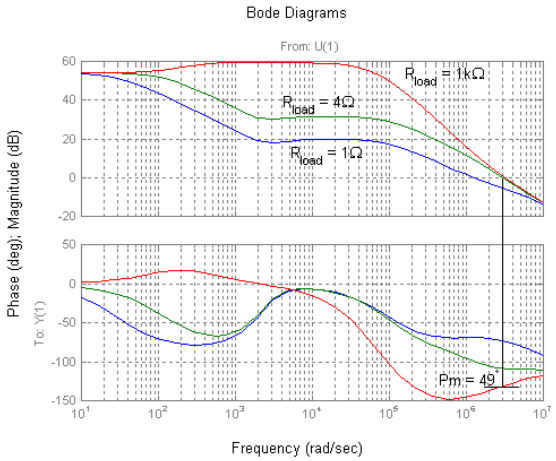

Figure 6 Open-loop voltage control loop transfer functions with different loads, demonstrating worst-case phase margin.

Table 3 Parameters used in voltage control loop design

Lag compensator pole time constant	τ_p	10µs
Lag compensator zero time constant	τ_z	0.82µs
Controller proportional gain	K_P	5

Using the voltage loop compensator parameters given in Table 3 results in the open- and closed-loop Bode plots shown in Figure 6 and Figure 7. The corresponding closed-loop step response is shown in Figure 8.

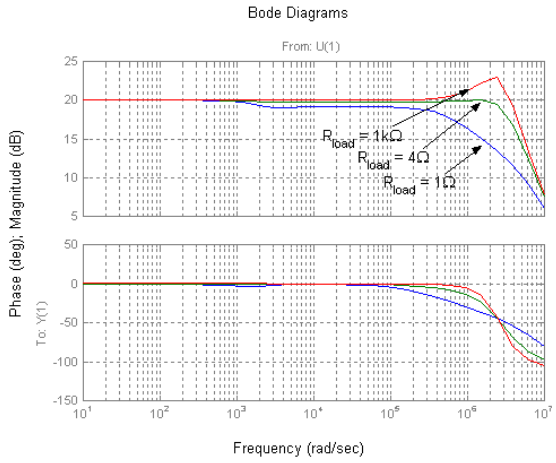

Figure 7 Closed-loop Bode plots of voltage control loop.

Adequate phase margin is obtained at all loads, while the output voltage settles at the correct value within 2µs for load resistances above 4Ω.

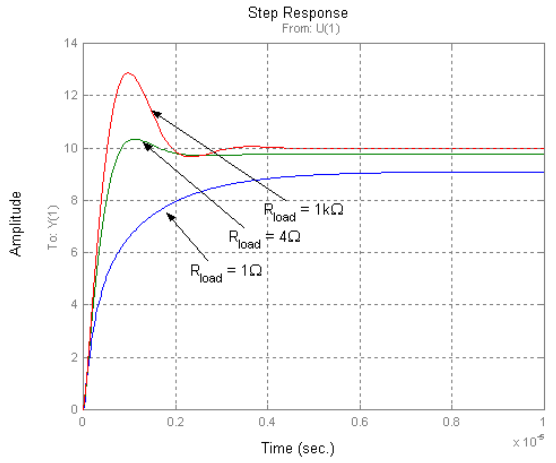

Figure 8 Step responses of closed voltage control loop showing that fast and well damped responses are achievable using the proposed control scheme.

The results obtained with the linear model are mainly useful for confirming that the paralleled converters can be controlled in a stable and fast manner. In the actual system, inductor current slew rates will limit the response speed of the power supply, regardless of the voltage loop gain provided. As will be shown, however, the calculated response times are well within range provided that output filter components are selected correctly.

V. PROTOTYPE DESIGN

Hysteresis control is used in both converters to maximize the control bandwidth per switching frequency ratio [6], [8]. The switching frequency of the fast converter is set to 1.5MHz, reflecting the control bandwidth requirement. The fast converter output filter cut-off frequency is chosen to allow sufficient output voltage slew rate. The L_2 filter inductor value is chosen as a compromise between minimizing ripple current and minimizing inductor size. MOSFETs for the fast converter are chosen with emphasis on low Q_g and C_{DS} to minimize the penalty for operating at high switching frequency, leading to use of the Fairchild FDD5612. This device has the lowest Q_g among considered 60V D-PAK MOSFETs (7.5nC), but still leads to switching losses being dominant.

The slow converter switching frequency is chosen for maximal efficiency. The L_1 filter inductor is finally chosen so that the slow converter contributes with acceptable output ripple voltage.

Closed-loop control bandwidth	B_{-3dB}	300kHz
Fast converter switching frequency	f_{sw2}	1.5MHz
Fast converter output filter cut-off frequency	$\frac{1}{2\pi\sqrt{L_2 C_{out}}}$	240kHz
Fast buck inductor	L_2	2.2µH
Output filter capacitor	C_{out}	200nF
Slow converter switching frequency	f_{sw1}	250kHz
Slow buck inductor	L_1	50µH

VI. SIMULATED RESULTS

A PSpice simulation model is used to verify the power supply design. As shown in Figure 9 and Figure 10, the designed control system leads to absence of DC current in L_2 while maintaining stability and fast response time (≈1.5µs) over the intended load range.

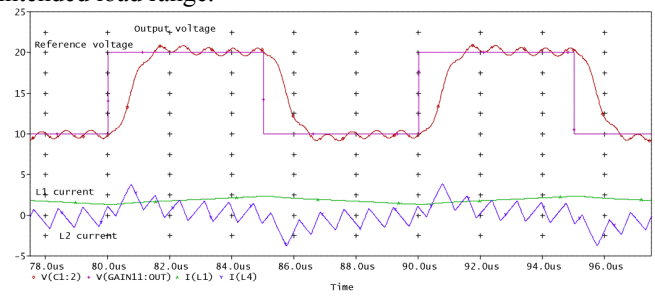

Figure 9 Simulated output (red) and reference voltages (magenta), L_2 (blue) and L_1 (green) buck inductor current. Converter driving 100kHz 10Vpp+15VDC square wave response into 8Ω.

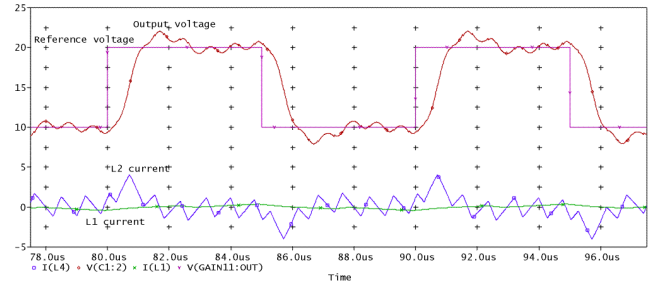

Figure 10 Simulated output (red) and reference voltages (magenta), L_2 (blue) and L_1 (green) buck inductor current. Converter driving 100kHz 10Vpp+15VDC square wave response into open load.

VI. ACHIEVED PRACTICAL RESULTS

A prototype power supply has been implemented, as shown in Figure 11, using a simple 2-layer PCB and low-cost components. Some precautions are necessary to prevent the 2 hysteresis controllers from synchronizing with each other through coupled switching noise. The problem is defeated through filtering at all hysteresis comparator input pins.

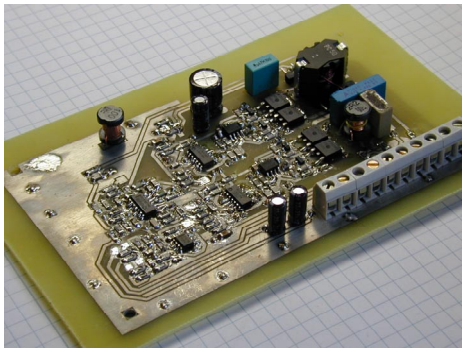

Figure 11 The constructed prototype power supply.

The 100kHz step response into 8Ω is shown along with PWM signal waveforms and inductor currents in Figure 13 and Figure 12. The response+settling time is 2µs, in accordance with specifications. The output voltage response is very similar to the simulated result (in Figure 9) apart from a small overshoot. This is probably due to unmodeled implementation dynamics in the simulation. The current responses are in good agreement, both regarding peak transient currents and ripple currents. It is especially evident that the fast converter supplies only the AC output current, while the slow converter handles the DC current, and as much AC current as allowed by L_1 current slew rate. The latter leads to the slow converter 'locking' onto the reference signal frequency, which is a feature of the hysteresis controller.

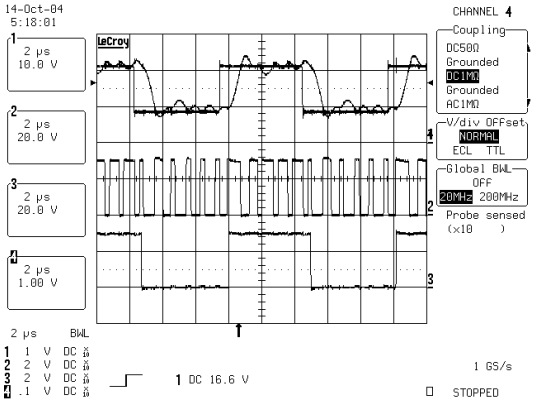

Figure 12 Output and reference voltages (top), HF (middle) and LF (bottom) buck PWM output voltages. Converter driving 100kHz 12Vpp+15VDC square into 8Ω.

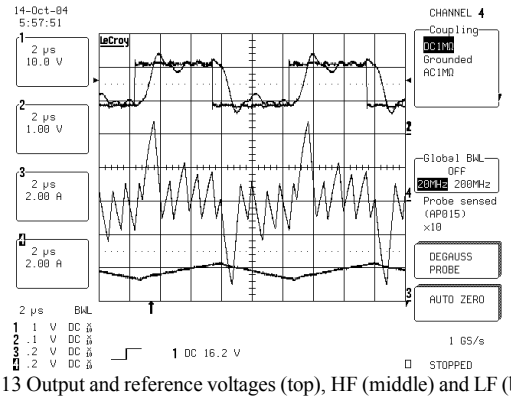

Figure 13 Output and reference voltages (top), HF (middle) and LF (bottom) buck inductor current, conditions as in Figure 12.

The unloaded step response is shown in Figure 14. A small overshoot occurs as predicted by simulation.

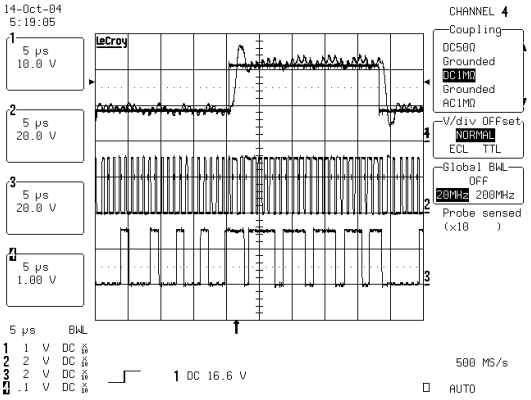

Figure 14 Output and reference voltages (top), HF (middle) and LF (bottom) buck PWM output voltages. Converter driving 20kHz 12Vpp+15VDC square into open load.

The long-term response of the inductor currents to an output voltage step is shown in Figure 15. This measurement clearly illustrates that the slow converter operates to its maximum capability during transients, and thus that the fast converter delivers an absolute minimum fraction of the load current. The absence of DC current in L_2 is also apparent.

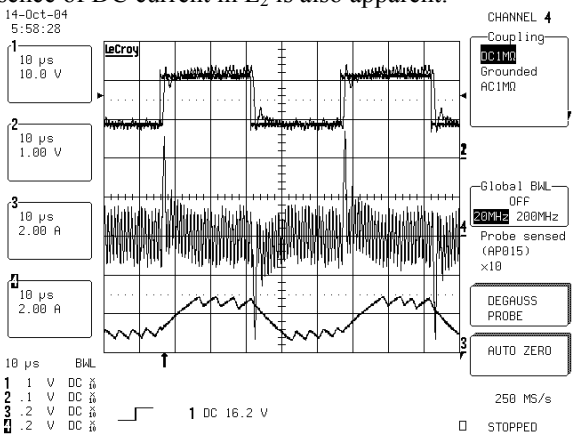

Figure 15 Output and reference voltages (top), HF (middle) and LF (bottom) buck inductor current. Converter driving 20kHz 12Vpp+15VDC square into 8Ω.

A power loss estimation model for the paralleled buck converters has been implemented in MATLAB. Figure 16 shows a comparison between estimated and measured efficiency for a constant output voltage. A high-speed oscilloscope with current probes is used for input/output power measurement since there is significant ripple, especially on output voltage. Oscilloscope measurement errors (measurement resolution is 8 bits) should account for some of the deviation between calculated and measured efficiency.

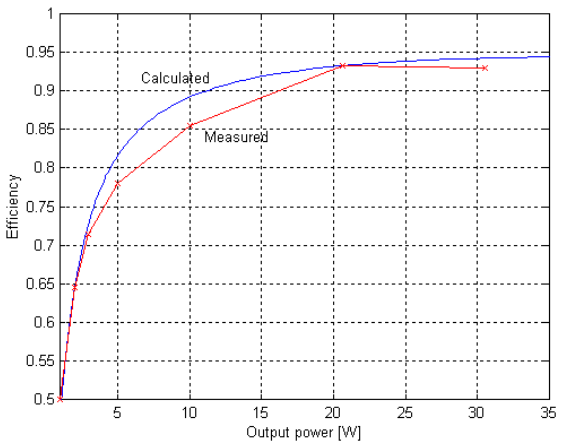

Figure 16 Calculated and measured efficiency figures for stationary 15VDC output voltage.

VII. CONCLUSION

A power conversion and control scheme for power supplies requiring high slew-rate and high efficiency has been presented. The power conversion scheme has been compared to a simpler solution, thereby justifying the proposed, more complex, solution. Comparison with a 2-phase buck solution has proven a complicated task, at least requiring complete loss calculation models for both topologies. However, simple initial considerations show that the proposed topology probably can perform at least as well as the more common 2-phase buck topology.

A fully operational prototype has demonstrated high efficiency, considering the bandwidth and slew-rate provided. The high efficiency naturally results from the use of a highly efficient low-bandwidth converter unloading the high-bandwidth converter in parallel, allowing reduced switching losses in the high-bandwidth converter.

For the control part, operation has been explained by linear modeling, and verified both through simulation and experimental work.

The results presented in this paper are currently state-of-the-art within the field of high-bandwidth power supplies with paralleled switching power conversion.

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