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Characterization and Evaluation of 600 V Range Devices for Active Power Factor Correction in Boundary and Continuous Conduction Modes

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***Abstract*—Traditional characterization of semiconductors switching dynamics is performed based on clamped inductive load measurements using the double pulse tester (DPT) configuration. This approach is valid for converters operating in continuous conduction mode (CCM), however in boundary conduction mode (BCM), if valley switching detection is used, the amount of energy recovered from the semiconductor output capacitance and the converter switching frequency need to be accurately calculated. This paper presents a characterization and evaluation procedure for conventional power factor correction circuits operating in CCM and BCM.**

Keywords—Power Factor Correction; Continuous; Boundary; Characterization; Evaluation.

I. INTRODUCTION

New semiconductor technologies, has made traditional converter operation modes to become obsolete for high switching frequency/high power density converters design. Traditional active power factor correction (PFC) circuits are based on a conventional boost converter, where the average input inductor current is controlled to achieve close to unity power factor. In high power applications continuous conduction mode (CCM) is the most used operation mode because of the reduced current stress. However, at lower power levels boundary conduction mode (BCM) is often preferred due to its low control complexity, not requiring converter input current sensing. The MOSFET on time is kept constant over the grid line period achieving an inherent proportionality between the converter input voltage and input current [1]. Power factor correction converters operating in BCM operate at the boundary between continuous and discontinuous conduction mode (DCM) [1], [2].producing the converter switching frequency to vary across the line cycle. This operation mode allows increasing the converter switching frequency due to the reduced switching losses with zero current switching (ZCS) operation at turn on. Moreover, zero voltage switching (ZVS) can also be achieved if a valley switching detection control scheme is used. The aim of this work is to compare state-of-the-art 600 V range devices performance by following a characterization procedure that can be used for both CCM and BCM. This paper presents a comparison and evaluation method based on a model for accurate prediction of the converter switching waveforms with special focus on the switching frequency prediction during BCM operation.

II. CHARACTERIZATION AND EVALUATION PROCEDURE

The characterization procedure is based on a double pulse tester (DPT) measurement. This circuit is the traditional clamped inductive load test set-up shown in Fig. 1. The device under test (DUT) is evaluated by building up some current in the inductor L, by keeping the device on for a controlled amount of time. When the required current level across the inductor has been reached, the DUT is turned off and on again, and the switching energy can be evaluated by integrating the V_{DS} times I_{DS} of the device. By repeating this procedure for different current levels, it is possible to create a set of data containing the switch-diode pair energy loss as a function of the current level.

In order to evaluate the performance of the evaluated devices, in this work a conventional boost based active power factor correction circuit as shown in Fig. 2 has been used. When the converter operates in CCM, the converter inner current loop adjusts the MOSFET on time to achieve unity power factor. Most of the time the inductor current is in CCM, however, as the converter approaches the zero crossings of the rectified input voltage waveform, the inductor current enters DCM operation. The necessary MOSFET on time can be calculated [3] as presented in (1) and (2) for CCM for DCM operation, respectively. The parameter M is defined as the dc voltage ratio as shown in (3), where V_{in} is the instantaneous converter input voltage. The value K is calculated as shown in (4). The

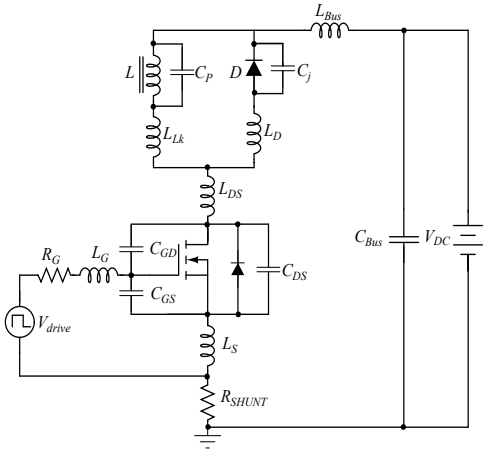

Fig. 1. Double pulse tester DPT schematic with parasitic components

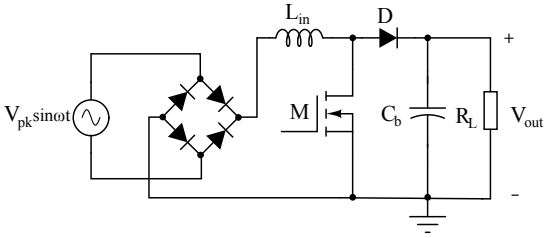

Fig. 2. Boost single phase PFC converter schematic

transition between CCM and DCM can be found as in (5). Finally, the inductor discharge interval can be found as presented in (6) and (7) for continuous and discontinuous conduction modes, respectively. Fig 3 shows the piecewise linear inductor current definition for discontinuous conduction mode. By using this definition, it is possible to find the converter currents across a half line cycle to calculate the semiconductor conduction losses, and interpolate the switching losses from the obtained DPT characterization data.

$$D_{CCM} = \frac{(M-1)}{M} \tag{1}$$

$$D_{DCM} = \sqrt{K \cdot M \cdot (M-1)} \tag{2}$$

$$M = \frac{V_{out}}{V_{in}} \tag{3}$$

$$K = \frac{2L_{in} \cdot T_s}{R_L} \tag{4}$$

$$I_{in} \leq \frac{D_{CCM} T_s V_{in}}{2L_{in}} \tag{5}$$

$$D_2 = 1 - D_{DCM} \tag{6}$$

$$D_2 = \frac{K \cdot M}{D_{DCM}} \tag{7}$$

The converter operating conditions in BCM are more difficult to calculate. The converter switching frequency varies across the line cycle. According to [4] the converter switching frequency can be calculated as shown in (8). This approximation is made based on the assumption the inductor waveform is a triangular waveform with peak values ranging from zero amps to twice the converter input average current. Based on this assumption and knowing the instantaneous converter conditions and the inductance value, it is possible to calculate the converter switching frequency across the line cycle.

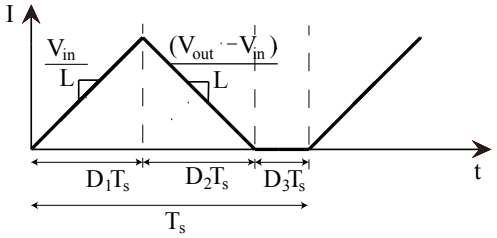

Fig. 3. Boost DCM inductor current waveform

$$f_{sw} = \frac{\left(V_{pk}/\sqrt{2}\right)^2 \left(V_{out} V_{pk} \sin \omega t\right)}{2LP_{out} V_{out}} \tag{8}$$

However, this prediction of the switching frequency has some limitations. Most of the converters operating in BCM or transition mode, make use of the valley switching operation [5], [6], [7]. This operation mode detects in different ways the inductor zero crossing current condition after the diode becomes reversed biased. When the current reaches zero, the MOSFET output capacitance resonates with the input inductor, making it possible to recover part of the energy stored on the device parasitic capacitance. The inductor current can be defined again using the current waveform presented in Fig. 4, where the period t_{valley} represents the valley switching period. The presence of this resonant period produces a mismatch on the calculated switching frequency. This mismatch becomes more evident as the resonant part of the inductor current increases with respect to the amount of power being transferred to the output. Fig. 5 shows a PFC converter operating in BCM mode. The converter is implemented using a $650\,V$ superjunction switch with a silicon carbide (SiC) diode. The converter switching frequency is $f_{sw} = 480\,kHz$. It can be observed that the valley switching subinterval uses a considerable part of the converter switching period. Moreover, in this case, the characteristic capacitance present in the vertical structure in superjunction devices produces a large time delay, since the MOSFET gate is turned off until the drain to source voltage rises to the final value. Therefore, using (8) will produce inaccurate estimation of the converter switching frequency under these conditions.

In this work, both the valley resonant period and the switch drain voltage rise time are considered in order to obtain a more accurate prediction of the converter switching frequency. The current and voltage during these periods are calculated using (9) and (10), respectively where I_c and V_c are the capacitor current and voltage. The non-linear capacitance voltage dependence is considered by interpolating from the manufacturer datasheet values, although curve fitting is also possible as previously presented in the literature [8], [9].

$$I_c(t) = I_c(0)\cos(\omega_0 t) + \frac{V_c(0) - V_{in}}{L\omega_0}\sin(\omega_0 t) \tag{9}$$

$$V_c(t) = (V_c(0) - V_{in})\cos(\omega_0 t) + \frac{I_c(0)}{C\omega_0}\sin(\omega_0 t) \tag{10}$$

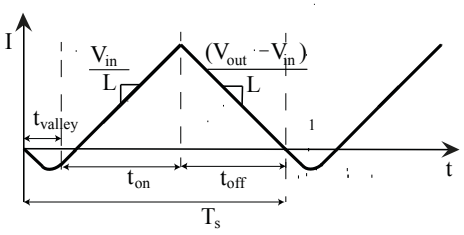

Fig. 4. Boost BCM inductor current waveform

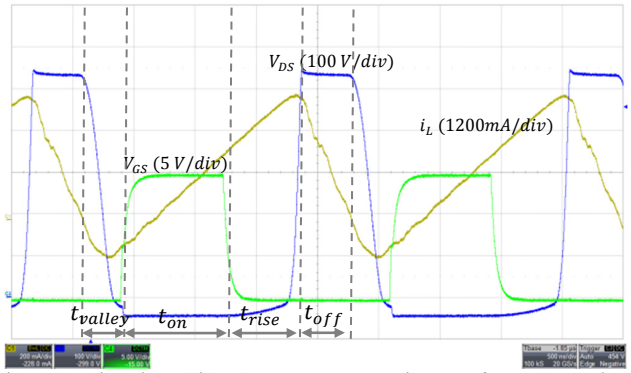

Fig. 5. Superjunction + SiC BCM converter operating waveforms. Gate voltage waveform (green 5V/div), drain voltage waveform (blue 100V/div) and inductor current waveform (yellow 200mA/div). Time scale: 500ns/div.

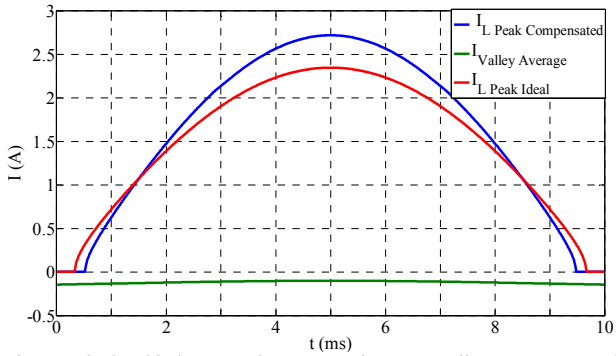

Fig. 6. Calculated inductor peak current and average valley current across half line cycle

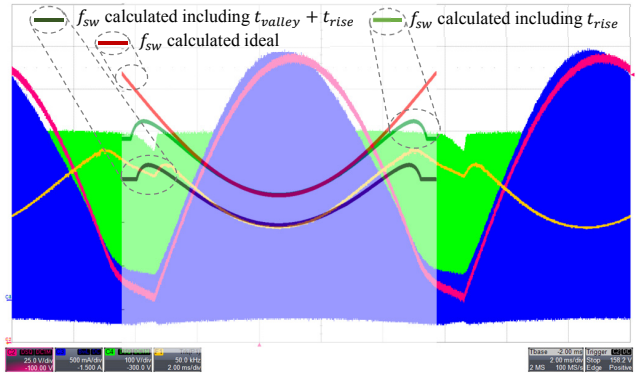

Fig. 7. Measured operating waveforms for a PFC boost converter. Drain to source voltage waveform (green 100 V/div), input voltage waveform (red 25 V/div, inductor current waveform (blue 500 mA/div) and switching frequency (yellow 50 kHz/div). Time scale: 2ms/div.

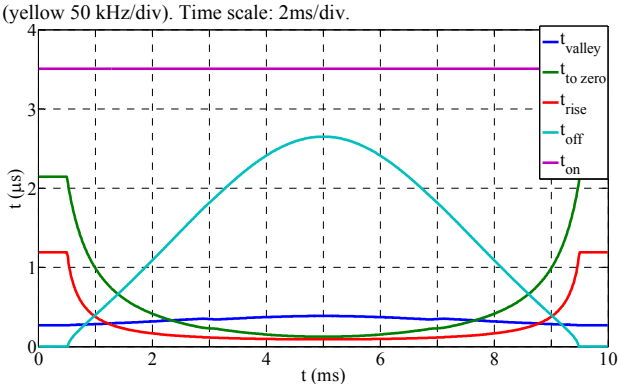

Fig. 8. Calculated BCM subintervals duration across half line cycle

Fig. 6 shows the calculated inductor peak current across half line cycle for the ideal case (red trace) where the peak value is equal to twice the required average input current. The green trace shows the average valley switching negative current. This portion of negative current increases the required switch on time in order to transfer the required amount of power to the converter load. Blue trace shows the effect of the negative valley current on the peak inductor current. Fig. 7 shows the measured converter waveforms and switching frequency for the conditions shown in Table I. The PFC controller operates with valley switching detection based on differentiation of the inductor voltage at the switch turn off. Superimposed with the measurement, the calculated switching frequency can be compared to the measured converter switching frequency. The red calculated trace corresponds to the ideal switching frequency calculated using (8). The green trace shows the effect of the MOSFET output capacitance charge at turn off. This effect becomes evident towards the input voltage zero crossings. Under these conditions, the fixed switch on time of the voltage control loop builds a small amount of current in the input inductor (due to the low instantaneous V_{in} value) creating a delay at the MOSFET turn off. The dark green trace includes the effect of the negative current flow created by the valley switching operation. As it can be observed, the switching frequency deviation becomes very significant across the whole line cycle. This calculation also includes the input decoupling capacitor effect on the converter switching frequency. As the operation approaches the zero voltage crossings of the rectified input voltage waveform, the positive current build up in the inductor is not enough to charge the MOSFET output capacitance up to the converter output voltage value, and the converter stops transferring power to the output. In this model it is considered that the converter input voltage remains constant at this value until the grid voltage is higher than the input capacitor voltage in the next cycle. However, as can be seen in Fig. 7, close to the input voltage zero crossings, the MOSFET drain voltage (green trace) and the input capacitor voltage (red trace) decrease due to the effect of the converter power losses. Fig. 8 presents the calculated subinterval times across the line cycle for the operating conditions shown in Fig. 7. As it can be seen, the MOSFET on time is considered to be constant across the cycle, but the off time decreases towards the input voltage zero crossings, which in the ideal case would create a switching frequency variation from the minimum switching frequency (11) to the maximum (12). However, as the operation approaches the zero crossings, the time the MOSFET drain to source voltage takes to rise (t_{rise}) and the time the inductor current takes to return to zero after the valley

TABLE I
SYSTEM SPECIFICATIONS AND COMPONENTS

Input voltage	$V_{in} = 120\ V_{rms}$
Output voltage	$V_{out} = 387\ V$
Output power	$P_{out} = 100\ W$
Input inductor	$P_{out} = 100\ W$
MOSFET	IPL65R130C7 650V superjunction Infineon
Diode	IDL10G65C5 SiC Infineon
Controller	FAN9612 BCM

$$f_{sw,min} = \frac{1}{(t_{on} + t_{off})} \quad (11)$$

$$f_{sw,max} = \frac{1}{t_{on}} \quad (12)$$

switching ($t_{to\,zero}$) increase, reducing the ideal converter switching frequency. The valley time subinterval remains almost constant during the whole cycle. The small deviation is caused by the differentiator action over the MOSFET drain to source dv/dt at the turn off. When the drain to source voltage starts decreasing, the differentiator will rise and decrease down to zero when the voltage derivative slows down close to the V_{DS} minimum to ensure valley switching or ZVS operation. In this case, the model is adjusted to start the MOSFET on time when the derivative slows down to 50 mV/ns.

III. Experimental Results

In order to perform the devices characterization, a low inductive DPT is used. The prototype is implemented using a four layer PCB taking special care to minimize the main ac current loop and driver current loop stray inductances while taking care not to unnecessarily increase the switching node stray capacitance. Moreover, a low capacitive inductor [10], [11], [12] and a minimum intrusive current measurement method [13], [14], [15] is employed in order to minimize the inserted inductance in the main switching loop. Fig. 9 shows the implemented DPT designed to accommodate 8x8 mm PQFN packages. In order to obtain more accurate switching energy measurements, the switching node (18 pF) and the oscilloscope probe capacitances (13.9 pF) are measured to be removed from the energy loss measurements. Fig. 10 and Fig. 11 present the measured switching energy loss for two superjunction devices in combination with a SiC diode. The characterization is performed at a rail voltage $V_{DC} = 400\ V$.The amount of energy corresponding to the switching node and the oscilloscope probe (2.55 μJ @ $400V$) has been removed from the turn on loss measurement. In this way, it is possible to observe that the turn on loss measurement at zero current level is between 3.6 μJ and 3.7 μJ. This value corresponds to the energy dissipated during the resistive charge of the diode parasitic junction capacitance. Therefore, the same amount of energy stored on this capacitance will be dissipated on the MOSFET channel during the MOSFET turn on. The measured value is in agreement with the manufacturer datasheet, which claims 3.5 μJ stored energy on the device output capacitance at $V_R = 400\ V$. Observing Fig. 11, it can be seen that at zero current conditions during the MOSFET turn off, the amount of measured energy corresponds to the energy stored on the MOSFET output capacitance which will be dissipated at turn on. The zero current values in this measurement have been extrapolated from the rest of the current points in the measurement, since it is impossible to measure a turn off event with zero current level. Both the superjunction measurements are in good agreement with the manufacturer datasheet specified energy. The 130 $m\Omega$ device presents a turn off loss at zero current level $E_{oss} = 4\ \mu J$ compared to $E_{oss} = 4.2\ \mu J$ specified in the component datasheet, while the 230 $m\Omega$ device presents $E_{oss} = 2.5\ \mu J$ compared to $E_{oss} = 2.62\ \mu J$.

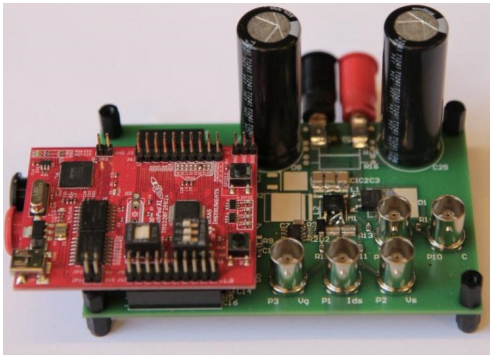

Fig. 9. Double pulse tester prototype

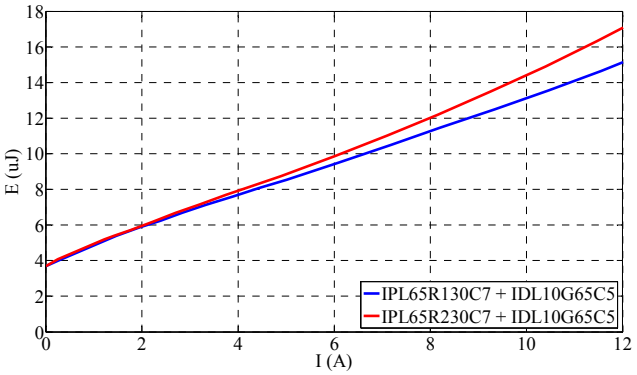

Fig. 10. Measured turn on energy loss

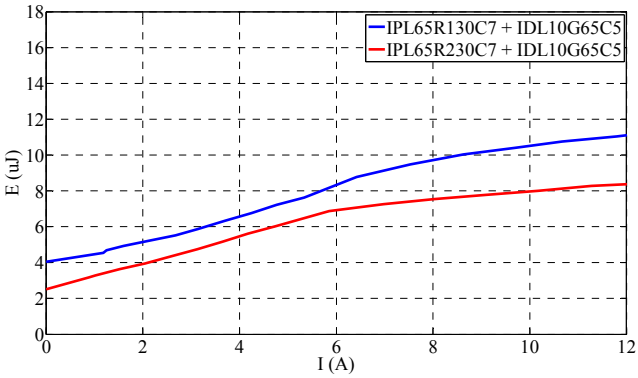

Fig. 11. Measured turn off energy loss

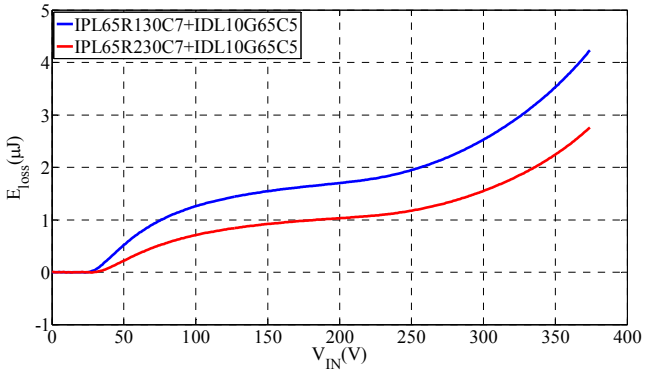

Fig. 12. Ideal capacitive loss at the switch turn on as a function of the converter input voltage

Fig. 12 shows the ideal amount of energy loss during valley switching operation of the converter. It can be seen that as the converter input voltage increases, the amount of recovered energy diminishes. On top of this energy loss, it has to be considered that the amount of energy delivered to charge the diode junction capacitance will be lost as resistive losses in the MOSFET channel. It is important to observe how the abrupt change in the superjunction MOSFET capacitance increases the turn on loss drastically even at low input voltage levels where the converter switching frequency will be higher. Moreover, most of the BCM controllers no matter if they are based on fixed delay time or differentiator will turn on the MOSFET when the capacitance abruptly changes and all the energy stored after this point will be lost. This will happen due to the fact that the capacitance change in the latest superjunction technology increases the value more than one order of magnitude. This fact produces the V_{ds} derivative to drastically slow down triggering the MOSFET turn on. In the same way, if a fixed delay time is used instead of a differentiator to decide the MOSFET turn on point in time, this delay time will be adjusted to catch the valley at higher V_{ds} voltages causing premature triggering at low input voltage levels.

IV. EVALUATION

By using the DPT characterization data, and the presented models for a PFC, is possible to compare the performance of the different evaluated devices. The amount of energy recovered prior to the MOSFET turn on in BCM needs to be removed from the characterization energy curves. In order to do so, the code developed for estimating the converter switching frequency also calculates energy stored on the devices output capacitances. On top of that, the conduction losses in the semiconductors are calculated including the resonant currents during valley switching operation. In order to simplify the calculation, the MOSFETs characteristic on resistance and diode threshold voltage and dynamic resistance specified @25℃ in the manufacturer datasheets are used. Fig. 13 and Fig.14 show a CCM and BCM semiconductor loss calculation breakdown for IPL65R230C7 in combination with a SiC diode IDL10G65C5. The converter operates with $V_{in} = 230\ V_{rms}$ and $P_{out} = 200\ W$ for an output voltage level $V_{out} = 390\ V$. Both BCM and CCM calculations are plotted versus the selected input inductor value. As it can be observed in CCM, the diode

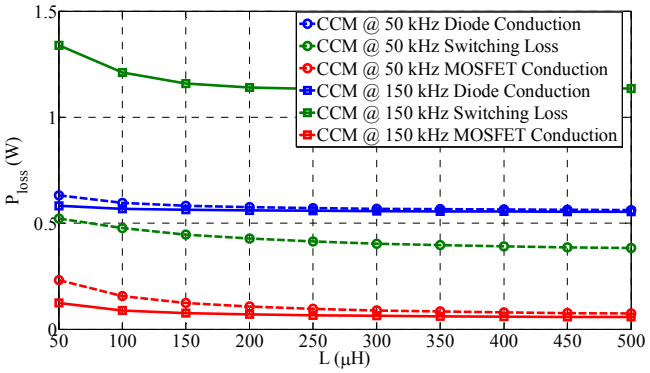

Fig. 13. Semiconductor power loss breakdown during CCM operation vs. input inductor value

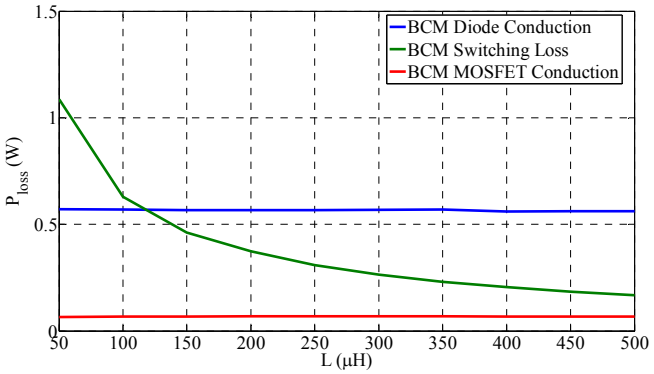

Fig. 14. Semiconductor power loss breakdown during BCM operation vs. input inductor value

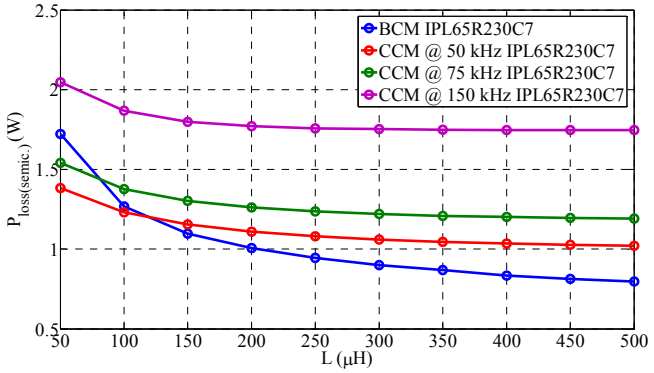

Fig. 15. Semiconductor power loss for IPL65R230C7 + IDL10G65C5 vs. input inductor value

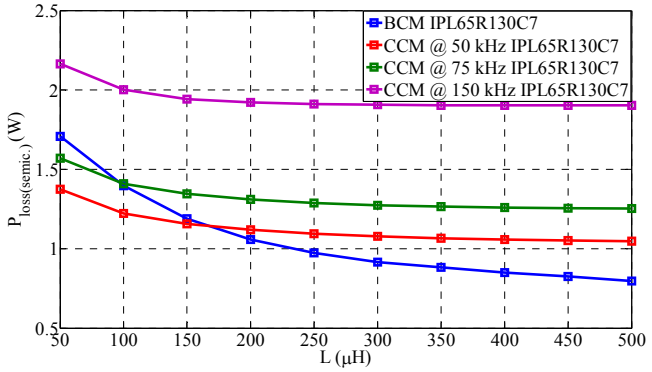

Fig. 16. Semiconductor power loss for IPL65R130C7 + IDL10G65C5 vs. input inductor value

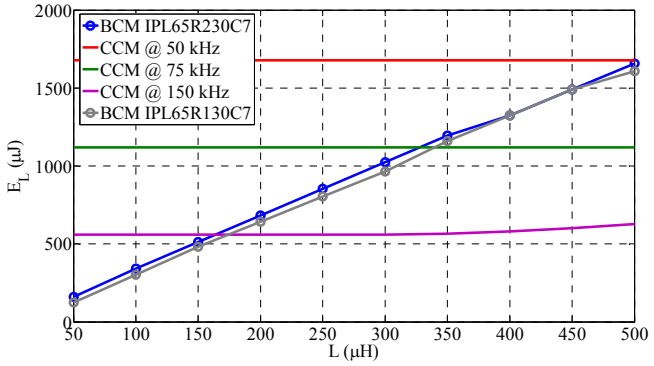

Fig. 17. Input inductor energy storage requirement vs. input inductance value for BCM and CCM operation

conduction loss is the predominant loss at low frequency levels. Increasing the input inductor value does not have a visible effect on this loss due to the fact that the main contribution to the loss in this component comes from the average current. It is only at very low inductance value where the rms component of the current has an effect on this loss. The MOSFET conduction loss at this power level and input voltage level contributes very little to the total final semiconductor loss. As the switching frequency and the inductance value increase, the MOSFET conduction loss diminishes due to the decreased rms component. The switching losses in CCM represent a large part of the total loss even at $f_{sw} = 50\ kHz$. Increasing the inductance value has a small effect on this loss due to the fact that the largest part of the loss at this voltage and power levels are capacitive losses. From Fig. 14, it seems clear that employing BCM operation mode will slightly increase the semiconductor conduction losses while reducing capacitive switching losses.

Fig. 15 and Fig.16 present a comparison of IPL65R230C7 and IPL65R130C7 in combination with the SiC diode IDL10G65C5 in CCM and BCM operating modes, while Fig. 17 present the input inductor energy storage requirement (13) which gives an estimation for comparison purposes of the input inductor size.

$$E_L = \frac{{I_{L,peak}}^2 L}{2} \tag{13}$$

From this comparison, it can be seen that when the input inductor value is around $L \approx 150\ \mu H$ the BCM operation presents equal or lower semiconductor losses than the CCM solutions @ $f_{sw} = 50\ kHz$ due to the capacitive switching loss reduction. Moreover, the input inductor size is reduced more than three times.

V. CONCLUSION

This paper presents an evaluation procedure to compare different PFC solutions operating in both CCM and BCM. The evaluation is based on DPT measurements combined with a detailed model for prediction of the converter switching frequency across the input line cycle. By combining these tools it is possible to predict the semiconductor performance and the attainable advantages that can be obtained in terms of power density/efficiency by inserting a new semiconductor technology.

This works presents a case study where two state-of-the-art Si MOSFETs C7 are evaluated with a G5 SiC diode in both modes. The obtained results show that the valley switching combined with the ZCS turn on present in this operation mode, overcomes the current stress increment and makes it possible to increase the converter switching frequencies attaining a large reduction on the converter magnetic storage requirement.

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