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MEMS Vertical Probe Cards With Ultra Densely Arrayed Metal Probes for Wafer-Level IC Testing

Fei Wang, Member, IEEE, Rong Cheng, and Xinxin Li

Abstract—We have developed a MEMS probe-card technology for wafer-level testing ICs with 1-D line-arrayed or 2-D area-arrayed dense pads layouts. With a novel metal MEMS fabrication technique, an area-arrayed tip matrix is realized with an ultra-dense tip pitch of 90 μm × 196 μm for testing 2-D pad layout, and a 50-μm minimum pitch is also achieved in line-arrayed probe cards for testing line-on-center or line-on-perimeter wafers. By using the anisotropic etching properties of single-crystalline silicon, novel oblique concave cavities are formed as electroplating moulds for the area-arrayed microprobes. With the micromachined cavity moulds, the probes are firstly electroplated in a silicon wafer and further flip-chip packaged onto a low-temperature cofired ceramic board for signal feeding to an automatic testing equipment. The micropores can be efficiently released using a silicon-loss technique with a lateral underneath etching. The measured material properties of the electroplated nickel and the Sn–Ag solder bump are promising for IC testing applications. Mechanical tests have verified that the microprobes can withstand a 65-mN probing force, while the tip displacement is 25 μm, and can reliably work for more than 100,000 touchdowns. The electric test shows that the probe array can provide a low contact resistance of below 1 Ω, while the current leakage is only 150 pA at 3.3 V for adjacent probes.

Index Terms—Dense-arrayed vertical tips, electroplating, IC testing, micromachining, probe card.

I. INTRODUCTION

WAFER-LEVEL IC testing has been an integral part of the IC manufacturing processes for over four decades [1]. Yet, its significance has only just been properly regarded with the recent dazzling development of microelectronic packaging technologies. Advanced concepts, such as multichip module, system-on-chip, system-in-package, and system-on-package, will eventually change electronic products into “convergent systems” that consist of computation, communication, consumer, and even biomedical functions [2]. This revolution-
a stiffer structure and can withstand a much larger probing force [7]–[10]. The cantilever probes can be densely arrayed in one direction and feature fine tip pitch less than 100 μm. Unfortunately, the cantilever structure usually takes more than hundreds of micrometers to 1 mm in the perpendicular direction to the tip array. Thus, they are only suitable for testing conventional in-line devices, such as memory devices in which testing pads are simply line-arrayed with the perimeter or line-on-center (LOC) configuration. Recently, 1- and 2-D arrayed pad layouts have been widely used in advanced devices, such as LCD-driver ICs and the wafers with pad redistribution, since IBM developed the controlled collapse chip connection (C4) process [11]. Many microspring structures have been fabricated with electroplating techniques for various applications, such as a measurement system for contacts [14], small-pitch flip-chip packaging [15], and a platform for high-frequency testing [16]. Based on multilayer electroplating techniques, a microspring probe card has been recently developed for C4 design [12]. Unfortunately, the fabrication demands a fussy process of five to seven separate electroplating steps that is not easily implemented. Moreover, the probes exhibit a spatial tip pitch, and it is difficult to test the device with the pitch less than 200 μm.

In this paper, we present a new type of MEMS probe card, in which both highly dense line-arrayed and area-arrayed nickel tips can be fabricated simultaneously in a same wafer. With a novel oblique silicon cavity mould by a unique etching technique, the nickel microprobes are, for the first time, electroplated on an inclined surface and further flip-chip bonded to a low-temperature cofired ceramic (LTCC) substrate via Sn–Ag solder bumps. Then, the probes can be high-yield released with a silicon-loss technique. With this method, the vertical metal probes can be densely arrayed in two dimensions. The detailed technique is described in the following sections.

II. DESIGN AND SIMULATION

The authors previously developed a MEMS probe card with “hoe”-shaped metal tips [17]. As shown in Fig. 1(a), the microprobe has a large footprint and features a 2-D tip pitch of 240 μm × 160 μm. The tip pitch is still larger than that demanded in many dense-pad IC testing applications. In this paper, we propose a much more compact structure that can be easily arrayed in either 1-D line or 2-D area. The top-view schematic is shown in Fig. 1(b). When the nickel electroplating is performed within a regular silicon anisotropic etching formed cavity, the “face-to-face” probe design can shrink the two-row or one-row line-arrayed tip pitch down to 35 μm. This type of probe card can be used for testing LOC devices or the multi-DUT testing. As for the dies with area-arrayed pads, densely 2-D arrayed microprobes will be formed with a novel oblique-cavity mould etching technique. As schematically shown in Fig. 1(c), the “face-to-face” two-row layout can be changed to a “one-after-one” design. The tip pitch of the former “face-to-face” design used two inclined walls from anisotropic etching. In contrast, the tip pitch in the “one-after-one” design can be much compressed, because the etched silicon cavity only contains one inclined sidewall for probe electroplating. It can be seen clearly from Fig. 1 that the area-arrayed tip pitch can be further shrunk to 90 μm × 196 μm for ultradense 2-D pad layout. By using this novel area-arrayed technique and the line-arrayed one, probe cards with various tip-array layouts can be realized with the vertical metal probe fabrication techniques for testing various types of DUT.

The 3-D views in Fig. 2 show the designed structure of the microprobe arrays. Both the line-arrayed and the area-arrayed probe cards are fabricated using similar processes. The vertical microprobes are first selectively electroplated in silicon cavity moulds that were previously formed by anisotropic etching in a silicon wafer and then flip-chip bonded to an LTCC board for backside I/O interconnection with ATE. Compared with conventional probe cards where postpackaging or assembly was used [13], the flip-chip bonding technique is a more efficient method to simultaneously transfer the thousands of micro-probes. The LTCC board provides a rigid substrate for the probe cards, which can withstand a total force of about 1–10 kg, since the contact force of each microprobe can be around 1–10 g. More importantly, the LTCC board and the silicon IC wafer have close values for coefficient of thermal expansion (CTE) that guarantees a small mismatch between the probe tips and the pads under test, even when used in a high-temperature burn-in test. Table I shows the comparison in CTE among silicon and other materials possibly used for probe-card substrate [18].

During wafer-level testing, the probe tips are forced to contact with the pads of the DUT and have to withstand a typical probing force of about 10 mN to achieve a low contact resistance between the tip and the pad. Meanwhile, the
obliquely up-tilted probe tip should also bend with an overdrive of about 10 μm to adapt to the pad’s nonuniformity across the DUT. In addition, the maximum stress in the microprobe body should be within the yield strength limitation of the electroplated nickel. To make efficient use of the space and secure mechanical reliability, the probe is designed into a stress-equal structure. In the stress-equal beam, the width of the microprobe linearly shrinks from the clamped root to the free end to secure that the normal stress caused by the probing force is not changed [17]. With this design, the probing-forced driven tip displacement can be improved by about 50%, compared with the conventional width-equal cantilever. Finite element method is applied to analyze and optimize the mechanical properties of the nickel cantilever. The Young’s modulus and Poisson ratio for the electroplated nickel used in the simulation are 170 GPa and 0.3, respectively. The structure parameters and ANSYS simulated results for three sets of probe cards are listed in Table II. Fig. 3(a) shows the ANSYS simulated tip displacement under a probing force of 20 mN. In Fig. 3(b), the equal-stress beam shows a uniform stress distribution from the root to the tip apex. All the design considerations allow for a large tip overdrive while keeping the stress safely lower than the rupture limitation of the material.

III. Fabrication

The fabrication starts on a 450-μm-thick (100)-oriented n-type silicon wafer. The detailed process steps are sketched in Fig. 4 and described as follows.

1) First, 1-μm-thick SiO₂ is thermally grown and patterned as the mask for the following anisotropic etching. The opening width of the mask will determine the etching depth of the cavities.

2) To obtain the oblique concave cavities, narrow trenches are formed by photoresist coating, patterning, and deep reactive ion etching (DRIE). As shown in the cross-sectional view of Fig. 5, the critical relationship between the opening width of the mask and the etching depth of the trench is

\[ H = \sqrt{2L} \]

3) Then, with the SiO₂ layer as etching mask, anisotropic etching with aqueous KOH (40 wt.%, 60 °C) is carried out subsequently to form the cavities that will be used as moulds for electroplating in the following process step. A regular anisotropic etching formed cavity, with two “face-to-face” {111} incline sidewalls, is formed at the regions without the narrow trenches for the 1-D line-arrayed microprobes. As for the 2-D area-arrayed microprobe regions, the DRIE-formed narrow trenches will help to shape the oblique cavities by fully using the anisotropic etching properties of single-crystalline silicon. For the right {110} vertical sidewall in Fig. 5, it would eventually stop at two concave {111} planes. The final profile for the left {110} vertical sidewall is determined by the relationship between the opening width of the SiO₂ mask (L) and the depth of the DRIE-formed narrow trench (H).

When \( H > \sqrt{2L} \), the etching front evolution process is shown as in Fig. 6. First, the top {100} surface is etched downward. In the mean time, the {110} vertical sidewalls are etched horizontally. When the two planes meet, the {100} surface will be stopped and merged at the inclined {111} plane, leaving a remained segment of the vertical {110} wall, as shown in Fig. 6(c). Then, the etching at the left-side vertical wall will keep on going until it finally stopped by the two concave {111} planes. Such a situation should be avoided since the following

![Fig. 2. Three-dimensional view of (a) the densely area-arrayed and (b) line-arrayed microprobes. The microprobes are fabricated by using nickel electroplating, flip-chip bonding to an LTCC board for further I/O interconnection via Sn–Ag solder bumps.](image-url)

Table I

<table>
<thead>
<tr>
<th>Material</th>
<th>CTE (ppm/°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon wafer</td>
<td>2.5–3.2</td>
</tr>
<tr>
<td>Epoxi</td>
<td>25–65</td>
</tr>
<tr>
<td>PCB (FR4)</td>
<td>13–18</td>
</tr>
<tr>
<td>PCB (pimide)</td>
<td>12–16</td>
</tr>
<tr>
<td>Ceramic</td>
<td>5–9.3</td>
</tr>
<tr>
<td>LTCC</td>
<td>3.4–6.5</td>
</tr>
</tbody>
</table>

Table II

<table>
<thead>
<tr>
<th>Structure Parameters and ANSYS Simulated Results for the Designed Three Types of Microprobes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter</td>
</tr>
<tr>
<td>---------------------</td>
</tr>
<tr>
<td>Probing height (μm)</td>
</tr>
<tr>
<td>Width b (μm)</td>
</tr>
<tr>
<td>Thickness t (μm)</td>
</tr>
<tr>
<td>Loading F (mN)</td>
</tr>
<tr>
<td>Displacement δ(μm)</td>
</tr>
<tr>
<td>Spring constant k (N/m)</td>
</tr>
<tr>
<td>Maximum stress T (GPa)</td>
</tr>
</tbody>
</table>
Fig. 3. ANSYS simulation results. (a) Equal-stress beam design is used to increase the tip displacement under a certain probing force. (b) Equal-stress beam shows a uniform stress distribution from the root to the tip apex.

Fig. 4. Fabrication processes for the dense-arrayed metal vertical probe card. (a) SiO₂ mask is patterned. (b) Trenches are formed using DRIE. (c) Anisotropic wet etching. (d) Photoresist is patterned for following electroplating. (e) Nickel electroplating. (f) Remove the photoresist and strip away the TiW/Cu seed layer between adjacent probes (with diluted H₂SO₄) for electric isolation. (g) Solder bumps are electroplated and reflowed on an LTCC board. (h) Flip-chip bonding. (i) Silicon wafer is peeled off, and the probes are finally released.

Fig. 5. Anisotropic silicon wet etching scheme for the oblique silicon cavity, with narrow trenches for finally shaping the area-arrayed metal probes.

sputtered and electroplated metal layer would be broken at this concave-angle region.

When \( H < \sqrt{2}L \), the etching evolution is shown as in Fig. 7. At first, the horizontal \{100\} surface and the vertical \{110\} sidewall will be etched separately. When the two planes meet, the vertical \{110\} sidewall will be stopped and merged at the inclined \{111\} plane, leaving a horizontal \{100\} surface segment. Now, a convex corner is exposed, and thus, the \{100\} surface segment will be replaced soon by a \{311\} fast etching plane because of the much faster etch rate of the \{311\} plane than the \{100\} plane. Finally, the \{311\} plane will also be merged at the \{111\} inclined plane, with a slight bottom remainder \( \delta \).
Fig. 7. Anisotropic etching evolution process under the condition of deficient DRIE depth ($H < \sqrt{2}L$).

and the remainder can be estimated by the following equation:

$$\delta = \frac{1}{2} \left( L - \frac{H}{\sqrt{2}} \right).$$

The DRIE tolerance usually causes a depth error that is no larger than 5 $\mu$m. Accordingly, the remainder will not exceed 1.7 $\mu$m and will not largely affect the fabrication process. Therefore, during the DRIE process for the narrow trenches, the etching depth should be controlled as $H \leq \sqrt{2}L$. The SEM image in Fig. 8 shows the final etched profile of the inclined silicon cavity mould for following metal electroplating.

4) After the silicon cavities are etched, a seed layer of TiW/Cu is deposited on the silicon surface, including the inclined walls of the etched cavities. The 200-nm-thick Cu film serves as the electric layer for nickel plating, and the 100-nm-thick TiW is deposited beneath the Cu layer for improving the adhesion between Cu and the substrate. Then, a 12-$\mu$m-thick photoresist layer is spray coated by using an EVG101 system (EV Group, Austria) [19] and then patterned to form the electroplating moulds.

5) The 10-$\mu$m-thick nickel microprobes are electroplated on the 54.74°-inclined (111) sidewall. To achieve a low-stress nickel layer, a sulphamate solution is prepared and a periodic reverse plating technique is used. The electroplating solution is mainly composed of nickel sulphamate (Ni(SO$_3$NH$_2$)$_2$ · 4H$_2$O, 500 g/L), boric acid (H$_3$BO$_3$, 40 g/L), nickel chloride (NiCl$_2$ · 6H$_2$O, 10 g/L), and some addictives, including butylenediol and saccharin. The pH value and the temperature of the solution are controlled as 4.0 and 40 °C, respectively.

6) After all the photoresist is stripped away, the exposed TiW/Cu seed layer is removed successively. So far, the microprobe structures are formed on the silicon wafer, as shown in Fig. 9.

7) On an LTCC board, TiW/Cu (50 nm/500 nm) is sputtered and coated with a thick photosresist (AZ9260, Clariant) layer. After the photoresist is patterned, 30-$\mu$m-thick Sn–Ag solder bumps are electroplated within the photoresist mould by using a Slotoloy SNA30 solution (Schloetter Plating Inc.). The plating temperature and the current density are controlled as 25 °C and 20 mA/cm$^2$, respectively, resulting in a deposition rate of about 3–4 $\mu$m/min. Then, the TiW/Cu signal lines are patterned using the photoresist spray-coating technique. Then, the solder bumps are reflowed with a five-zone reflow oven (Falcon 8500). All the five reflow zones are filled with N$_2$ gas, and the temperatures of the five zones are set as 100 °C, 150 °C, 220 °C, 260 °C, and 80 °C, respectively [20], [21]. The Sn–Ag solder bumps manifest their fabrication details in Fig. 10.

8) The plated nickel probes on the silicon wafer are aligned and bonded to the LTCC board with a standard flip-chip process that comprises fluxing, placement, reflow, and curing [22].

9) Then, the silicon substrate is peeled off using the lateral underneath etching effect of TMAH anisotropic wet etch (75 °C, 25 wt.%). After the silicon substrate is lost, the vertical probes are finally free standing.

The SEM images in Fig. 11 show the free-standing vertical area-arrayed microprobes with ultradense tip pitch of 90 $\mu$m × 196 $\mu$m, with a close-up inset showing the details of the nickel probe bonded with the LTCC board via Sn–Ag solder bumps. Fig. 12 shows a digital photograph of the fabricated probe-card prototype packaged on an LTCC board for interconnecting with I/O interface of ATE. The close-up SEM inset illustrates the high uniformity of the densely area-arrayed microprobes.

IV. CHARACTERIZATION

The developed probe cards are characterized by testing a set of mechanical and electrical parameters. The tested parameters include contact force, overdrive, tip planarity, contact...
resistance, signal path resistance, and leakage current. The detailed characterization is given in the following sections.

A. Material Properties

1) Electroplated Nickel: The material properties of the electroplated nickel are characterized using a Nano-indenter XP system, which has been accepted as the most common method for testing Young's modulus and hardness [10], [23]. The measured Young's modulus and Vickers hardness of the electroplated nickel are 116 GPa and 420, respectively. The Young's modulus is slightly lower than 125 GPa, which was reported from the bending test in [24]. The measured Vickers hardness in this paper is a little higher than the previously reported value of 400. The high hardness of the electroplated nickel can help the probe tip to scratch the natural oxide on the Al pad surface to enable a lower electrical contact resistance. High hardness also helps lead to a high life expectancy of the probes.

2) Sn–Ag Solder Bump: The Sn–Ag solder bumps are the mechanical and electrical interconnects between the nickel microprobes and the LTCC board. Therefore, both the mechanical and electrical properties of the Sn–Ag solder bumps are characterized in this paper. Shear test for the solder bumps is performed to evaluate the bonding strength between the nickel microprobe and the LTCC board with a Dage-4000 shear tester. The inset image in Fig. 13 shows the schematic of the shear strength test. A total of about 300 bonded probes are tested, resulting in a Gaussian distribution. Most of the solder bumps show about 60-gf shear force when the test speed is 600 μm/s and the shear height is 20 μm. The tested results demonstrate that the fabricated microprobes can be used under a large scratching force of hundreds of millinewtons.
A series-resistance testing scheme is designed to measure the electrical resistance of the Sn–Ag solder bumps. The testing scheme has been described in detail in [17]. When a constant current source of 20 mA is applied through the series of solder bumps, the resistance can be read by detecting the output voltage. The measured series resistance is never higher than 1.8 Ω for 30 pairs of bumps in series, which means that the interconnect resistance for one solder bump is generally lower than 0.03 Ω.

B. Mechanical Characterizations

1) Spring Constant of the Probe: The spring constant of the probe is measured by a force–displacement tester, which is built to measure the contact force versus tip displacement for the microprobes [17]. As schematically shown in Fig. 14(a), when the piezoelectric ceramic actuates the testing needle to contact with the probe tip, the contact force can be monitored and read with an electric balance, while the tip displacement is in proportion to the applied voltage. In this way, the loading-displacement curves are obtained and shown in Fig. 14(b). All the three types of probe cards with different spring constants have been tested, resulting in a good agreement with the designed results. The difference between design and test is generally smaller than 7%. The micrographs in Fig. 14(c) and (d) show the microprobe before and after the loading force is applied, respectively.

When a pulsed voltage is applied to the piezoelectric actuator, the testing needle would vibrate up and down. The reliability of the probes could then be evaluated with many touchdowns. In our experiment, the probes were able to reliably survive more than 100,000 repeated cycles of loading contact. Inspected with microscopy and SEM, most of the microprobes appear unchanged after the 100,000 touchdowns. However, about 5% of the probes show a little bit of wear at the tip. The SEM images shown in Fig. 14(e) and (f) are the worst case among the microprobes in our lifetime test and its close-up view at the tip. Some wear is apparent for this probe.

2) Tip Planarity and Scrub Mark: The tip planarity of the probe card is evaluated by optically scanning the probe tips using a WYKO NT-2000 optical metrology system (Veeco Instruments Co. Ltd.) that provides noncontact high-resolution 3-D profile measurement. The testing results show that, within a 10 by 10 probe array, the nonuniformity in the tip planarity is within ±4 μm, which is better than the previously reported data where a cantilever-tip probe structure is used [7]. A better uniformity could be obtained by better control of the solder-bump height variation and the bonding force during the flip-chip bonding.
tip pitch of 90 μm × 196 μm and 50 μm have been achieved for testing area-arrayed and line-arrayed pads, respectively. Satisfactory mechanical and electric properties have been obtained, and the probe cards show promise of testing next-generation ICs.

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The authors would like to thank X. Lin and Prof. L. Luo for their advice on flip-chip packaging and also K. Jiang, Prof. H. Yang, and X. Ge for their help with the device fabrication.

REFERENCES


V. CONCLUSION

A novel MEMS probe-card fabrication technique has been developed. Ultradense vertical metal tips are integrated in the probe card for the wafer-level testing of advanced ICs with various types of dense pad layout. By using a novel oblique concave cavity mould technique, microprobes with a minimum


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