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BLACK SILICON WITH TUNNEL OXIDE PASSIVATED CONTACTS

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ABSTRACT: We investigate surfaces of black silicon (bSi) fabricated by reactive ion etch (RIE) on n-type Si substrates and passivated by *in-situ* doped polycrystalline Si (poly-Si) deposited by low pressure chemical vapor deposition (LPCVD). We achieved full surface coverage of bSi surfaces for poly-Si thickness of 20 nm. We determined sheet resistance on p-type and n-type poly-Si by means of micro four-point probe measurements. Effective lifetime mapping on symmetrically passivated samples shows that n-type poly-Si offers excellent surface passivation after hydrogenation, reaching effective lifetime values of almost 4 ms on non-textured substrates. P-type poly-Si shows values of effective lifetime lower than 800 µs and requires further improvement. We calculated i-V_{oc} of up to 711 mV and 609 mV for asymmetrically passivated lifetime samples without texturing and with bSi, respectively. The effective lifetime is limited by the less-than-optimal passivation of the p-type poly-Si. Preliminary solar cell measurements indicate that both cell voltage and fill factor require major improvement on textured surfaces. Current work is directed towards the following goals: improving the quality of the p-type poly-Si; testing possible replacement of wet chemistry to grow the tunnel oxide using dry furnace oxidation; fabricating and comparing cells with p-n junction at the front or at the bottom of the cell.

1 INTRODUCTION

The tunnel oxide passivated contact (TOPCon) is a class of selective contacts that enables excellent charge carrier selectivity on crystalline Si. [1,2] It consists of an ultra-thin tunnel silicon oxide (SiO_2) layer in combination with a poly-Si layer, and it offers almost as high quality of surface passivation as its sister architecture HIT (heterojunction with intrinsic layer) based on hydrogenated amorphous Si (a-Si:H) [3], with the advantage of being compatible with high temperature processing (up to around 900 °C) [4]. Less-than-maximum short circuit current J_{SC} currently limits the power conversion efficiency of TOPCon solar cells. Black silicon (bSi) [5,6] has demonstrated great potential as texturing method for Si thanks to its excellent intrinsic antireflective properties [7]. Power conversion efficiencies between 18 and 22% have been achieved in the lab using laser-doped selective emitters [8] and interdigitated back contact (IBC) cells [9]. These results have been obtained using maskless reactive ion etch (RIE) for the Si texturing. Importantly, RIE works on any Si surface irrespective of the crystallinity and the method used for wafering, including diamond-wire. The increased surface recombination due to increased surface area and process-induced damage currently limits the open circuit voltage (V_{OC}) and thus the efficiency of RIE textured solar cells. TOPCon seems therefore an appropriate candidate to passivate a notoriously challenging surface such as RIE-textured Si. Here, we present our first attempt at combining RIE bSi with TOPCon passivation. We fabricated *in-situ* doped poly-Si layers by LPCVD, a method that offers higher compatibility with industrial production than commonly used ion implantation for doping. We demonstrate excellent passivation by n-type poly-Si, while further work is required to improve the passivation by p-type poly-Si and thus to obtain significant device efficiency.

2 EXPERIMENTAL DETAILS

2.1 *Fabrication*

100 mm n-type Czochralski (100) Si (350 µm thickness, 4 Ω cm resistivity, oxygen concentration < 11.5 ppa) from Okmetic were used as substrates. BSi texturing was performed by RIE in a SPTS Pegasus system with process temperature of -20 °C, process time of 14 min, SF_6 and O_2 plasma with 7:10 gas flow ratio, chamber pressure of 38 mTorr, 3 kW coil power and 10 W platen power. Wafers were then RCA cleaned and a tunnel silicon oxide with thickness of 1.5 nm was grown in 68 wt% HNO_3 at 95 °C for 10 min. *In-situ* doped poly-Si passivating contacts were deposited by LPCVD at 620 °C with SiH_4, B_2H_6 and PH_3 as precursors for Si, B and P respectively. Deposition time was varied in order to obtain nominal thickness ranging between 10 and 40 nm. All wafers where annealed in N_2 for 20 min at 850 °C. Symmetrical lifetime samples were prepared by depositing one poly-Si layer on both sides of the wafers during the same LPCVD run. Asymmetrically passivated wafers were prepared with the following steps: protection of the back side by depositing 300 nm of SiO_2 by plasma-enhanced CVD (PECVD, SPTS system); first tunnel-oxide/p-type poly-Si LPCVD run; RIE and wet etch in buffered HF solution to remove poly-Si and SiO_2 on the back side, respectively; protection of the front side by 300 nm PECVD SiO_2; second tunnel-oxide/n-type poly-Si LPCVD run; RIE (SPTS) and wet etch in buffered HF solution to remove poly-Si and SiO_2 on the front side, respectively; annealing of the poly-Si. Hydrogenation of lifetime samples was performed using the following steps: deposition of 75 nm SiN_x:H at 300 °C by PECVD; drive-in of hydrogen by annealing for 1 h at 400 °C in a tube furnace with N_2 atmosphere; removal of SiN_x:H by buffered HF. Solar cells with area of 6 cm^2 were fabricated from these asymmetrically passivated samples with following cross-section: front grid with 500 nm thick Al fingers/75 nm Al-doped zinc oxide (AZO)/15 nm p-type poly-Si/SiO_2/c-Si/SiO_2/40 nm n-type poly-Si/75 nm AZO/250 nm Al full back contact. Al was deposited by physical vapor deposition in a Temescal system. AZO was deposited by atomic layer deposition (ALD) at 200 °C in a Picosun system using Tetramethylammonium (TMA), Diethylzinc (DEZ) and water vapor as precursors for Al, Zn and O respectively.

2.2 *Characterization*

The thickness of the poly-Si was measured with a VASE ellipsometer on planar Si substrates. Cross-section scanning electron microscopy was performed in a Supra v40 SEM (Zeiss) at an accelerating voltage of 5 kV. Sheet resistance was measured on poly-Si layers using a micro-four point probe (µ4PP) CAPRES M300-tool with equidistant, straight 10 µm pitch micro four-point probes (M4PP). The n-type poly-Si was measured using 50 µA AC current at 13 Hz, using a punch-through current of 500 µA for 0.01 s. The p-type poly-Si was measured using 7 µA AC current at 13 Hz, using a punch-through current of 500 µA for 0.05 s. Minority carrier effective lifetime was measured on the full 100 mm area of the wafers using the microwave detected photoconductance method with a MDP mapper from Freiberg in steady-state configuration, with laser wavelength of 977 nm and photon flux of 4×10^{17} cm^{-2} s^{-1}. Current-voltage characteristics of solar cells were measured under 1 Sun using a solar simulator from Newport. Quantum efficiency and reflectance measurements were performed in a QEXL set-up equipped with an integrating sphere.

3 RESULTS

Figure 1 shows cross-section SEM images of bSi surfaces after deposition of poly-Si layers with nominal thickness of 10, 20 and 30 nm. Owing to the interest in minimizing the thickness of the front passivating contact to limit parasitic absorption, it is of interest to investigate what thickness of poly-Si is necessary to achieve complete surface coverage of the nanostructures. Less-than-complete surface coverage may result in degraded surface passivation. Some voids are visible in the poly-Si layer with nominal thickness of 10 nm, which implies that such thickness is not sufficient to provide full coverage of the hillock-like structures of bSi. Complete surface coverage is achieved for nominal thickness of 20 and 30 nm.

Next, we present measurements of sheet resistance of two 40 nm thick poly-Si layers, performed by µ4PP. The µ4PP is needed to avoid penetration of ultra-shallow junctions, which usually occurs when using macroscopic four-point probes. Penetration of the junction causes measurement errors, since the sheet resistance of the substrate is measured in parallel to that of the thin top-layer. Figure 2 shows line-scan measurements across the 100 mm wafer for p-type poly-Si and n-type poly-Si (top and bottom, respectively). A certain non-uniformity can be seen in the values of sheet resistance, likely due to non-uniformity of the LPCVD processing. The sheet resistance of the p-type poly-Si is rather high for a passivating contact, with lowest values of 4 kΩ close to the edge of the wafers. The n-type poly-Si, instead, is characterized by a by a more suitable sheet resistance between 600 and 800 Ω (apart from 1 mm or less from the edge of the wafer, where is drops to about 200 Ω).

Lifetime measurements on symmetrical samples (i.e. with poly-Si with the same polarity on both surfaces) are summarized in Figure 3. Both p-type and n-type poly-Si benefit from the hydrogenation induced by deposition of a sacrificial SiN_x:H followed by annealing. Importantly, the higher effective lifetime is retained in all cases after removing the sacrificial SiN_x:H layer. The lowest average effective lifetime of the p-type poly-Si passivated samples

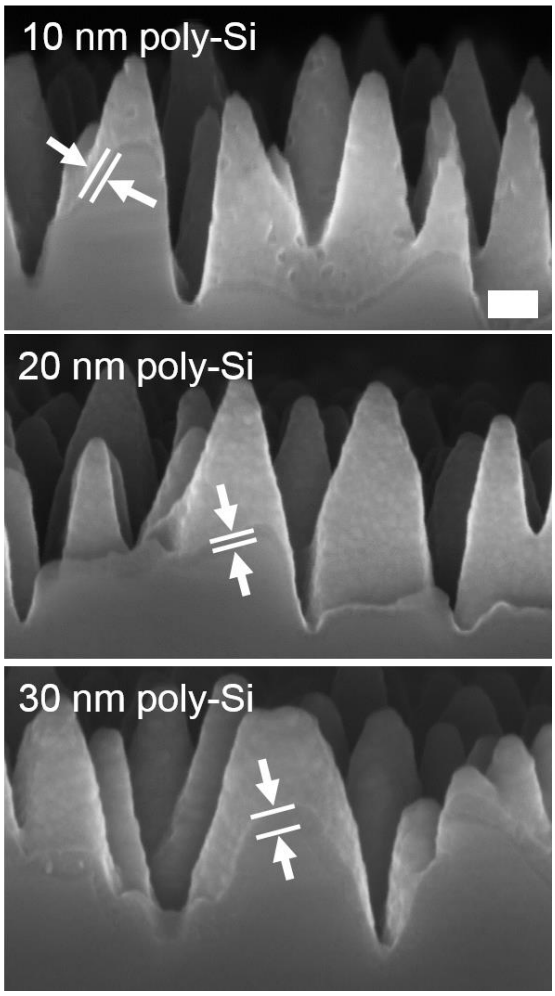

Figure 1: Cross-section SEM images of Si surfaces textured by RIE and coated with poly-Si layers of increasing nominal thickness. The poly-Si layers are indicated by the white arrow. The scale bar represents 100 nm.

is 162 ± 24 µs before hydrogenation. Both p-type poly-Si wafers show effective lifetime of around 750 µs after hydrogenation. Nonetheless, the quality of the passivation offered by our poly-Si is still far less-than-optimal and further work is needed to improve it. In addition to improve the quality of the p-type poly-Si, we are currently investigating the possibility to replace the SiO_2 tunnel layer grown by oxidation in HNO_3 with dry furnace oxidation. The quality of passivation afforded by as-deposited n-type poly-Si is an order of magnitude better than that of p-type poly-Si, with average lifetime between 2.8 and 3 ms. The average lifetime increases further upon hydrogenation, reaching 3.8 ms for the best sample.

Figure 4 summarizes measurements of effective lifetime mapping performed on asymmetrically passivated samples, i.e. with p-type poly-Si on the front and n-type poly-Si on the bottom (layer thickness of 40 nm in both cases). Two of the wafers were textured with bSi and this surface was passivated with p-type poly-Si. For these wafers, calculating the implied V_{oc} (i-V_{oc}) gives a more realistic indication of the voltage that the final cells will sustain. i-V_{oc} was calculated using the equation

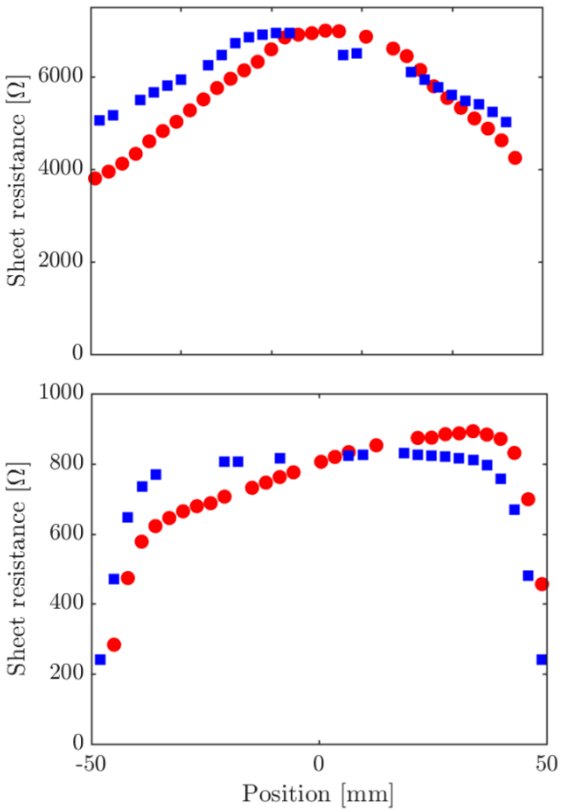

Figure 2: Sheet resistance measured along two perpendicular directions across a planar 100 mm wafer for p-type poly-Si (top) and n-type poly Si (bottom). Thickness of the poly-Si is 40 nm for both wafers.

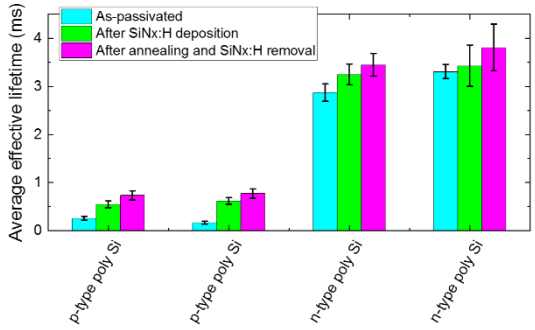

Figure 3: Effective lifetime averaged on full 100 mm wafers passivated symmetrically with 40 nm of either p-type or n-type poly-Si.

$$\text{i-}V_{OC} = \frac{kT}{q} \ln\left[\frac{\Delta n(\Delta n + N_D)}{n_i^2}\right]$$

where kT/q is the thermal voltage (25.85 mV at room temperature), N_D is the concentration of donors in the substrate, n_i is the intrinsic concentration of carriers in Si, and Δn is the concentration of light-generated carriers. Δn was calculated as the product of τ_{eff} and the photon generation rate G, which is known from measurements settings. The average lifetime before hydrogenation for planar wafers is between 333 ± 72 µs and 583 ± 62 µs. As expected, the lower quality of passivation afforded by the p-type poly-Si dominates the effective lifetime.

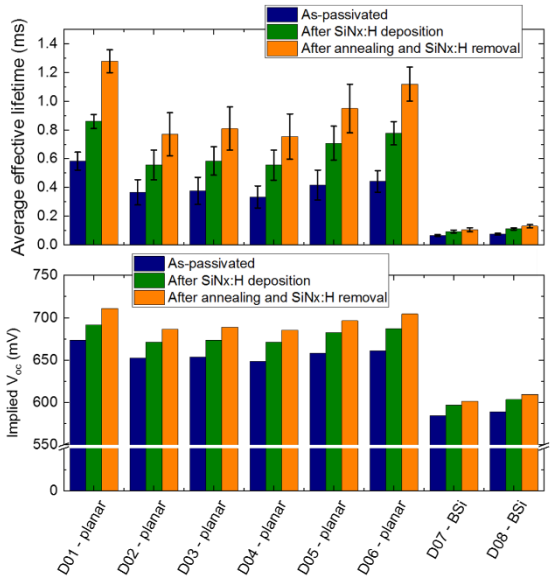

Figure 4. Top: effective lifetime averaged on full 100 mm wafers passivated asymmetrically with 40 nm p-type and n-type poly-Si on either side. Bottom: effective lifetime data converted in implied V_{oc} data for the same samples.

These values translate in i-V_{oc} of 648 and 673 mV, respectively. All samples show an increase of effective lifetime upon hydrogenation, with lifetime values after SiN_x:H removal of 1.28 ± 0.08 ms and 0.754 ± 0.16 ms. This translates into i-V_{oc} of 711 mV and 685 mV, respectively. The two bSi textured wafers show worse results, with average effective lifetime of 105 ± 12 µs and 130 ± 10 µs even after hydrogenation. This results into values of i-V_{oc} of 609 and 601 mV, respectively.

Finally, we present results from our first batch of solar cells. Here, the hydrogenation procedure was not carried out and thus lower performance is to be expected. Results of IV and spectral characterization are summarized in Figure 5. Our process flow, where the poly-Si is doped in-situ during LPCVD, allows for decoupling thickness of the front and back contact poly-Si, at the cost of a high number of process steps. Limiting the thickness of poly-Si front contact would be beneficial in terms of minimizing parasitic absorption. Here, we used a nominal thickness of 15 nm for the p-type poly-Si front contact, which should be sufficient to achieve full surface coverage even on textured substrates. The planar, non-textured cells show the highest performance, with maximum power conversion efficiency of 15.2%. The efficiency of cells with textured surfaces is considerably lower, 9.6 % for KOH texturing and 8.6 % for bSi texturing, respectively. The KOH texturing results in slightly higher J_{sc} than that of the planar reference (38.0 and 36.7 mA cm^{-2}, respectively). However, texturing results in considerably lower V_{oc} and lower fill factor. The latter may also be due to issues with metallization, which is currently under improvement. Finally, it is interesting that bSi texturing results in lower J_{sc} as well, as compared to the other cells. This is caused by the poorer passivation currently offered by the p-type poly-Si. The results in terms of J_{sc} are corroborated by measurements of quantum efficiency (QE) in the bottom panel of Figure 5. The data confirm that bSi textured cells, although with the highest potential for current generation thanks to the lowest front surface reflection, display the poorest QE and in particular very low QE for wavelength below 600 nm, which points once

again at poor passivation by the front contact. Besides the required improvement in the quality of our p-type poly-Si, it would also be of interest to passivate textured surfaces with n-type poly-Si and place the p-n junction at the bottom of the cell. Fabrication and testing of cells with this structure are underway.

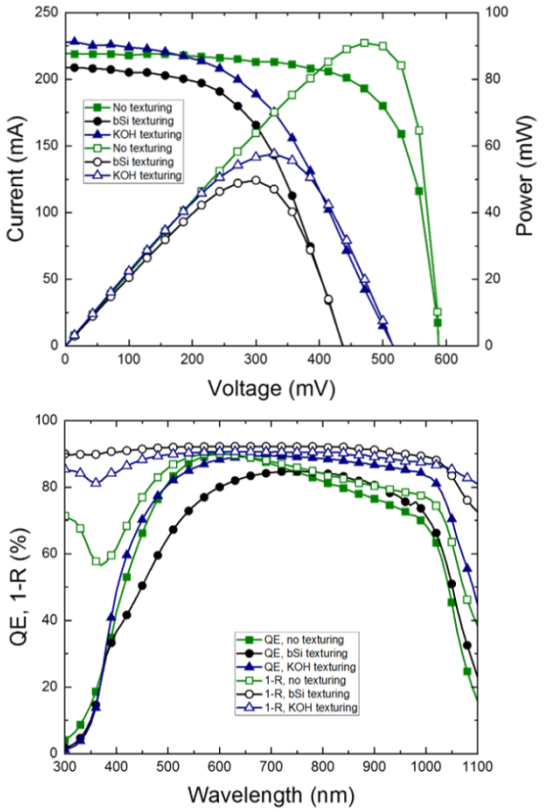

Figure 5: Characterization of solar cells with different surface texturing. Top: current-voltage characteristics under 1 Sun illumination. Bottom: quantum efficiency and front surface reflection subtracted from unity as function of photon wavelength.

4 CONCLUSIONS

We presented passivating contacts of *in-situ* doped poly-Si, fabricated by low pressure chemical vapor deposition, on planar and black Si textured surfaces. SEM characterization confirms that full surface coverage of black Si surfaces is achieved for thickness of poly-Si of 20 nm. We achieved implied V_{oc} values of up to 711 mV for asymmetrically passivated lifetime samples without texturing and after hydrogenation using a sacrificial SiNx:H. The effective lifetime is limited by the less-than-optimal passivation of the p-type poly-Si. The values of i-V_{oc} measured on bSi textured surfaces are lower (609 mV). Preliminary solar cells measurements indicate that both cell voltage and fill factor require major improvement on textured surfaces. Current work is focusing on: improving the quality of the p-type poly-Si; testing possible replacement of wet chemistry to grow the tunnel oxide with dry furnace oxidation; fabricating and comparing cells with p-n junction at the front or at the bottom of the cell.

5 ACKNOWLEDGMENTS

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