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Abstract

This report presents circuits with complementary transistors intended for the realization of logical functions. The advantage of these circuits is shown to be the simple dimensioning, leading to great flexibility in the realization of logical functions and efficient utilization of the components. This is paid for by a lower transmission speed than that ultimately possible with the same active components.

The basic circuits are interpreted as representing single logical functions (AND, OR and NOT) in double-polarity logic, while the single-polarity logic circuits normally used represent combined logical functions (NOR and NAND).

Contents

1. Introduction

The present report is intended to give a brief description of the circuits used by the data-processing section of the Electronics Department for the realization of logical functions. These circuits must not be regarded as standard circuits for use in all digital systems to be designed. However, they have proved very useful for experimental work in enabling us to design data-recording equipment with the fewest possible components, simple dimensioning and a high degree of reliability. In some measure these advantages have been obtained at the expense of speed, but in most equipment in current use the reaction time of the logic circuits is unimportant as compared with that of other components such as relays, recording units and motors.

2. Logic Circuits with pnp and npn Transistors

Even if we confine ourselves to the realization of logical functions by means of semiconductor components, there are many possibilities. The most frequently used circuits are based on resistance-transistor or diode-transistor logic circuits, in which the logical function is realized by means of resistances and diodes respectively, while the transistor serves as an amplifier. The circuits described[1, 2, 3] are all based on the use of mainly one type of transistor, either pnp or npn. This means that the logical truth value ("1") is represented by either a negative or a positive voltage (single-polarity logic). In consequence, a circuit usually satisfies a combined logical function, either NOT-OR (NOR) or NOT-AND (NAND).

In its work with digital technique, the data-processing section has employed another circuit type, based on the utilization of the complementary properties of pnp and npn transistors; the two kinds of transistor are used alternately, i.e., the outputs of pnp transistors activate the inputs of npn transistors. One advantage of this combination is the possibility of dimensioning with a wider safety margin (the "efficiency" is greater) as the collector current of a transistor is utilized to a higher degree for the control of the following stages. At the same time the basis of the dimensioning (see the appendix) is simpler and provides a better possibility of individual dimensioning. Thus one is allowed more liberty in the choice of fan-in and fan-out numbers and hence a better possibility of realizing a given logical function by means of the fewest possible components. It is natural to inter-

pret these circuits as being based on double-polarity logic, i. e., "1" is represented now by a positive, now by a negative voltage according as the function is realized by a pnp or an npn circuit. This means that a single circuit does not perform logical inversion (NOT); it is therefore necessary to use special circuits to realize NOT functions.

Figure 1 shows the circuits it has proved expedient to use, together with the block symbols representing them in the double-polarity logic. As signal voltages corresponding to "1" are used 0 and -8 volts. Thus the polarity signs of the block symbols indicate the voltage, + for 0 volts and - for -8 volts, that corresponds to the logical truth value of the wire concerned. In block combinations the connections must accordingly have the same polarity sign at both ends.

Where this is not the case, polarity changers must be inserted. These stages are AND circuits whose emitter has a fixed potential corresponding to the logical truth value of the circuit in question. With a view to the practical work, however, it is expedient to give these circuits a block symbol of their own (fig. 2).

The NOT function is here realized by a diode-transistor circuit in which the transistor has the same polarity as has that activating the circuit. A variant of the NOT circuit, the inhibitor circuit, is shown in fig. 2.

The work connected with the realization of a compound logical function naturally falls in three phases, namely working out of a descriptive logic block diagram, the logic block diagram used, and the circuit diagram. By way of example the design of an equalizer is shown in fig. 3.

The disadvantages of the use of complementary circuits are in the first place that, for the desired possibilities to be available, one must have several circuits, namely for both the AND and/or OR and the NOT functions, and of the pnp as well as the npn type.

In the second place these circuits are slower than single-polarity ones because less power is available to counteract the storage effect in the transistors. Where transistors of recent design are used, the difference is, however, only a fraction of a microsecond and usually of no importance in data-processing equipment.

The use of complementary transistors in memory circuits (bistable circuits) has been investigated by Bossart (ref. 4); the paper contains calculations of the storage time and rise time of these circuits, but combinatory circuits are not dealt with in detail.

As seen in fig. 4, a bistable circuit with DC set and reset is built up by means of the elementary logic circuits. In literature such a circuit is

often referred to as "latch" to distinguish it from the flip-flop, which requires a shift pulse to be brought into a state corresponding to the conditions indicated on it. The flip-flop or triggered bistable circuit is used with advantage for instance in shift registers because the memory required during the shift may be realized by means of passive components.

Figure 5 shows the realization of a triggered bistable circuit with complementary transistors. The set-reset function is here performed by a symmetrical transistor; if A is 0 volts (true value, "1"), the symmetrical transistor will work as an emitter follower and, by a pulse at its base, set the bistable circuit; if A is not 0 volts (false value, "0"), the transistor will work as a collector follower and, by a pulse at its base, reset the circuit.

Acknowledgement

The author is indebted to Flemming Steenbuch for the translation of this report into English.

Appendix

A. 1. Dimensioning of Logic Circuits with pnp and npn Transistors

Figure 6 shows a section of a circuit from a logic system in which the complementary properties of pnp and npn transistors are utilized. If the block diagram is realized by means of the circuits shown in fig. 1, an AND block will result in a chain of transistors (p and q), while the OR blocks will be realized by diode matrices (m, n and m', n'). If we consider a transistor in the chain q, we may determine the collector current that the transistor must be capable of supplying to the n' following stages, and thus the base current required by the transistor.

In the absence of this base current, the transistor must be securely cut off by means of the resistance R_A and the voltage V_3.

When all the n chains loading a chain p have been determined in this way, the conditions for the chain p have been fixed.

The following symbols are used in addition to those indicated in the figure:

I_d : diode reverse current

V_C : voltage drop of the collector emitter in the case of conducting transistor

V_B : voltage drop of the base emitter in the case of conducting transistor

V_D : voltage drop of the diode

I_{CBO} : collector cut-off current.

The maximum value of the collector current that the chain q must be able to supply to the row k' will be

$$\max I_C = \sum_{j=1}^{n'} a_{k'j} \frac{V_2}{R_{B'}} + \left(\sum_{j=1}^{m'} a_{ij} \sum_{i=1}^{n'} a_{k'j} - \sum_{j=1}^{n'} a_{k'j} \right) I_d \,, \quad (1)$$

where $a_{ij} = 1$ when a diode is inserted between the wires i and j; in the absence of a diode, $a_{ij} = 0$.

The first term of eq. (1) is the total base current to be supplied by the chain q, the last term is the maximum total diode reverse current to be given off. This happens when only one of the rows in the matrix network m' n' is activated (represents logical "1").

From eq. (1) we have

$$\max I_C = \sum_{j=1}^{n'} a_{k'j} \frac{V_2}{R_{B'}} + \sum_{j=1}^{n'} a_{k'j} \left(\sum_{i=1}^{m'} a_{ij} - 1 \right) I_d \quad . \qquad (2)$$

The minimum base current available to a transistor in the chain q is

$$I_B = \frac{V_2 - (p+q-1)\, V_C - V_B - V_D}{R_B} - \frac{V_3 + (q-1)\, V_C + V_B}{R_A} \quad . \qquad (3)$$

On insertion of the current amplification $\beta = \frac{I_C}{I_B}$ we derive from eqs. (2) and (3) the following inequality, which must be fulfilled to ensure that a transistor is conducting, that is, that the voltage drop of the collector emitter is smaller than the knee voltage:

$$\beta \left(\frac{V_2 - (p+q-1) V_C - V_B - V_D}{R_B} - \frac{V_3 + (q-1) V_C + V_B}{R_A} \right) \geq \sum_{j=1}^{n'} a_{k'j} \frac{V_2}{R_{B'}} + \sum_{j=1}^{n'} a_{k'j} \left(\sum_{i=1}^{m'} a_{ij} - 1 \right) I_d \, . \qquad (4)$$

To ensure the cut-off of the transistor the following inequality must be satisfied:

$$\frac{V_3}{R_A} \geq \sum_{i=1}^{m} a_{il}\, I_{CBO} + \left(\sum_{i=1}^{m} a_{il} \sum_{j=1}^{n} a_{ij} - \sum_{i=1}^{m} a_{il} \right) I_d + I_{CBO} \quad ; \qquad (5)$$

the first term is the collector cut-off currents from all transistors that can activate the transistor considered, the second term is the diode reverse currents in those rows of the matrix network which are connected to the column l, and the last term is the cut-off current of the transistor itself. Eq. (5) may be rewritten as

$$\frac{V_3}{R_A} \geq \left(\sum_{i=1}^{m} a_{il} + 1 \right) I_{CBO} + \sum_{i=1}^{m} a_{il} \left(\sum_{j=1}^{n} a_{ij} - 1 \right) I_d \quad . \qquad (6)$$

It should be noted that the quantities on both sides of the inequality sign in (4) should in fact be corrected for the position of the transistor in the chain q since a transistor at the bottom of the chain must also supply the base current of the other transistors in the chain. This is compensated for by the fact that the bottom transistor is itself supplied with a stronger base current, and we find that if the inequality

$$\frac{V_2}{R_B} - \frac{V_3}{R_A} < \beta \left(\frac{V_C}{R_B} + \frac{V_C}{R_A} \right)$$

is satisfied, (4) holds. This is the case, to a sufficient approximation, with the circuits used in practice.

If we compare (4) and (6) with the corresponding inequalities for single-polarity logic circuits (ref. 1), we see that the advantage of calculating the double-polarity circuits is that from (6) we may determine R_A independently of the other stages (and R_B) and then, by means of (4) , may determine R_B from our knowledge of the preceding and the following stage.

From (3) and $\beta I_B = I_C$ we obtain for R_B the expression

$$R_B \quad \frac{V_2 - (k + 1 - 1) V_C - V_B - V_D}{\frac{I_C}{\beta} + \frac{V_3 + (1 - 1) V_C + V_B}{R_A}} \quad .$$

This expression has the form

$$R_B \leq \frac{V_2'}{\frac{I_C}{\beta} + \frac{V_3'}{R_A}} \quad ,$$

where V_2 and V_3 are corrected for the transistor and diode voltage drops.

A. 2. Calculation of Standard Component Values

By a circuit with standard component values is understood a circuit with fixed transistors, diodes and resistance values. If a logic system is realized with such circuits, the load must be kept within the permissible values of these.

For circuits of this kind we must have

$$\sum_{j=1}^{n'} a_{k'j} \sum_{i=1}^{m'} a_{ij} = \sum_{i=1}^{m} a_{il} \sum_{j=1}^{n} a_{ij}$$

and

$$R_{B'} = R_B .$$

By means of (6), expression (4) may then be rewritten

$$\beta \left(\frac{V_2 - (p+q-1) V_C - V_B - V_D}{R_B} - \frac{V_3 + (q-1) V_C + V_B}{R_A} \right) \geq \sum_{j=1}^{n'} a_{k'j} \frac{V_C}{R_B} + \frac{V_3}{R_A} \quad . \quad (7)$$

Putting

$$\sum_{j=1}^{n'} a_{k'j} = N \quad \text{(fan-out number)} ,$$

we have

$$\frac{V_2 \left(1 - \frac{N}{\beta}\right) - (p+q-1) V_C - V_B - V_D}{V_3 \left(1 + \frac{1}{\beta}\right) + (q-1) V_C + V_B} \geq \frac{R_B}{R_A} \quad .$$

Example:

The nominal voltages used are

$V_2 = -8.5$ volts

$V_3 = -4.5$ volts.

For the transistors, OC 47 and OC 141, and the diode, OA 85, we have

$V_C \sim 0.20$ volt (OC 47 and OC 141; $I_C = 10$ mA; $T = 25^\circ C$)

$V_B \sim 0.35$ volt (" " " " ")

$\beta \sim 30$ (min OC 47 : 50; OC 141 : 100; $I_C = 15$ mA)

$V_D \sim 0.5$ volt (OA 85; $I_D = 2$ mA; $T = 25^\circ C$) .

If we assume tolerances of +10% for V_2 and -10% for V_3, +5% for R_B and -5% for R_A (worst-case design) and nominal values of R_B and R_A of

$\underline{R_B = 3.9\ k\ \Omega}$

$\underline{R_A = 4.7\ k\ \Omega}$,

we obtain the following inequality that must be fulfilled:

$\underline{N + 0.8\,p + 1.5\,q < 10.}$

$\underline{p = q = 1;\quad N < 8}$

$\underline{p = q = 2;\quad N < 5}$

$\underline{p = q = 3;\quad N < 3}$.

The condition (6) sets a limit to the number of diodes. With the values

$I_{CBO} = 100\ \mu A$ (max OC 47 and OC 141: 35 μA; $V_C = 5$ volts; $T = 60^\circ C$)

$I_d = 50\ \mu A$ (max OA 85 : 40 μA; $-V_D = 10$ volts; $T = 60^\circ C$)

and the earlier used values of V_3 and R_A, with the most unfavourable tolerances, we obtain the condition

$$\sum_{i=1}^{m} a_{il} \left(\sum_{j=1}^{n} a_{ij} + 1 \right) \leq 14 \quad .$$

We put

$$\sum_{i=1}^{m} a_{il} \quad \sum_{j=1}^{n} a_{ij} = \sum N ,$$

which is the sum of the fan-out numbers of all transistors activating the transistor considered. Further we put

$$\sum_{i=1}^{m} a_{il} = M \quad \text{(fan-in number)}$$

and obtain

$$\underline{M + \sum N \leqq 14 .}$$

A. 3. The Load Conditions of the NOT Circuit

The NOT circuit employed, and the variants NOR and INHIBITOR, are dimensioned on the basis of the formulae given by Masher[1]. Figure 7 shows the permissible load conditions, the symbols being the same as above. The values of voltages, currents, tolerances, etc., are likewise the same as those used in the foregoing.

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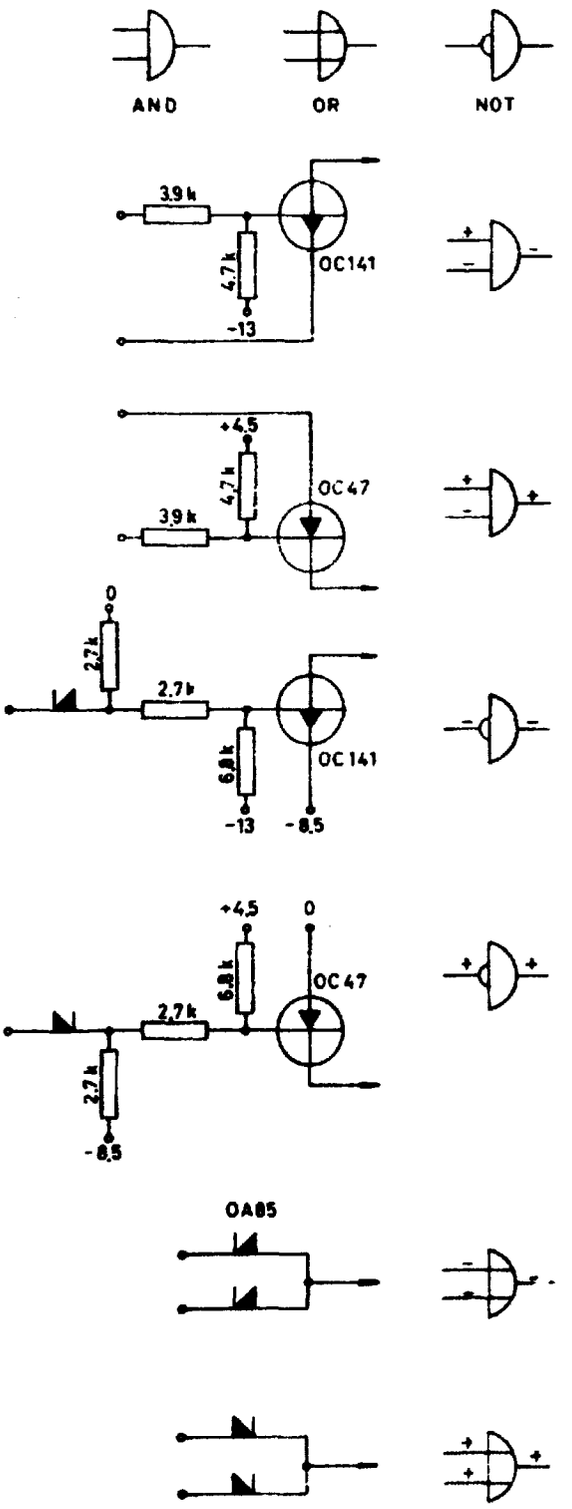
2) W. J. Wray, DC Design of Resistance Coupled Transistor Logic Circuits. I. R. E. Transactions on Circuit Theory CT-6 (1959) 304-310.

3) W. B. Cagle and W. H. Chen, A New Method of Designing Low Level, High Speed Semiconductor Logic Circuits. Wescon Convention Record, Pt. 2 (1957) 3-9.

4) Lee M. Bossart, Complementary Transistor Memory Circuit and Logic Applications. SCTM 51-62 (72) (1962).



Logic circuit and corresponding symbols for double - polarity logic

The signs indicate the signal polarity of the logical truth value

Fig. 1. Logic block symbols.

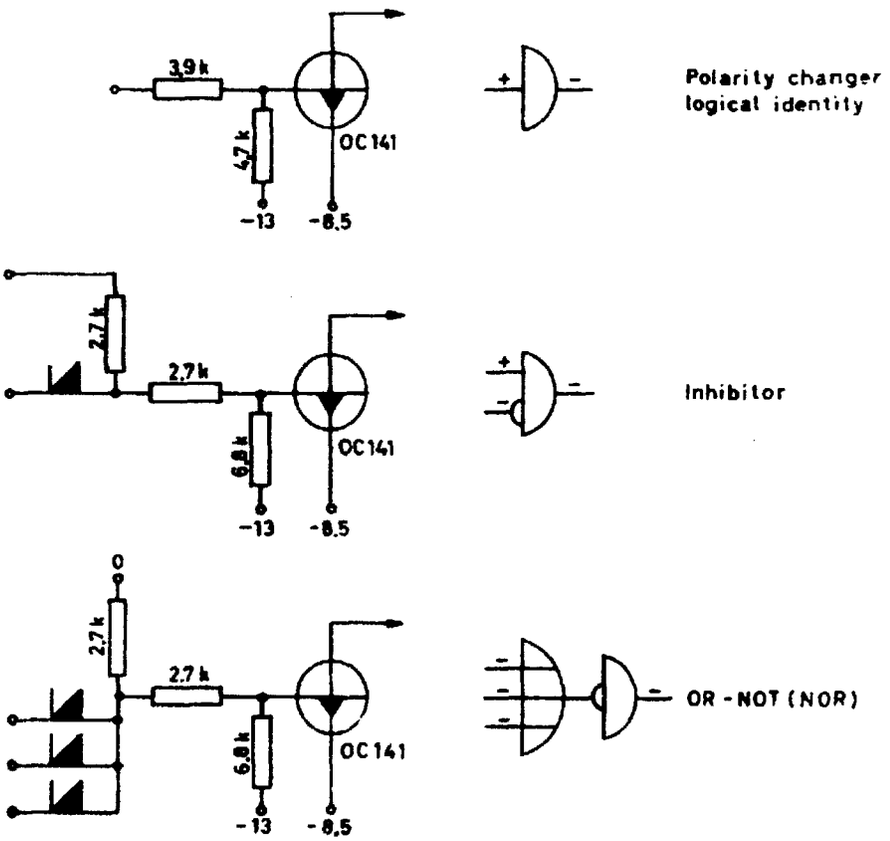


Fig. 2. Variants of circuits in fig. 1.

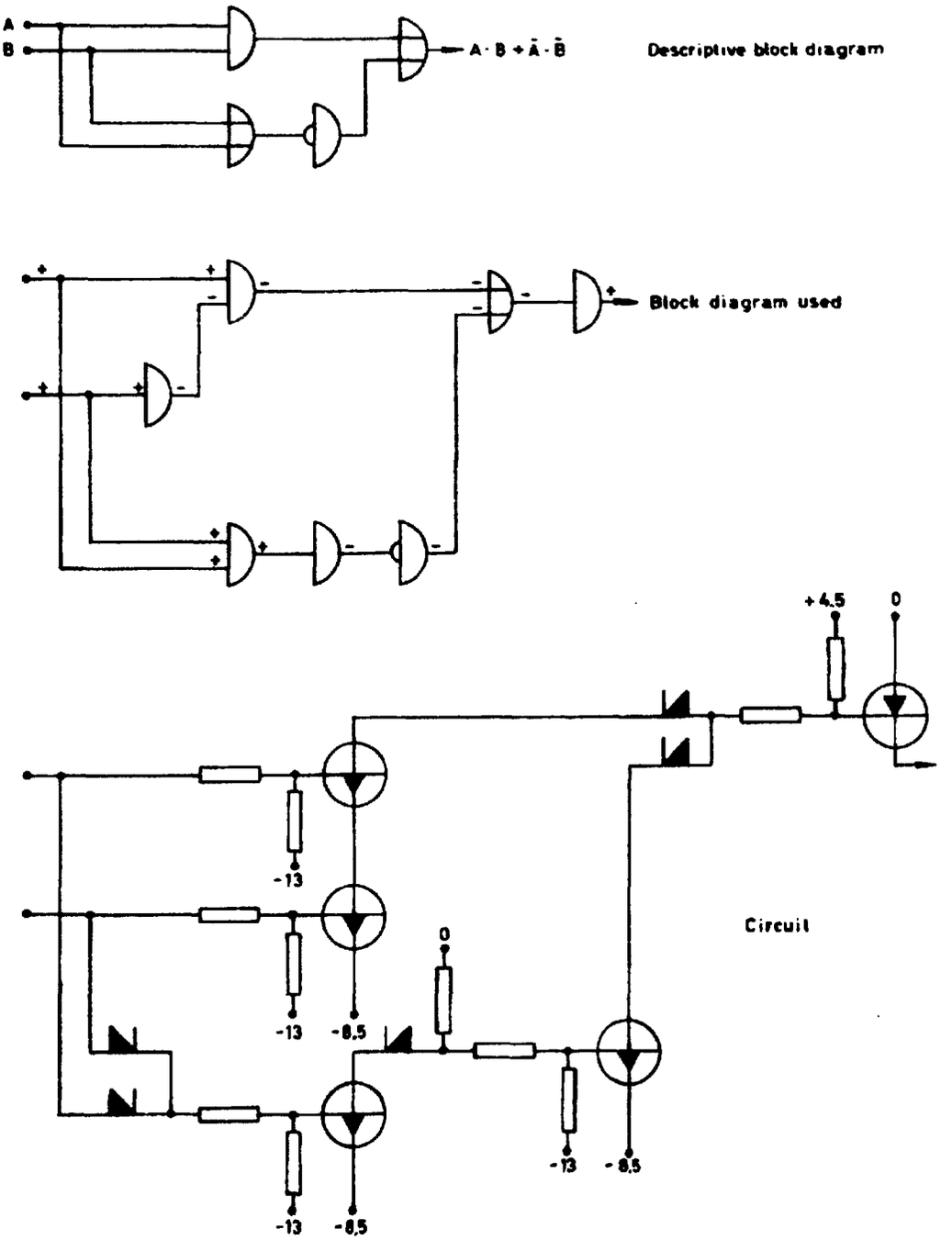


Fig. 3. Equalizer.

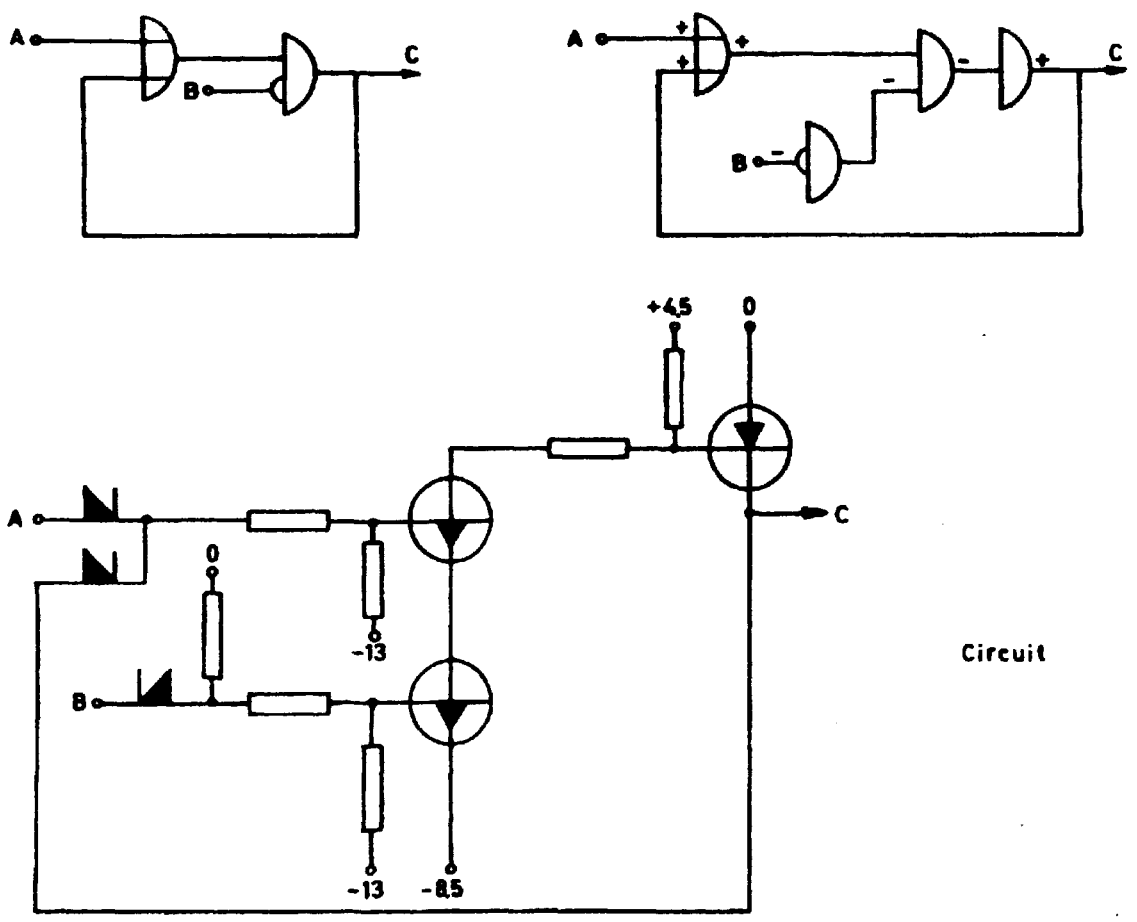


Fig. 4. Bistable circuit (RS flip-flop, "latch").

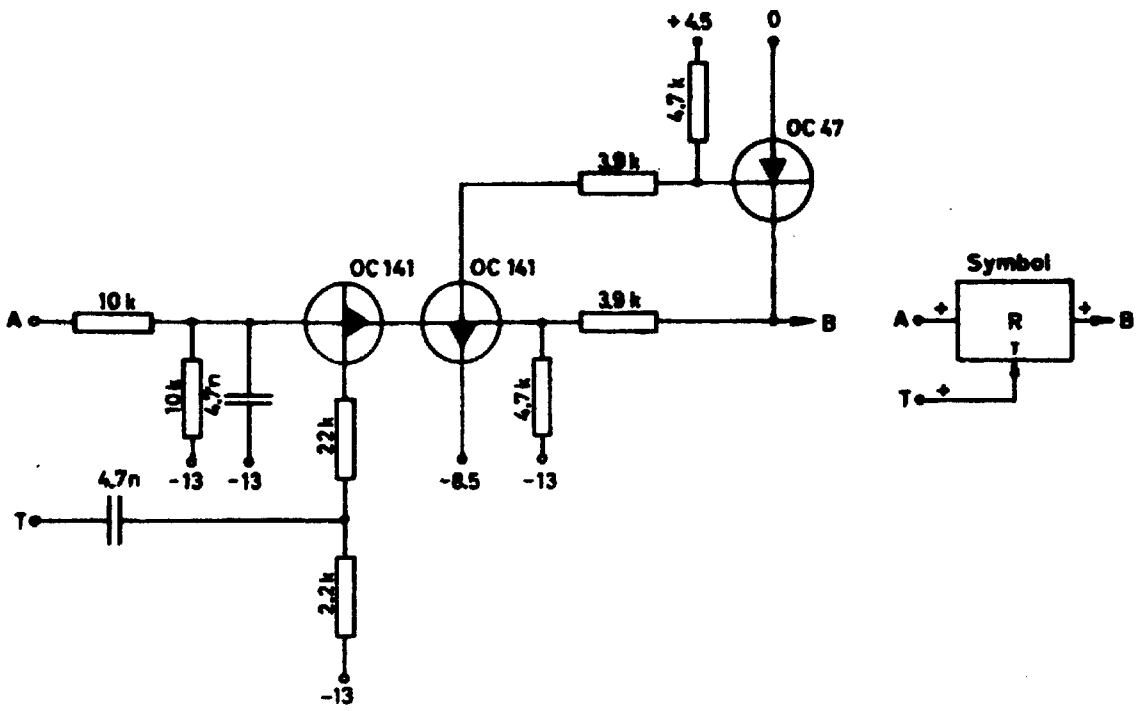


Fig. 5. Triggered bistable circuit (RST flip-flop).

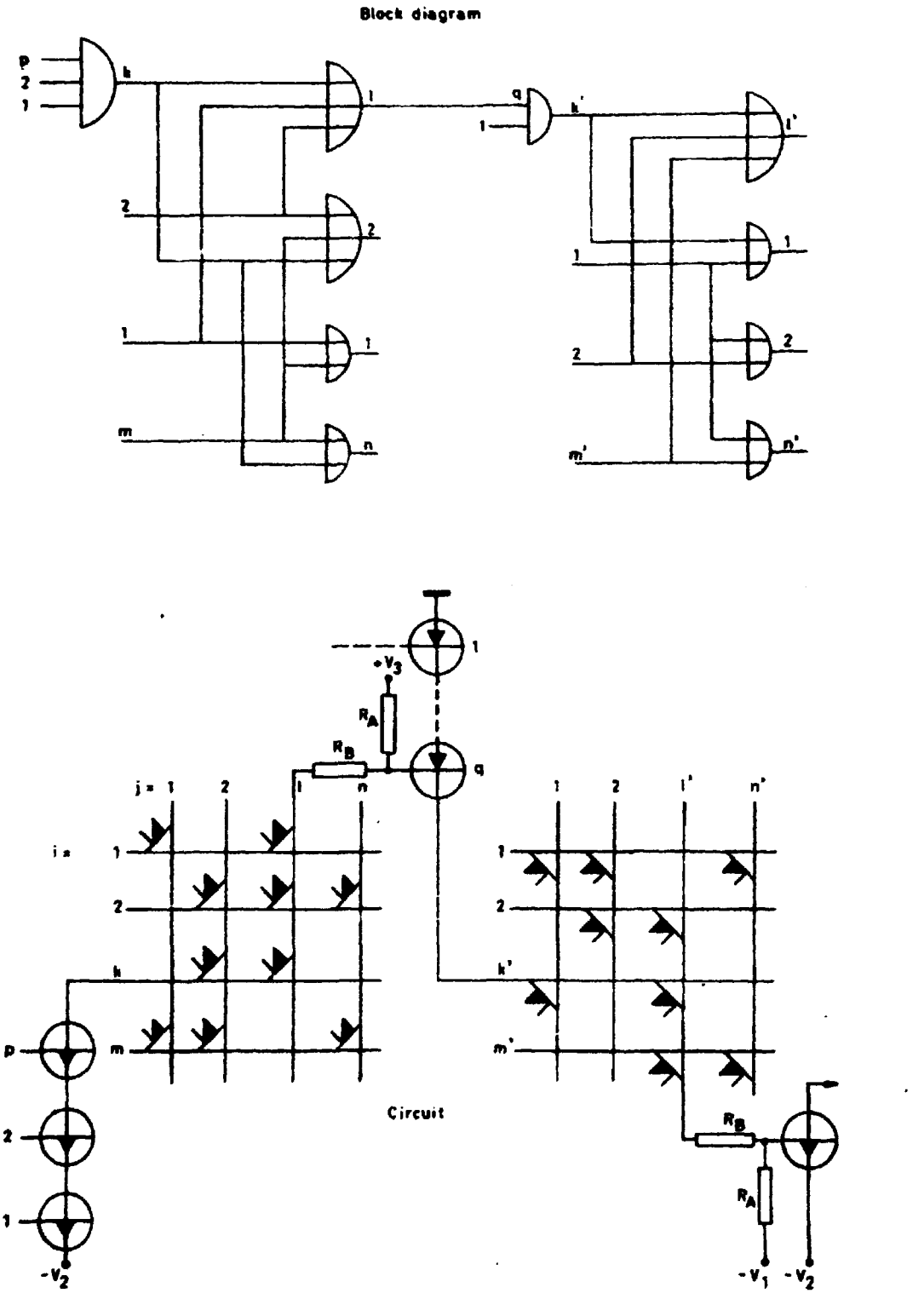


Fig. 6. Calculation of component values.

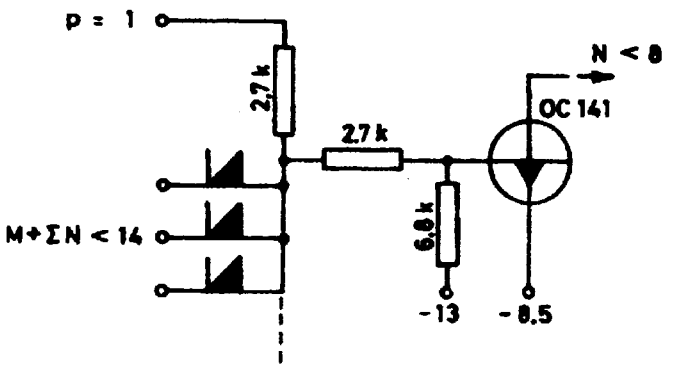


Fig. 7. Load conditions of the NOR inhibitor.