Reconfiguration of Computation and Communication Resources in Multi-Core Real-Time Embedded Systems

Reconfigurable computing allows application programmers to significantly increase the speed of software algorithms by implementing computationally demanding tasks in hardware while maintaining a certain degree of flexibility. This can be achieved by using FPGAs to implement hardware accelerators that can be reconfigured when no longer needed, enabling the re-use of the resources of the FPGAs to realise new functionalities. For multi-core platforms, reconfiguration can be extended to the infrastructure supporting intercore communication and used to dynamically modify the characteristics of the communication channels between the tasks that are affected by the reconfiguration. This thesis investigates the use of reconfiguration in the context of multicore real-time systems targeting embedded applications. We address the reconfiguration of both the computation and the communication resources of a multi-core platform. Our approach is to associate reconfiguration with operational mode changes where the system, during normal operation, changes a subset of the executing tasks to adapt its behaviour to new conditions. Reconfiguration is therefore used during a mode change to modify the real-time guaranteed services provided by the hardware platform to fit the requirements of the current mode. The reconfiguration of the computation resources consists of altering the hardware implementation of selected resources, such as accelerators, and it is achieved by using the dynamic partial reconfiguration feature offered by FPGAs. With regards to this, we also present a lightweight reconfiguration controller, named RT-ICAP, specially developed to support time predictable dynamic partial reconfiguration. There configuration of the communication resources consists of setting up and tearing down the end-to-end channels offered by the communication fabric between the cores of the platform. To support this, we present a new network on chip architecture, named Argo 2, that allows instantaneous and time-predictable reconfiguration of the communication channels. Our reconfiguration-capable architecture is prototyped using the existing time-predictable multi-processor platform T-CREST. The thesis also presents low-level reconfiguration time analysis for these architectures. The evaluation of the proposed approach and the developed architectures is carried out using synthetic benchmarks and hardware accelerators generated by high-level synthesis tools. For the reconfiguration of computation resources, the results show that the use of accelerators in combination with dynamic partial reconfiguration leads to better utilisation of the FPGA resources and tighter worst-case execution time bounds than a pure software solution. Moreover, the results show that using are configurable solution delivers a worst case performance comparable with that of a non-reconfigurable solution. For the reconfiguration of communication resources, the results show that the worst-case reconfiguration time ranges from hundreds to thousands of clock cycles, making our solution considerably faster than other functionally equivalent networks-on-chips. In addition to the evaluation based on synthetic benchmarks, we also present a proof-of-concept case study based on a multi-core audio digital signal-processing application that combines reconfiguration of both the computation and communication resources. The case study shows that the presented approaches for reconfiguration can be effectively used in a real-world application and can lead to a reduction of the overall hardware size and better use of the platform resources while maintaining comparable computation performance with respect to a non-reconfigurable approach.

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