Low power/low voltage techniques for analog CMOS circuits

This work presents two separate study cases to shed light on the different aspects of low-power and low-voltage design. In the first example, a low-voltage folded cascode operational transconductance amplifier was designed to achieve 1-V power supply operation. This is made possible by a novel current driven bulk (CDB) technique, which reduces the MOST threshold voltage by forcing a constant current though the transistor bulk terminal. A prototype was fabricated in a standard CMOS process; measurements show a 69-dB dc gain over a 2-MHz bandwidth, and compatible input- and output voltage levels at a 1-V power supply. Limitations and improvements of this CDB technique are discussed. The second part of the work is concerned with analog RF circuits. A previously unknown intrinsic non-linearity of standard ΣΔ fractional-N synthesizers is identified. A general analytical model for ΣΔ fractional-N phased-locked loops (PLLs) that includes the effect of the non-linearity is derived and an improvement to the standard synthesizer topology is discussed. Also, a new methodology for behavioral simulation is presented: the proposed methodology is based on an object-oriented event-driven approach and offers the possibility to perform very fast and accurate simulations; the theoretical models developed validate the simulation results. A study case for EGSM/DCS modulation is used to demonstrate the applicability of the simulation methodology to the analysis of real situations. A novel method to calibrate the frequency response of a Phase-Locked Loop concludes the research. The method requires just an additional digital counter to measure the natural frequency of the PLL; moreover it is capable of estimating the static phase offset. The measured value can be used to tune the PLL response to the desired value. The method is demonstrated mathematically on a typical PLL topology and it is extended to ΣΔ fractional-N PLLs.

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