High Speed Frame Synchronization and Viterbi Decoding - DTU Orbit (21/10/2019)

High Speed Frame Synchronization and Viterbi Decoding: Final Report
The study has been divided into two phases. The purpose of Phase 1 of the study was to describe the system structure and algorithms in sufficient detail to allow drawing the high level architecture of units containing frame synchronization and Viterbi decoding. After selection of which specific units to detail, the purpose of Phase 2 was to make VHDL models for the selected units. The overall development process is described in the report. The systems we consider are high data rate space communication systems. Also, the systems use some form of QPSK modulation and transmit data in frames separated by a sync marker and protected by error-correcting codes. We first give a survey of trends within the area of space modulation systems. We then discuss and define the interfaces and operating modes of the relevant system components. We present a list of system configurations that we find potentially useful. Algorithms for frame synchronization are described and analyzed. Further, the high level architecture of units that contain frame synchronization and various other functions needed in a complete system is presented. Two such units are described, one for placement before the Viterbi decoder and another for placement after the decoder. The unit for placement after the decoder was selected for detailing in Phase 2. We describe the detailed architecture in sufficient detail to allow modeling and verification of the models. The models aim at specifying all functional details and may be a first step towards a realization in an FPGA. Node synchronization performed within a Viterbi decoder is discussed, and the high level architectures of three possible implementations of Viterbi decoders are described: The first implementation uses a number of commercially available decoders while the two others are completely new implementations aimed at ASICs, one for a data rate of 75 Mbit/s and the second for a data rate of 150 Mbit/s. The latter unit was selected for detailing in Phase 2. We describe the detailed architecture in sufficient detail to allow modeling and verification of the models. The models aim at specifying all functional details and may be a first step towards a realization in an ASIC.

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