Exploring conductivity in ex-situ doped Si thin films as thickness approaches 5nm

Silicon (Si) has been scaled below 10nm in multigate and silicon-on-insulator (SOI) device technologies, but clearly Si thickness cannot be reduced indefinitely, as we will run out of atoms eventually. As thickness approaches 5nm, surfaces and interfaces will significantly impact the electrical behavior of Si, and surface physics cannot be discounted. Below that, bulk material properties will be altered considerably in the few-monolayer limit. One of the most basic defining properties of a semiconductor is its conductivity. To improve conductivity, while inducing a channel by appropriate biasing, it is necessary to define an accurate impurity doping strategy to reduce parasitic resistance. In this paper, we investigated the changing electrical conductivity of SOI films as a function of the Si thickness, in the range of 3–66nm. SOI films were ex situ doped using three different approaches: liquid/vapor phase monolayer doping of phosphorus using allyldiphenylphosphine, gas-phase doping of arsenic using arsine (AsH3), and room-temperature beam-line ion implantation of phosphorus. The circular transfer length method and micro-four-point probe measurements were used to determine the resistivity of the Si films, mitigating the contribution from contact resistance. The resistivity of the Si films was observed to increase with decreasing Si film thickness below 20nm, with a dramatic increase observed for a Si thickness at 4.5nm. This may drastically impact the number of parallel conduction paths (i.e., nanowires) required in gate-all-around devices. Density functional theory modeling indicates that the surface of the Si film with a thickness of 4.5nm is energetically more favorable for the dopant atom compared to the core of the film.

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