Analysis and implementation of packet preemption for Time Sensitive Networks

A standard priority-queuing system is capable of arranging packets with different traffic classes to guarantee a relatively low latency for the high priority traffic. However, in practical cases, severe delay may be caused by starting a large, low-priority frame ahead of a time-critical frame. In this paper, interspersed express traffic is evaluated, which enables preemption of non-time-critical transmission, in particular, the preemptive queuing system allows the cut-through transmission for critical traffic and minimizes the jitter. We analyse the performance of packet preemption through a system level simulation in Riverbed Modeler. The simulation is complemented by numerical analysis which provides the average queuing delay for both types of traffic (preemptable and express). Furthermore, the paper describes an approach to implement the packet preemption solution on an FPGA in VHDL, which illustrates the complexity of hardware implementation.

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