An SDRAM controller for real-time systems

For real-time systems we need to statically determine worst-case execution times (WCET) of tasks to proof the schedulability of the system. To enable static WCET analysis, the platform needs to be time-predictable. The platform includes the processor, the caches, the memory system, the operating system, and the application software itself. All those components need to be timing analyzable. Current computers use DRAM as a cost effective main memory. However, these DRAM chips have timing requirements that depend on former accesses and also need to be refreshed to retain their content. Standard memory controllers for DRAM memories are optimized to provide maximum bandwidth or throughput at the cost of variable latency for individual memory accesses. In this paper we present an SDRAM controller for realtime systems. The controller is optimized for the worst case and constant latency to provide a base of the memory hierarchy for time-predictable systems.

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