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A Fast-Processing Modulation Strategy for Three-Phase Four-Leg Neutral-Point-Clamped Inverter Based on the Circuit-Level Decoupling Concept

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Abstract—**In this paper, a modulation strategy based on the circuit-level decoupling concept is proposed and investigated for the three-level four-leg neutral-point-clamped (NPC) inverter, with the aim of delivering power to all sorts of loads, linear/nonlinear and balanced/unbalanced. By applying the proposed modulation strategy, the four-leg NPC inverter can be decoupled into three three-level Buck converters in each defined operating section. This makes the controller design much simpler compared to the conventional four-leg NPC inverter controllers. Also, this technique can be implemented with a simple logic and can be processed very quickly. Moreover, the switching loss is reduced substantially and the dc-link capacitors' voltages balance is also achieved without any feedback control. The proposed modulation technique is verified by the experiment.**

Keywords-circuit-level decoupling; inverter; neutral-point-clamped; PWM modulation; three-level

I. INTRODUCTION

The neutral-point-clamp (NPC) inverter [1], [2], is the most extensively applied converter topology at present. However, the conventional three-leg NPC inverters are not suitable for three-phase four-wire systems [3]. The four-leg NPC inverter is a promising topology compared to the three-leg NPC inverter in three-phase four-wire systems [4]-[6]. A great variety of modulation methods available for this inverter can be classified as pulse width modulation (PWM) and 3D space vector modulation (SVM) [4]-[7]. However, all these previously proposed modulation schemes have considerable disadvantages such as complicated digital logic as in 3D SVM and non-complete utilization of the inverter capacity as in SPWM.

A new modulation strategy for the three-level four-leg NPC inverter is introduced in this paper and a theoretical basis for the proposed strategy is developed based on the analysis of circuit-level decoupling method [8], [9]. The salient features of the proposed strategy are the following:

- The four-leg NPC inverter can be decoupled into three-level Buck converters in every 60° operating section of a fundamental cycle, which leads to a simpler design of closed-loop controllers;
- It provides inherent capability to maintain the voltages of the DC capacitors equal without any requirement to additional control effort;
- As six of its sixteen switches are not operated at switching frequency at any instant, the switching losses are reduced;
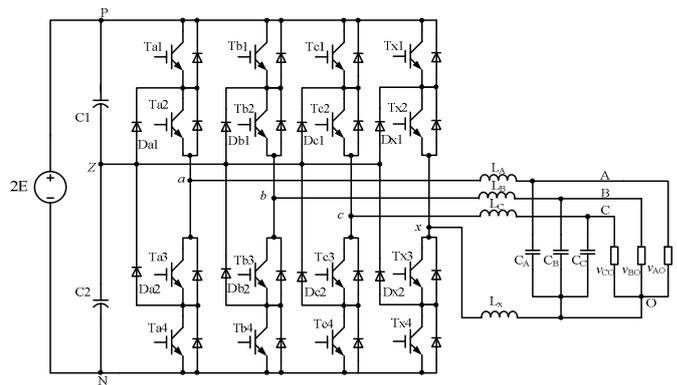- Only one carrier wave is needed for PWM signal modulating.

Figure 1. Schematic of the three-phase four-leg NPC inverter topology.
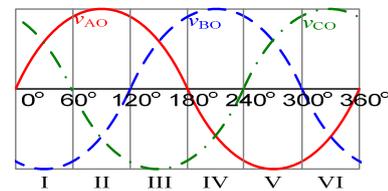
Figure 2. Waveform of the three-phase output voltage.
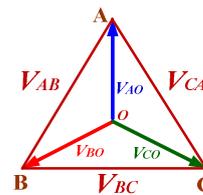
Figure 3. Vector diagram of the three-phase ouput voltages.

This paper introduces the circuit-level decoupling of the four-leg NPC inverter and the modulation strategy implementation in section II, and provides the detailed analysis on implementation of the proposed PWM scheme in section III. Section IV presents the experimental results, and finally section V concludes this paper by highlighting the advantages of the proposed modulation strategy.

II. OPERATION PRINCIPLE OF THE PROPOSED PWM MODUALTION STRATGY

A. Idea of the Circuit-Level Decoupling Scheme

A three-level four-leg NPC inverter is depicted in Fig. 1. Well controlled, the inverter is able to generate balanced and high-quality AC output voltages (as shown in Fig. 2) irrespective of the load condition. These expected voltages are equivalent to an equilateral triangle in the vector plane as

shown in Fig. 3, where the three outside lines represent line voltages V_{AB}, V_{BC} and V_{CA} and the three inside lines correspond to phase voltages V_{AO}, V_{BO}, and V_{CO}. It is found that there are only three independent lines within this triangle. In other words, if the position and length of three independent lines are determined, the rest of the lines in the triangle are automatically settled [8]. This indicates that the active control of any two line voltages and one-phase voltage can lead to the full control of a three-phase four-leg NPC inverter. Therefore, the circuit-level decoupling method for three-level NPC inverters proposed in [9], can then be extended to four-leg ones. As illustrated in Fig. 2, a line period can be divided into six regions. By inspecting the three-phase voltage waveforms in each region, one common fact is found that two phase voltages are always positive and the other one is negative in regions I, III and V (odd regions), whereas the opposite condition can be found in regions II, IV and VI (even regions). This fact leads to the thought of pulse width modulating the switches in the phases with same signs while keeping the switches in the other phase steady state for entire or part of the region. For this reason, in the odd regions, the following modulation method is used:

1) The lowest phase voltage along with its corresponding line voltages are selected as the active voltages under control.

2) The switches T_{i3} and T_{i4} (i=a, b, c) for the phase with lowest voltage are always turned on, and the corresponding T_{i1} and T_{i2} for this phase are always turned off.

3) The switches for the other two phases and also the neutral phase are controlled by SPWM scheme.

With this treatment, Fig. 1 is equivalent to Fig. 4(a) in region I, which can be further simplified and organized into Fig. 4 (b), where $S_{TLi(i=1,2,3)}$ is the equivalent single pole triple throw switch for each phase half bridge. The same equivalent circuit is also applicable to regions III and V.

While in even regions, the voltage waveforms in Fig. 2 have the same pattern and the following modulation method is used:

1) The highest phase voltage along with its corresponding line voltages are selected as the active voltages under control.

2) The switches T_{i1} and T_{i2} (i=a, b, c) for the phase with highest voltage are always turned on, and the corresponding T_{i3} and T_{i4} for this phase are always turned off.

3) The switches of the other two phases and also the neutral phase are controlled by SPWM scheme.

In region II, the four-leg inverter in Fig. 1 is equivalent to Fig. 5(a), and hereby the simplified circuit with the model of the single pole triple throw switch is obtained in Fig. 5(b). Similarly, the same equivalent circuit is applicable to regions IV and VI as well.

B. Operation Principle of the Equavilent Converters

For a further analysis on the operation principles, the following assumptions are made firstly: $L_A=L_B=L_C=L_x$, $C_A=C_B=C_C$ and the switching frequency is much higher than the fundamental frequency. In region I, it can be seen in Fig. 4 that $V_p=V_{AB}$, $V_n=V_{CB}$ and $V_x=V_{OB}$. Hereby, when $V_{m(m=p,n,x)} \geq E$, the corresponding switch $S_{TLm(m=p,n,x)}$ is switched between the switching nodes P and 0 with a duty cycle defined by $d_{m(m=p,n,x)}=T_{onP,m(m=p,n,x)}/T_s$, where $T_{onP,m(m=p,n,x)}$ is the connection time with the switch node P, and T_s is the switching period. According to the volt-second balance principle on inductors in

(a)

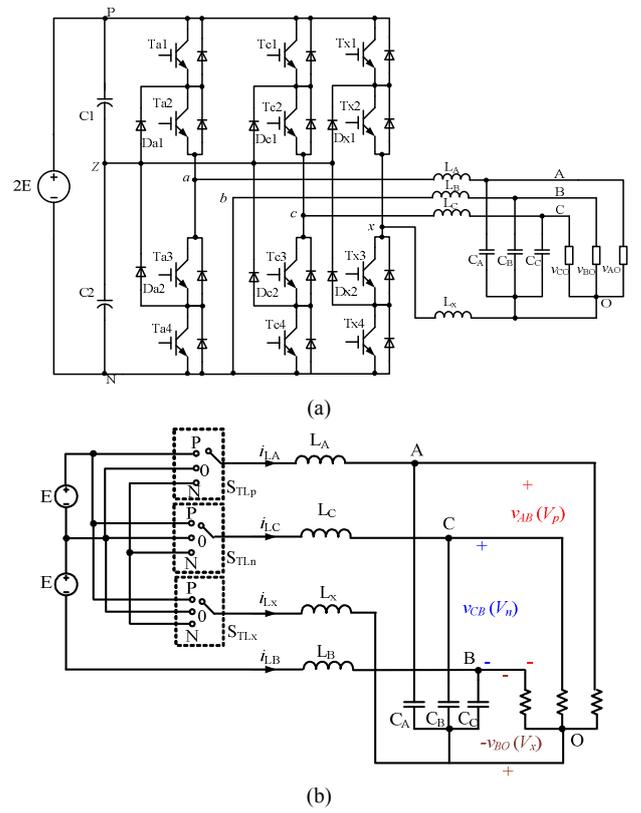
(b)

Figure 4.   Equivalent circuit of four-leg NPC inverter in region I.

(a)

(b)

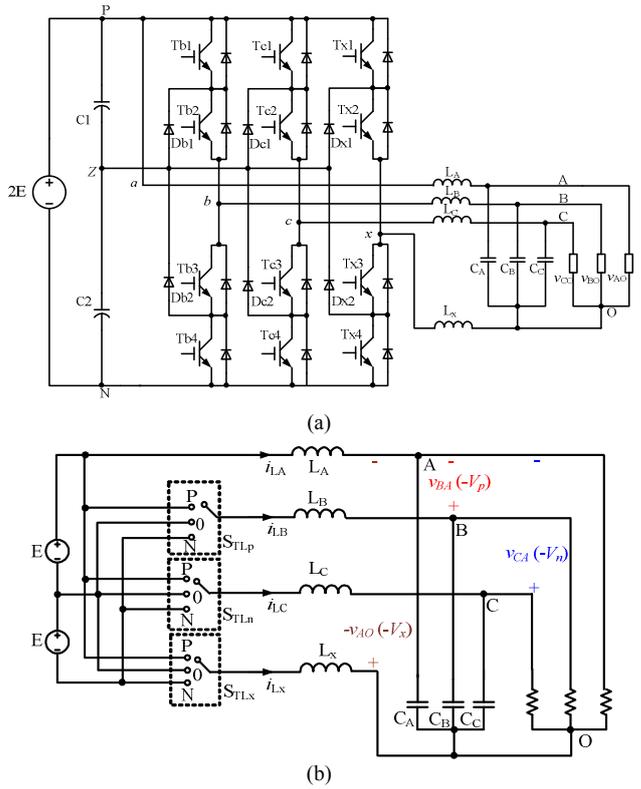Figure 5.   Equivalent circuit of four-leg NPC inverter in region II.

a whole switching period, the following equations can be derived,

$$(2E - V_p).d_p + (E - V_p).(1 - d_p) = 0 \qquad (1)$$

$$(2E - V_n).d_n + (E - V_p).(1 - d_n) = 0 \qquad (2)$$

$$(2E - V_x).d_x + (E - V_x).(1 - d_x) = 0 \qquad (3)$$

Then, the duty cycles are expressed

$$d_p = \frac{V_p - E}{E}; \quad d_n = \frac{V_n - E}{E}; \quad d_x = \frac{V_x - E}{E} \quad (4)$$

On the contrary, when $V_{m(m=p,n,x)} < E$, the corresponding switch $S_{TLm(m=p,n,x)}$ is switched between the switching nodes 0 and N with a duty cycle defined as $d'_{m(m=p,n,x)} = T_{on0,m(m=p,n,x)}/T_s$, where $T_{on0,m(m=p,n,x)}$ is the connection time with the switch node 0. According to the inductor volt-second balance in a whole switching period, the following equations can be derived,

$$(E - V_p).d'_p + (0 - V_p).(1 - d'_p) = 0 \quad (5)$$

$$(E - V_n).d'_n + (0 - V_n).(1 - d'_n) = 0 \quad (6)$$

$$(E - V_x).d'_x + (0 - V_x).(1 - d'_x) = 0 \quad (7)$$

Correspondingly, the duty cycles are expressed

$$d'_p = \frac{V_p}{E}; \quad d'_n = \frac{V_n}{E}; \quad d'_x = \frac{V_x}{E} \quad (8)$$

Hence, (4) and (8) constitute the relationship of three three-level Buck converters and to make this conclusion even clearer the equivalent circuit of phase leg a and the typical waveforms for V_{AB} (V_p) as an example are plotted in Fig. 6.

In region II, as shown in Fig. 5, the active line voltages and phase voltage are V_{BA} ($-V_p$), V_{BA} ($-V_n$) and V_{AO} ($-V_x$), respectively. Accordingly, if $-V_{m(m=p,n,x)} \leq -E$, the equivalent switch $S_{TLm(m=p,n,x)}$ will be switched between the terminals N and 0 with the duty cycle $d_{m(m=p,n,x)} = T_{onN,m(m=p,n,x)}/T_s$. Otherwise, if $-V_{m(m=p,n,x)} > -E$, $S_{TLm(m=p,n,x)}$ will be switched between the terminals 0 and P with the duty cycle $d_{m(m=p,n,x)} = T_{on0,m(m=p,n,x)}/T_s$. In order to obtain the steady state transfer functions from duty cycles to input/output voltages, the volt-second balance principle is adopted again, the same duty cycle descriptions as in region I can be obtained below.

$$\begin{cases} d_p = \dfrac{V_{BA} + E}{-E} = \dfrac{V_{AB} - E}{E} = \dfrac{V_p - E}{E} \\[2mm] d_n = \dfrac{V_{CA} + E}{-E} = \dfrac{V_{AC} - E}{E} = \dfrac{V_n - E}{E} \\[2mm] d_x = \dfrac{V_{OA} + E}{-E} = \dfrac{V_{AO} - E}{E} = \dfrac{V_x - E}{E} \end{cases} \quad (9)$$

$$\begin{cases} d'_p = \dfrac{V_{BA}}{-E} = \dfrac{V_{AB}}{E} = \dfrac{V_p}{E} \\[2mm] d'_n = \dfrac{V_{CA}}{-E} = \dfrac{V_{AC}}{E} = \dfrac{V_n}{E} \\[2mm] d'_n = \dfrac{V_{OA}}{-E} = \dfrac{V_{AO}}{E} = \dfrac{V_x}{E} \end{cases}, \quad (10)$$

It is clear that in region II the four-leg NPC inverter can also be decoupled into three three-level Buck converters. As an example, the equivalent circuit of phase leg b and the typical waveforms for the output voltage V_{BA} ($-V_p$) are plotted in Fig. 7 to present the decoupling effect.

Applying the same analysis to one entire fundamental cycle, the representation of the decoupled three-level Buck converters for the four-leg NPC inverter can be derived in every 60° region. Also, controller design and selection of the
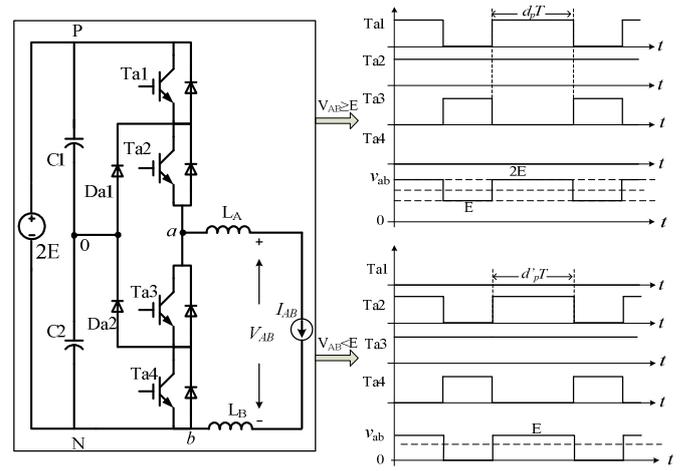

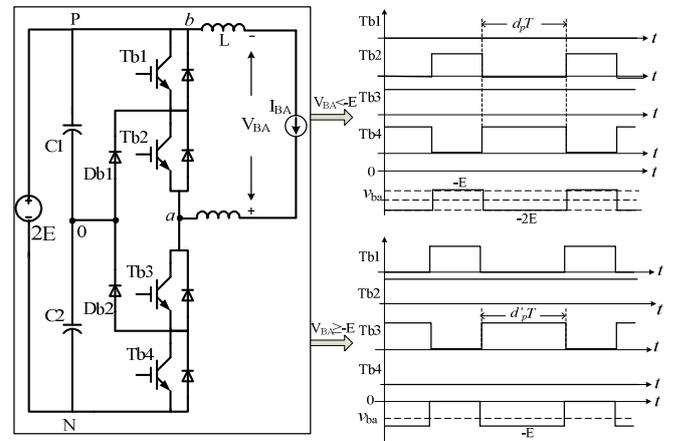Figure 6. Equivalent circuit, control strategy and typical waveforms for output voltage V_{AB} (V_p) in region I.

Figure 7. Equivalent circuit, control strategy and typical waveforms for output voltage V_{BA} ($-V_p$) in region II.

output filter parameters L and C can thereby follow the same rules as those for three-level DC-DC converters.

C. Average NP voltage self-balancing ability

The main technical challenge in any application of the NPC inverter is to maintain the voltages of the two DC-side capacitors equal and at a pre-specified level.

When the four-leg NPC inverter connects with the three-phase balanced load, i_{Lx} equals to zero, so it will not affect the NP voltage. Under this case, by inspecting references listed in Table I, it can be seen that in the adjacent two regions the control signals are always same, for instance, in regions I and II the line voltage V_{AB} is adopted as the signal CON$_p$. A so-called anode three-level Buck converter (A-TLBC) and a cathode three-level Buck converter (C-TLBC) can be obtained [10]. Furthermore, both of the three-level Buck converters can be combined into one converter with common input dividing capacitors. Thus, by rotating the energy provision burden between these capacitors through the adjacent operating regions, the two dividing capacitors will provide, on average, an equal amount of energy to the load, which allows them to maintain a balance voltage over time, thereby the voltage of the dividing capacitors can be balanced naturally, so any additional feedback or feed-forward control is not needed. Moreover, as the analyzed results in [9], the frequency of NP voltage ripple is 150 Hz.
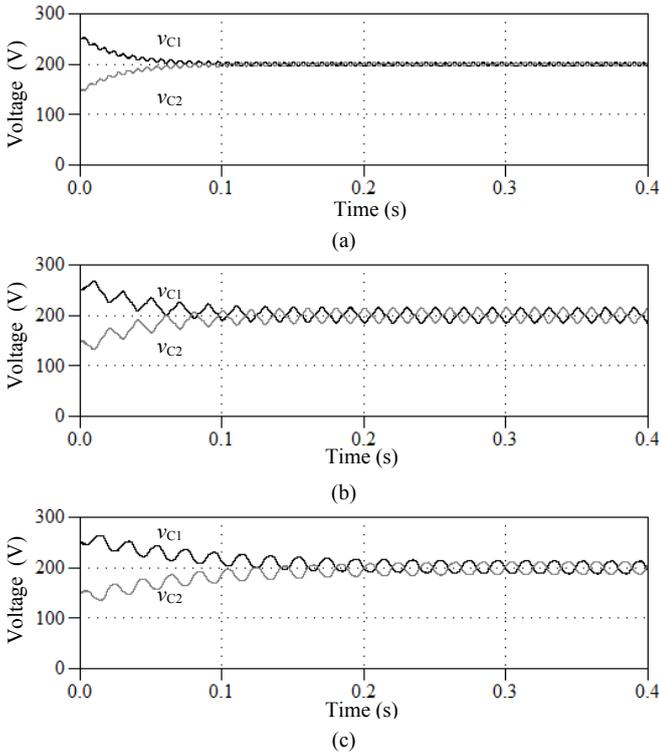
Figure 8. Simulated waveforms of DC-side voltage balancing. (a) with three-phase load, (b) with two-phase load, and (c) with only phase-C load.

When there is a load imbalance, the neutral current i_{Lx} will vary the NP voltage ripple frequency as well as the ripple magnitude. But the voltages of the two DC-side capacitors can still maintain equal, because the control signal of the neutral phase CON_x in the first half fundamental period has symmetrical phase voltage sequence with that in the second one, i.e. $-V_{BO}$, $-V_{AO}$, $-V_{CO}$ in the regions I, II, III, and V_{BO}, V_{AO}, V_{CO} in the regions IV, V, VI, respectively. Hence, the variation frequency of CON_x is 50 Hz and it can decide the NP voltage ripple frequency which is also 50 Hz. More detailed quantitive analysis on NP voltage variation and DC bus current ripple will not be presented in this paper.

To verify the analysis above, the four-leg NPC inverter is simulated by Matlab. The adopted simulation parameters are: Wye-connected resistive-inductive load $15\Omega/23mH$ per phase, 250VAC/50Hz output voltage, DC-side capacitors $C_1=C_2=1000\mu F$, and the initial voltages across C_1 and C_2 V_{C1}=250VDC and V_{C2}=150VDC, respectively. The transient waveforms of the DC-side voltage balancing are shown in Fig. 8 and the differences of those waveforms, such as shape, ripple frequency and magnitude, and transient time, can be observed clearly.

III. IMPLEMENTATION OF THE PROPOSED MODULATION STRATEGY

A. Implementation of Modulator

Fig. 9 shows the proposed modulator for the four-leg NPC inverter, which is responsible to determine the decouple logic and distribute the corresponding driving signals. It consists of a region selector, a carrier signal selector, a PWM generator and a gate signal distributor. If the feedback controller is designed, outputs of the designed controller (current and/or voltage signals) can be connected into the carrier signal selector. The region selector determines the active working region, as shown in Fig. 2, by detecting the zero-crossing point of the expected
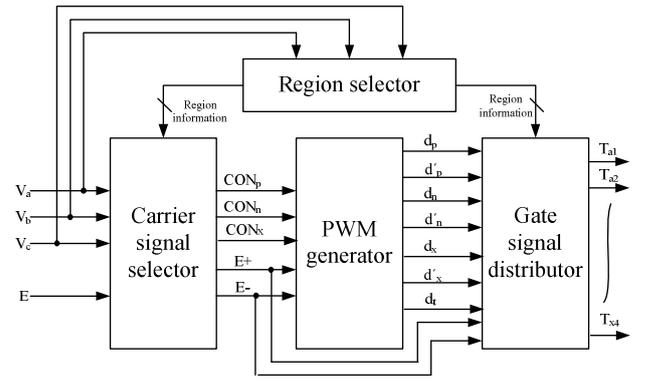

Figure 9. The block diagram of the proposed modulator.

TABLE I. SYNTHESIS OF THE DRIVING SIGNALS

Region Selector		Control Signal Selector			Gate Signal Distributer			
Regions		CON_p	CON_n	CON_x	d_p or d'_p	d_n or d'_n	d_x or d'_x	d_t
I	E^+	$V_{AB}-E$	$V_{CB}-E$	$-V_{BO}-E$	$d_p=T_{a1}$, $T_{a2}=1$	$d_n=T_{c1}$, $T_{c2}=1$	$d_x=T_{x1}$, $T_{x2}=1$	$T_{b3}=T_{b4}=1$
	E^-	V_{AB}	V_{CB}	$-V_{BO}$	$d_p=T_{a2}$, $T_{a1}=0$	$d_n=T_{c2}$, $T_{c1}=0$	$d_x=T_{x2}$, $T_{x1}=0$	
II	E^+	$V_{AB}-E$	$V_{AC}-E$	$V_{AO}-E$	$d_p=T_{b4}$, $T_{b3}=1$	$d_n=T_{c4}$, $T_{c3}=1$	$d_x=T_{x4}$, $T_{x3}=1$	$T_{a1}=T_{a2}=1$
	E^-	V_{AB}	V_{AC}	V_{AO}	$d_p=T_{b3}$, $T_{b4}=0$	$d_n=T_{c3}$, $T_{c4}=0$	$d_x=T_{x3}$, $T_{x4}=0$	
III	E^+	$V_{BC}-E$	$V_{AC}-E$	$-V_{CO}-E$	$d_p=T_{b1}$, $T_{b2}=1$	$d_n=T_{a1}$, $T_{a2}=1$	$d_x=T_{x1}$, $T_{x2}=1$	$T_{c3}=T_{c4}=1$
	E^-	V_{BC}	V_{AC}	$-V_{CO}$	$d_p=T_{b2}$, $T_{b1}=0$	$d_n=T_{a2}$, $T_{a1}=0$	$d_x=T_{x2}$, $T_{x1}=0$	
IV	E^+	$V_{BC}-E$	$V_{BA}-E$	$V_{BO}-E$	$d_p=T_{c4}$, $T_{c3}=1$	$d_n=T_{a4}$, $T_{a3}=1$	$d_x=T_{x4}$, $T_{x3}=1$	$T_{b1}=T_{b1}=1$
	E^-	V_{BC}	V_{BA}	V_{BO}	$d_p=T_{c3}$, $T_{c4}=0$	$d_n=T_{a3}$, $T_{a4}=0$	$d_x=T_{x3}$, $T_{x4}=0$	
V	E^+	$V_{CA}-E$	$V_{BA}-E$	$-V_{AO}-E$	$d_p=T_{c1}$, $T_{c2}=1$	$d_n=T_{b1}$, $T_{b2}=1$	$d_x=T_{x1}$, $T_{x2}=1$	$T_{a3}=T_{a4}=1$
	E^-	V_{CA}	V_{BA}	$-V_{AO}$	$d_p=T_{c2}$, $T_{c1}=0$	$d_n=T_{b2}$, $T_{b1}=0$	$d_x=T_{x2}$, $T_{x1}=0$	
VI	E^+	$V_{CA}-E$	$V_{CB}-E$	$V_{CO}-E$	$d_p=T_{a4}$, $T_{a3}=1$	$d_n=T_{b4}$, $T_{b3}=1$	$d_x=T_{x4}$, $T_{x3}=1$	$T_{c1}=T_{c2}=1$
	E^-	V_{CA}	V_{CB}	V_{CO}	$d_p=T_{a3}$, $T_{a4}=0$	$d_n=T_{b3}$, $T_{b4}=0$	$d_x=T_{x3}$, $T_{x4}=0$	

output AC voltages. The carrier signal selector selects the active control signals (modulation reference waves), which are represented by CON_p, CON_n and CON_x. Moreover, it also selects the switching position signal E^+ or E^-, which indicates that the half of DC bus voltage E is larger or smaller than the corresponding output line voltage. The selected control and reference signals are processed by the PWM generator to generate the duty-ratio signals. The gate signal distributor sends these duty-ratio signals to the gate driver circuits in order to trigger the appropriate switches of the sixteen transistors $T_{a1} \sim T_{c4}$ and $T_{x1} \sim T_{x4}$ according to the information from the region selector and the carrier signal selector. In Table I, the selected line voltages that act as outputs of the equivalent decoupled circuits in every region are listed, which also depends on the switching-position signals; the assignment of duty cycles of the active switches i.e. d_p, d'_p, d_n, d'_n, d_x, d'_x, is listed in Table I as well; d_t, which equals 1, is allocated to the switch that is always on in the inactive phase.

Comparing to the 3D-SVM-based modulator, the modulator proposed in this paper can be even implemented by a simple logic and an analogue circuit. The algorithm of modulator is simple and thereby it can be processed very quickly. As for the closed-loop controller design, the design methods for three-level DC-DC converters can be utilized easily to implement output voltage control of the four-leg NPC inverter due to the circuit decoupling concept, and thereby a high-speed DSP accompanied with a high sampling-rate A/D converter to achieve coordinate transformation is no more needed.
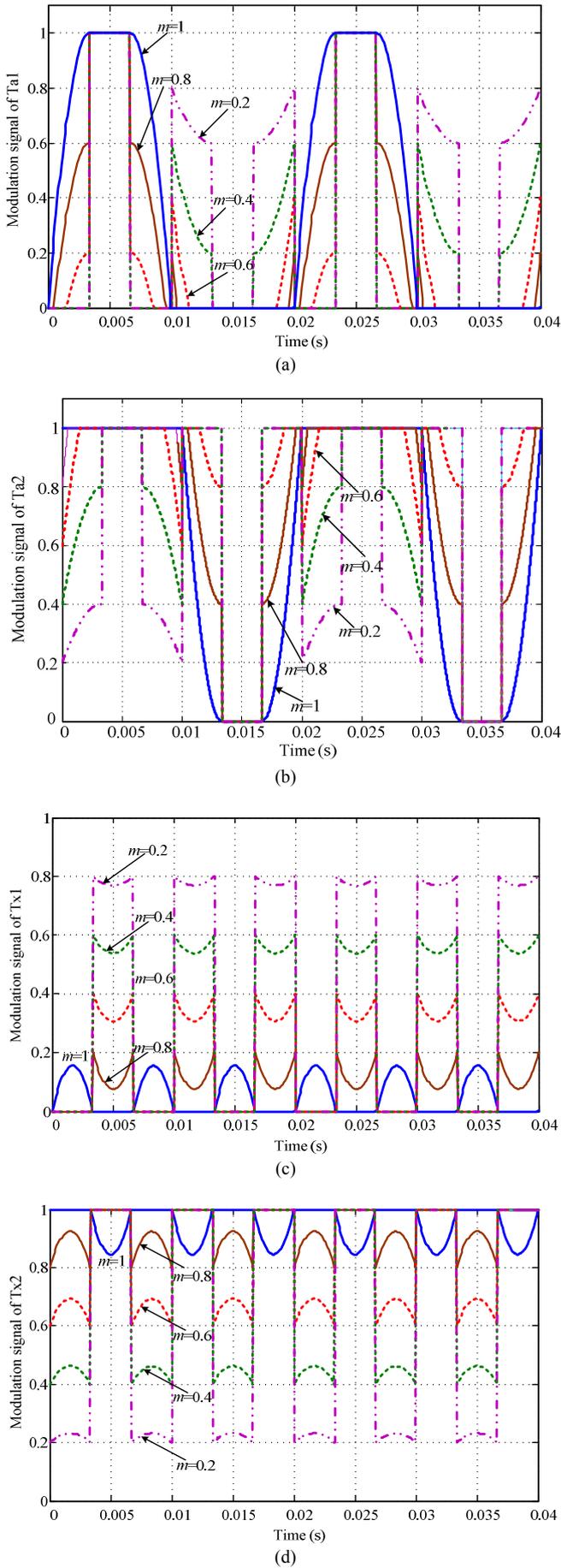
Figure 10. Modulation signals of T_{a1}, T_{a2}, T_{x1} and T_{x2} with difference modulation indices.

B. Analysis of Modulation Signals

From (4), (8), (9) and (10), and the control signals listed in Table I, it can be found that the modulation references are always line voltages for the switches in the legs a, b and c, and phase voltages for the switches in the fourth leg x. At the limit, $d_p=1$ or $d_n=1$, the maximal output line voltage is to be $2E$, which means the maximal amplitude-modulation ratio is:

$$m_{max} = \frac{v_{l-l}}{\sqrt{3} \cdot E} = \frac{2 \cdot E}{\sqrt{3} \cdot E} = \frac{2}{\sqrt{3}} = 1.1547 \qquad (11)$$

Therefore, (11) shows the maximum modulation index that is achievable for the linear-modulation mode by the proposed strategy. This maximal value is also obtained by 3D-SVMs or by other carrier-based PWM strategies with a proper zero-sequence signal injection. The aftermentioned modulation index m in this paper is expressed by normalizing with respect to this maximum value m_{max}.

Fig. 10, illustrates the modulation signals for switches T_{a1}, T_{a2}, T_{x1}, and T_{x2} in the phase legs a and x, for different modulation indices. It is clear that (1) line voltages are used as the modulation references for T_{a1} and T_{a2}, and phase voltages are applied as references for T_{x1} and T_{x2} ; (2) T_{a1} and T_{a2} have no switching actions in regions II and V; (3) modulation signals are within the range [0, 1], so all the references can share one common carrier wave. Hence, the modulation signals for the switches located in phase legs b and c can be obtained by ±120° phase-shifting with respect to the modulation signals of phase leg a, respectively. While complicated in shape, since the equations describing the functions are relatively simple sections of sinusoids, they can be readily implemented in real-time digital form.

C. Implementation of Closed-Loop Control

In this paper, the modulator and closed-loop controller are implemented digitally by a TMS320F28335 eZdsp. The system closed loop control block diagram has been presented in Fig.11. According to system performance, control variables are the three-phase output voltages (V_{abc}). The control is performed in the synchronous rotating frame which converts measured AC values into the DC ones. This allows the use of conventional Proportional-Integral (PI) controllers achieving zero steady state error. According to Fig.11, the reference voltages ($V_{abc}*$) along with the measured output voltages (V_{abcf}) are converted into $V_{qd}*$ and V_{qdf} respectively. Comparing the reference and actual values of the converted voltages, the error signals are generated. The generated error signals are passed through PI controllers and the required V_{qd} values are obtained. Converting these values to V_{abc} voltages, proper signals for the carrier signal selector block (Fig.8) are produced.
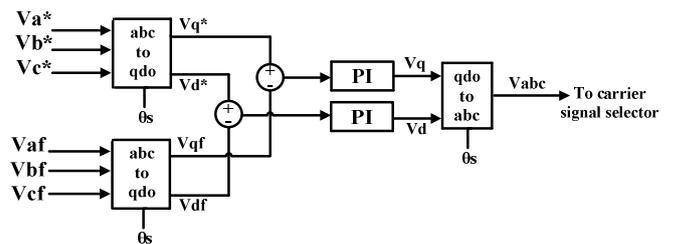

Figure 11. Block diagram of system closed loop control.

IV. EXPERIMENTAL VERIFICATION

The proposed modulation technique has been verified by experiment from a prototype built in the lab. The parameters for the prototype are listed in Table II. The converter operates over both a Wye-connected resistive load and a nonlinear load.

TABLE II. PARAMETERS OF THE EXPERIMENT

Output power	1.5 kW
Output fundamental frequency	50 Hz
DC bus voltage	250 V DC
Switching frequency	20 kHz
Output low-pass LC filter	L_A=L_B=L_C=120 μH, C_A=C_B=C_C=40 μF
Digital signal processor	TMS320F28335 eZdsp

Fig. 12 shows the experimental results when the prototype is tested with balanced resistive load and the modulation index is 0.8. The output phase voltage, the output line voltage and the three phase sinusoidal output voltages are depicted in Fig. 12 (a), (b) and (c), respectively. It can be seen that there are no switching actions in phase leg a during the operating regions II and IV.

Fig.13 (a) and (b) present the closed-loop controlled prototype's response with the proposed modulation strategy, when it is tested under balanced and unbalanced resistive load. The top one of the waveforms is output voltage v_{BO}, while the bottom three waveforms are three phase load currents i_A, i_B and i_C. Fig.13 (a) shows the prototype's response when the load is unbalanced with two-phase load (phase B disconnected) and Fig.13 (b) shows its response with one phase load (phases B and C are disconnected). In both of the cases, the output voltage waveform demonstrates a high-quality sinusoidal shape.
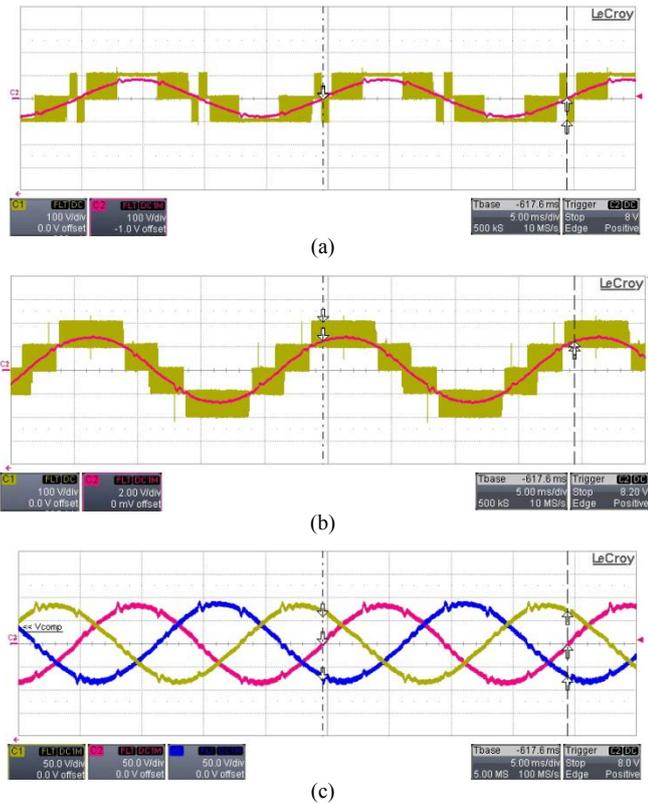

(a)

(b)

(c)

Figure 12. Experimental results with balanced resistive load (a) output phase voltage v_{az} and v_{AO} [100 V/div], (b) ouput line voltage v_{ab} and v_{AB} [100 V/div] and (c) output three-phase voltages v_{AO}, v_{BO} and v_{CO} [50 V/div]. (Time base: 5 ms/div)
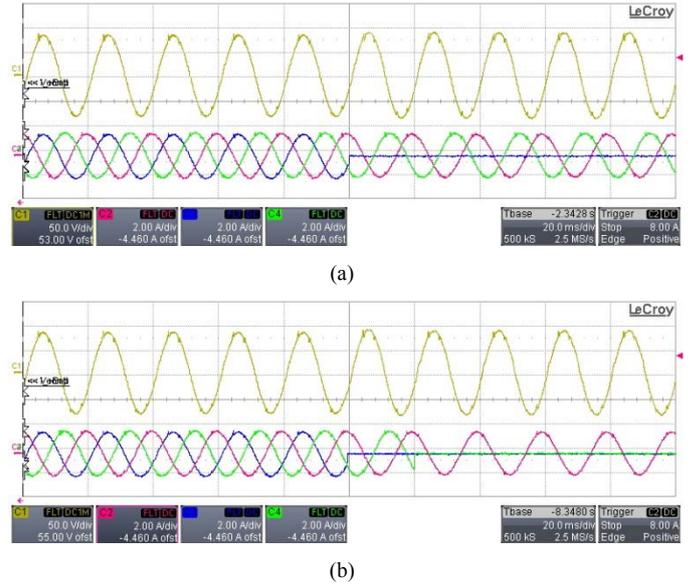

(a)

(b)

Figure 13. Experimental results of output voltage (v_{BO}, [50 V/div]) and currents (i_A, i_B, i_C, 2 A/div) with unbalanced resistive load (a) with two-phase load and (b) with only one phase load. (Time base: 20 ms/div).
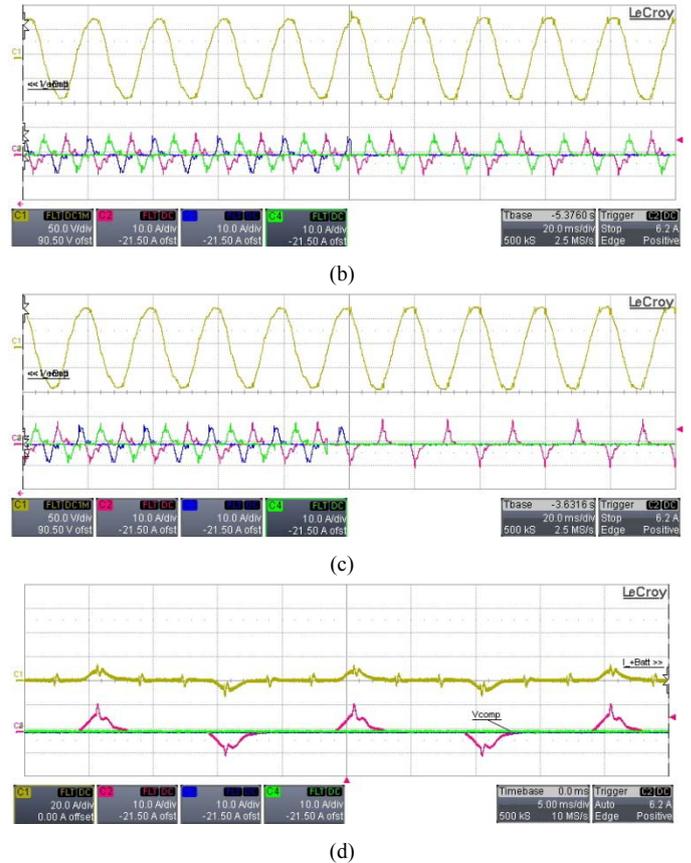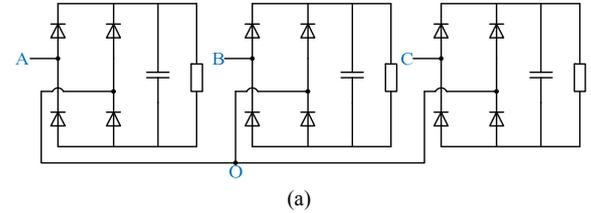

(a)

(b)

(c)

(d)

Figure 14. Experimental results of output voltage (v_{BO}, [50 V/div]) and currents (i_A, i_B, i_C, 10 A/div, i_X 20 A/div) when the prototype tested under single-phase nonlinear load. (a) Circuit of single phase nonlinear load, (b) with two-phase load (phase B disconnected), (c) with one phase load (both phase B and phase C disconnected), and (d) currents i_A and i_X with one phase load (phase B and phase C disconnected). (Time bases: 20 ms/div for (b) and (c), 5 ms/div for (d)).

Fig.14 (a)-(d) proves the prototype's unbalanced and nonlinear load handling capability with proposed modulation strategy under closed-loop control. The three single phase nonlinear load adopted in the experiment is presented in Fig.14 (a), which is realized by diode rectifiers followed by parallel-connected resistors and 330 μF/400V capacitors. Each load is connected between one of the output phase terminals A, B, C, and the neutral terminal O. In the Fig.14 (b) and (c) are the phase output voltage v_{BO} and output currents i_A, i_B, i_C, and in Fig.14 (d) depict output currents i_A and neutral current i_X. Fig.14 (b) shows the experimental results with two-phase nonlinear load and the other phase open, and Fig.14 (c) presents the experimental results with one phase nonlinear load and the other two phases open. It explores that the prototype with the proposed modulation strategy is to be unaffected by not only nonlinear but also unbalanced loading situation. In Fig. 14 (d), it is clear that the unbalanced current between the output phases flows through the fourth leg of the NPC inverter.

V. CONCLUSION

This paper has introduced a simple and fast-processing PWM modulation strategy for the three-phase four-leg NPC inverter. The proposed strategy employs a circuit-level decoupling method and is able to decouple the power train into three three-level Buck converters in every 60° region.

The proposed modulation strategy for the four-leg NPC inverter has following advantages.

(1) *Fast-processing*: the structure of modulator is simple and the algorithm can be implemented easily, and only one carrier signal is needed;

(2) *Average NP voltage self-balancing*: it can keep the NP voltage at one half of the DC-link voltage without any feedback or feed-forward control;

(3) *Excellent load handling capability*: it can generate balanced high-quality output voltage waveforms with all sorts of balanced/unbalanced as well as linear/nonlinear loads;

(4) *Low switching losses*: The switching loss is reduced significantly by not switching the phases which have the highest or lowest voltages, and also two of the switches in the fourth-leg are not operated with the switching frequency.

The experimental results measured on the prototype built in the lab are provided to support the theoretical analysis and verify the proposed concept. In addition, this decoupling concept can be extended and utilized in other multilevel (5-level, 7-level…) inverters or active PWM rectifiers.

While the main drawback of the proposed modulation scheme is that the THD of output voltage and current waveforms, which will varies with the modulation index, is worse when modulation indices are lower, like the conventional discontinuous SPWM modulation schemes. This feature will be studied in depth and reported in the future papers.

REFERENCES

[1] A. Nabae, I. Takahashi and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Transactions on Industrial Applications,* vol. 1A-17, no. 5, pp. 518-523, Step.-Oct. 1981.

[2] J. Rodriguez, S. Bernet, P. K. Steimer and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Transactions on Industrial Electronics,* vol. 57, no. 7, pp. 2219-2230, 2010.

[3] J. Rodriguez, B. Wu, M. Rivera, A. Wilson, V. Yaramasu and ch. Rojas, "Model Predictive Control of Three-Phase Four-Leg Neutral-Point-Clamped Inverters," *in International Power Electronics Conference,* 2010, pp.3112-3116.

[4] J. Yao and T. Green, "Three-Dimensional Space Vector Modulation for a Four-Leg Three-Level Inverter," *in IEEE European Conf. on Power Electronics and Applications*, 2005, pp. 1-9.

[5] S. Ceballos, J. Pou, E. Robles, J. Zaragoza, P. Ibanez and J. L. Martin, "Fault Tolerant Hybrid Four-Leg Multilevel Converter," *in IEEE European Conf. on Power Electronics and Applications,* 2007, pp. 1-9.

[6] S. Ceballos, J. Pou, J. Zaragoza, J. L. Martin, E. Robles, I. Gabiola and P. Ibanez, "Efficient Modulation Technique for a Four-Leg Fault Tolerant Neutral-Point-Clamped Inverter," *IEEE Transactions on Industrial Electronics,* vol. 55, no. 3, pp. 1067-1074, Mar. 2008.

[7] N. Dai, M. Wong and Y. Han, "Application of a Three-Level NPC Inverter as a Three-Phase Four-Wire Power Quality Compensator by Generalized 3DSVM," *IEEE Transactions on Power Electronics,* vol. 21, no. 2, pp. 440-449, Mar. 2006.

[8] L. Li and K. M. Smedley, "A new analog controller for three-phase four-wire voltage generation inverter," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1711-1721, 2009.

[9] Z. Zhang, O. C. Thomsen and M. A. E. Andersen, "The circuit level decoupling modulation strategy for three-level neutral-point-clamped (TL-NPC) inverter," *in European Conference on Power Electronics and Applications,* 2011, pp.1-10.

[10] X. Ruan, B. Lin, Q. Chen, S.-C. Tan and C. K. Tse, "Fundamental considerations of three-Level dc-dc converters: topologies, analysis, and control," *IEEE Transactions on Power Electronics,* vol. 55, no. 11, pp. 3733-3743, 2008.