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Superconductor-Semiconductor-Superconductor Planar Junctions of Aluminium on δ-doped Gallium-Arsenide

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Abstract - **We have fabricated and characterized planar superconductor-semiconductor-superconductor (S-Sm-S) junctions with a high quality (i.e. low barrier) interface between an n^{++} modulation doped conduction layer in MBE grown GaAs and *in situ* deposited Al electrodes. The Schottky barrier at the S-Sm interface was compensated by inserting several Si δ-doped layers above the conduction layer and close to the surface of the GaAs heterostructure. Below 1.2 K, the transition temperature of Al, the dc I-V curves of such S-Sm-S junctions with a wide and short GaAs channel exhibited the classic features of S-N-S junctions including subharmonic energy gap structure (SGS) and excess current (EC) due to Andreev reflections at the interfaces.**

I. Introduction

The motivation for the work reported here is on one hand of a technological nature: the development of superconducting field-effect transistors (SUPRAFETs or JOFETs) based on fast semiconductor materials, e.g. GaAs/AlGaAs heterostructures and on the other hand oriented towards gaining a better understanding of the fundamental transport properties of S-Sm-S structures, including a determination of the characteristic length and time scales.

For hybrid S-Sm structures is it a fundamental technological problem to fabricate low resistance S-Sm contacts, i.e. high transparency contacts between the superconducting metal and the semiconductor material forming the channel. As a rule, a Schottky barrier is formed between a metal with a high Fermi energy, E_F, and the semiconductor with a low E_F. In this paper we demonstrate how the inclusion of heavily Si-doped monolayers in the MBE-grown GaAs crystal (δ-doped layers) just below the semiconductor surface results in a drastic reduction in the interface resistance by a factor of 2000 or more. A clean S-Sm interface is obtained by depositing the Al layer *in situ* on the freshly grown GaAs. The measured transparency, $T(E_F)$, is of the order of 50 %, i.e. an electron at E_F incident on the GaAs-Al interface has a 50 % chance of being transmitted into the superconductor.

For $T < T_c$ (Al) = 1.20 K we have measured the I-V characteristics of planar S-Sm-S junctions with varying distance, L, between the superconducting electrodes. The I-V curves exhibit *excess current (EC)* at high voltage ($V > 2\Delta/e$) and the differential resistance (dV/dI) vs. V curves exhibit the well-known *subharmonic energy gap structure (SGS)* at $V = 2\Delta/ne$ where Δ is the superconducting gap in Al. Both features stem from Andreev reflections at the GaAs/Al interfaces. From the EC we calculate the interface transparency. The SGS is a signature of correlated electron-like and hole-like quasiparticles that undergo Andreev reflections at the Sm-S interfaces. From such data we have determined the characteristic length for the diffusive but correlated electron-hole quasiparticle transport phenomena through the junction to be of the order of the phase-breaking diffusion length, ℓ_ϕ, in GaAs (about 3 μm at 0.3 K). Down to a temperature of 0.3 K no supercurrent was observed in junctions with L down to 1.1 μm.

II. The S-Sm-S Junction

Recently, the fabrication and study of superconductor-semiconductor-superconductor (S-Sm-S) junctions have gained increasing interest. For applications, the main part of the work reported has been aimed at developing three terminal superconducting junctions in which electric field effect in the semiconductor channel can be used to control the conductance and the critical value of the supercurrent between the closely spaced superconducting electrodes [1]. A supercurrent can flow if the separation between the superconductors is smaller than the coherence length in the semiconductor, ξ, and if the S-Sm interfaces are highly transparent.

In parallel with these efforts, there has also been a growing interest in the fundamental aspects of equilibrium and transport phenomena in mesoscopic (phase-correlated) normal metal conductors (N) or semiconductors connected to superconductors [2-11]. The description of the well-known (static) proximity effect can be extended to the dynamic (non-equilibrium) case of charge transport across an S-N interface where the microscopic picture is based on the Andreev reflection, by which an electron (hole) in the N-region is transmitted into the S-region as part of a Cooper pair while a

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hole (electron) is retro-reflected along the time-reversed path of the incoming particle [12]. For an S-N interface this leads to an increased conductance which is seen as the socalled excess current at high voltage bias ($V > \Delta/e$). It may be assumed that the same theoretical model applies to a S-Sm interface with a highly transparent interface.

Our S-Sm-S junctions may be modelled as two S-N junctions back-to-back with some dirty normal metal (degenerate semiconductor) in between. Provided the separation, L, between the two interfaces is smaller than the phase-breaking length in the semiconductor, ℓ_ϕ, interference effects arise for charge carriers Andreev reflected from the two interfaces. Such phase-coherent interference effects are seen as changes in the zero-bias differential resistance of the junction as a function of energy. The diffusion length, $\ell_\phi = (D\tau_\phi)^{1/2}$, sets the limit for the phase-correlated (energy conserving) traversals of electrons and holes across the junction. Here D is the diffusion constant: $D = v_F(N)\ell/3$ (in 3-dim.), ℓ is the mean free path and τ_ϕ is the phase-breaking time. In the dirty limit, the coherence length in the N-region, $\xi = (hD/4\pi^2 k_B T)^{1/2}$, is much longer than the mean free path. Since in GaAs this time is simply the inelastic relaxation time, τ_E, the phase-coherent effects at zero bias co-exist with the energy-conserving multiple Andreev reflections which give rise to the SGS at $V = 2\Delta/en$, ($n = 1,2,3,...$), a series of minima in the differential resistance vs. voltage curve.

The Andreev reflection probability at an N-S interface may be derived from a dimensionless interface scattering parameter, Z, which also enters into the expression for the normal state resistance of an N-S interface: $R_N = R\,(1 + Z^2)$ (the BTK-model, [13]). R is the barrierless resistance and Z is the effective strength of the interface scattering: in a model with a δ-function barrier of strength H, Z is given by: $Z = (Z_o + (1-r^2)/4r)^{1/2}$ with $Z_o = 2\pi H/hv_F$ and $r = v_F(N)/v_F(S)$. As seen, a mismatch between the Fermi velocities, $v_F(N)$ and $v_F(S)$, in the N and the S regions contributes to the effective interface scattering strength, Z. Naturally, a low Z value corresponds to a high probability of Andreev reflection at the N-S (or Sm-S) interface, i.e. a high transparency of the interface, $T = (1 + Z^2)^{-1}$ [13]. Z is also directly related to the magnitude of the excess current and the strength of the SGS [14,15].

Recently, most research groups working on S-Sm-S junctions have chosen III-V semiconductor compounds. The material of choice has been highly doped InAs due to the ability of this material to form very low interface barriers with most metals deposited on the surface. On the surface of p-type InAs a 2-dim. electron gas (2DEG) inversion layer is formed, but unfortunately with a rather low mobility. More advanced III-V compound heterostructures like InAs-AlSb quantum wells [16] and gated devices based on buried channels in InAs-InGaAs [17] have been used. Also the use of backgated n-type InGaAs grown on p-type InP substrates have been demonstrated [18]. Another approach has been the use of annealed Ti/Sn contacts to GaAs/AlGaAs heterostructures containing a 2DEG below the surface [19]. All these devices, however, rely on rather involved processing procedures. High interface transparency and long ℓ_ϕ require both a high doping level and a high carrier mobility in the semiconductor channel. These two requirements are not easily fulfilled at the same time and a compromise is found. We have developed a new and simple method for fabricating planar S-Sm-S devices based on Al and Si-doped GaAs with very high contact transparency and a reasonably long ℓ_ϕ. From a technological point of view GaAs is the most studied III-V compound and molecular beam epitaxy (MBE) systems with Ga, As, Al and Si sources are installed in many research laboratories.

III Experimental technique and results

The Sm channel material of the S-Sm-S junction was 200 nm thick GaAs grown in a VARIAN MBE chamber on an undoped GaAs substrate. The 200 nm GaAs was doped with Si to 4.4×10^{18} cm^{-3} and capped with five δ-doped layers separated by 2.5 nm of undoped GaAs. Each of the δ-doped (mono)layers contained 5×10^{13} Si atoms per cm^2. The purpose of these layers was to decrease the Schottky barrier at the semiconductor-metal interface which was formed by depositing 200 nm of Al after the substrate temperature had been lowered to 30° C (to mimimize the formation of AlAs/AlGa compounds at the interface). As seen from Fig. 1 the δ-doped layers had a dramatic effect on the interface resistance corresponding to a reduction of the contact resistivity from 1×10^{-7} Ωm^2 to about $0.5 \times 10^{-10} \Omega\, m^2$, i.e. two orders of magnitude decrease in interface resistance for this particular geometry and three orders of magnitude reduction in contact resistivity. In upper panel of Fig.1 we have sketched how the conduction energy band edge in principle may look like for the structure with and without the δ-doped layers.

The S-Sm-S junctions were fabricated in the following way: First a 17 μm wide mesa structure was etched in the Al/GaAs layers and Ti/Au bonding pads were deposited. Secondly, a narrow stripe of width L (from 1 to 5 μm) was etched in the Al layer across the mesa. For this second step we used conventional electron beam lithography in PMMA resist and the Al thin film was wet etched in H_3PO_4:H_2O (1:2) at 50° C for about 2 min (see ref. 20 for further details).

The I-V and dV/dI vs. V characteristics were measured simultaneously by a phase sensitive detection technique with an AC voltage level much smaller than the thermal flutuation level: $V_{rms} << k_B T/e$. Most of the measurements were carried out in a conventional pumped ^3He cryostat with a base temperature of 0.3 K.

The two terminal resistance of the final planar S-Sm-S structure was dominated by the resistance of the oxide barriers between the Al and the Ti/Au layers. The four terminal resistance, however, only probed the L long and 17 μm wide Al-GaAs-Al structure in series with the S-Sm contacts (the distance between the voltage probes was 100 μm). On other samples from the same MBE-grown wafer, the Al thin film

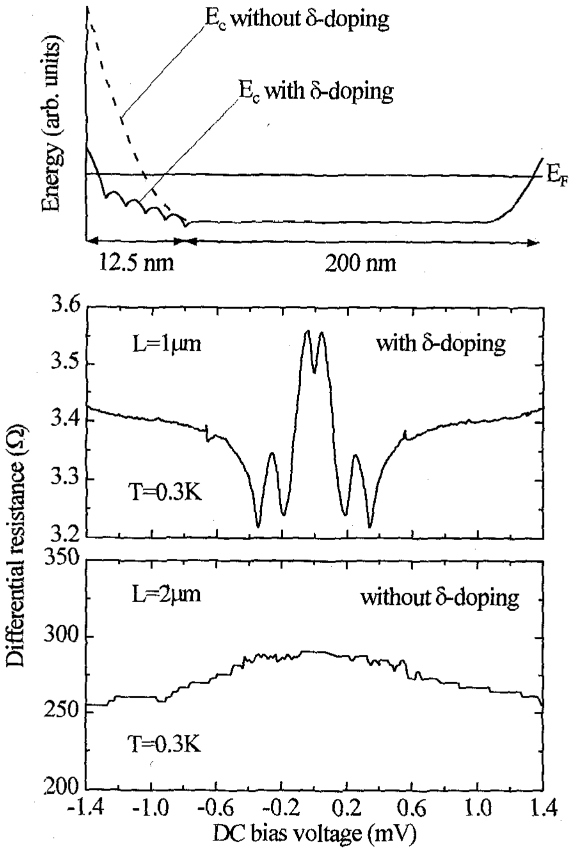

Fig.1. Upper panel: Energy vs. distance diagram showing in principle the position of the conduction band edge, E_c, and the Fermi energy level, E_F, for the GaAs channel of total thickness 212.5 nm with and without δ-doping. The two lower panels present the measured effect of the δ-doping: Differential resistance, dV/dI, vs. voltage, V, measured at 0.3 K for two Al/GaAs/Al junctions with and without the δ-doped layers.

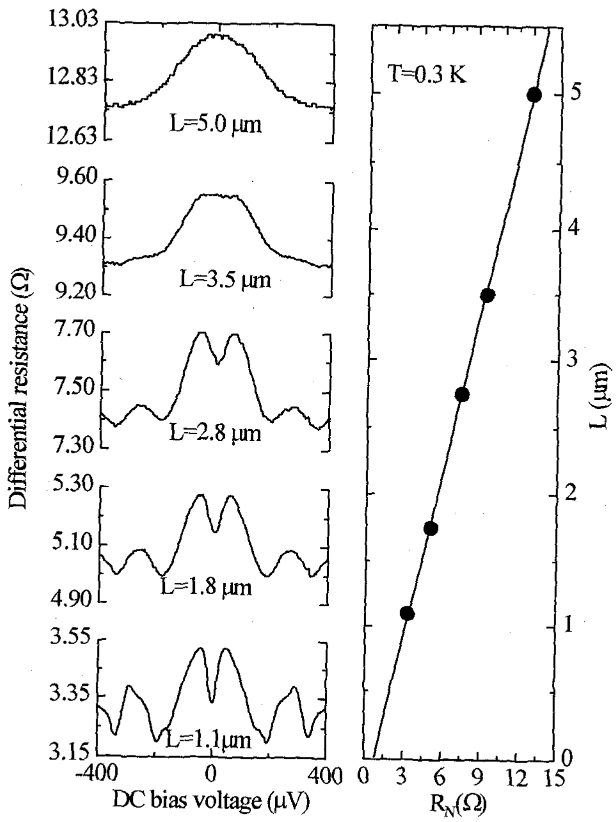

Fig. 2. Result of Transmission Line Measurements (TLM) at 0.3 K on five Al/GaAs/Al junctions with various length, L , and constant width and thickness of the GaAs channel (W x d = 17 x 0.2 μm^2).

Right panel: Plot of L vs R_N where R_N is the differential resistance at high bias voltage ($V > 2\Delta/e$). The slope of the straight line gives the characteristic conductance of the GaAs channel, while the X-axis intercept gives twice the contact resistance between Al and GaAs.

Left panel: Differential resistance, dV/dI, vs. voltage, V. The subharmonic energy gap structure (SGS) and the zero bias dip are clearly seen.

was completely removed in order to assess the GaAs conductive layer. The characterization included weak localization measurements, which on the basis of the well established theory by Hikami et al. [21] yielded the phase breaking length, ℓ_ϕ.

The low temperature mobility of the GaAs conductive layer was $\mu_e = 0.13\ m^2/Vs$ and the carrier density $n_e = 4.8 \times 10^{24}\ m^{-3}$, corresponding to a mean free path $\ell = 50$ nm and a diffusion constant $D = 0.016\ m^2/s$. The Al thin film had a critical temperature $T_c = 1.2$ K, close to the bulk value. By using the transmission line method on samples with varying separation between the Al electrodes we determined the specific contact resistivity ρ_N both above and below T_c. As mentioned above, for the δ-doped samples we found $\rho_c(T>Tc) = 53 \times 10^{-12}\ \Omega\ m^2$ in the normal state. At the Al/GaAs interface in the planar geometry current flows from the highly conductive Al layer to the more resistive GaAs layer over a typical decay length $\ell_c(T>T_c) = (d\rho_c/\rho_{GaAs})^{1/2} = 0.9\ \mu m$ where d and ρ_{GaAs} are the thickness and resistivity of the GaAs layer, respectively [20] (this decay length is the reason why the contact resistance and the contact resistivity do not scale.) For $T < T_c$ we found the decay length to be $\ell_c(T<T_c) = 0.15\ \mu m$ and $\rho_c(T<Tc) = w^2 dR_o^2/4\rho_{GaAs} = 1.0 \times 10^{-12}\ \Omega\ m^2$, where R_o is the intercept on the R_N vs. L plot shown in Fig. 2. R_N is the differential resistance measured at high voltage bias for $T < T_c$.

At 0.3 K the calculated coherence length in the GaAs region was 0.25 μm, at 25 mK 850 nm. With L down to 1.1 μm no supercurrent was observed in the junctions down to 0.3 K. Fig. 2 presents the experimental dV/dI vs. V curves at 0.3 K for five samples from the same wafer with L varying from 5.0 to 1.1 μm. As seen the characteristic length for the observation of the phase-correlated SGS is around 3 μm at 0.3 K. This is in good agreement with the weak localization measurements which showed that with decreasing temperature the phase breaking length, ℓ_ϕ, increased from 2 μm at 1.2 K

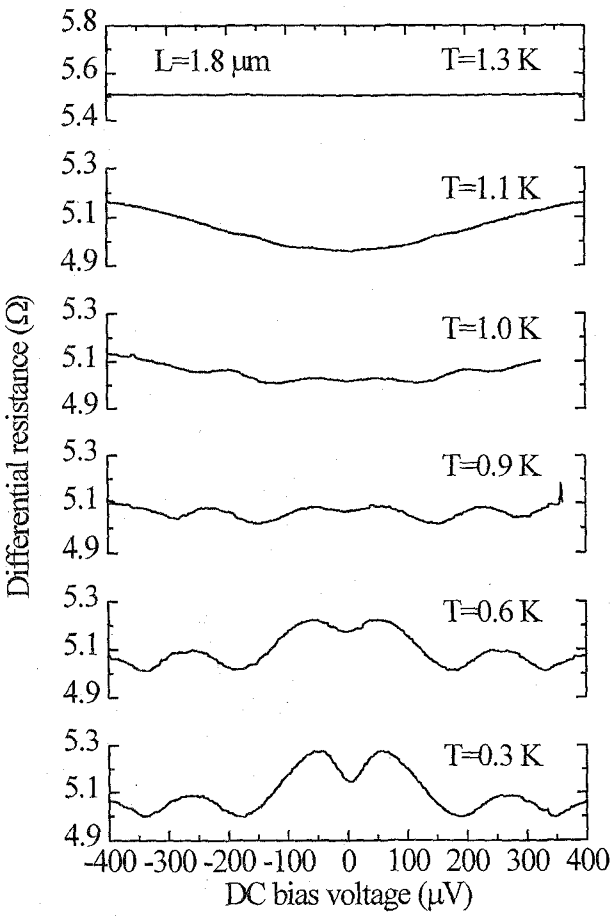

Fig. 3. Temperature dependence of the dV/dI vs. V curves for a Al/GaAs/Al junction with channel length, L = 1.8 μm. T_c(Al) = 1.2 K.

to 2.8 μm at 0.3 K. In Fig. 3 the temperature variation of the SGS is shown for a sample with L = 1.8 μm. As seen the SGS minima in the dV/dI vs. V curves fall at $V = \pm 2\Delta/ne$, with n = 1 and 2 and with $\Delta(T \ll T_c) = 175$ μeV, the value of the superconducting energy gap in bulk Al. We note that the strength of the SGS and the zero bias dip vary in the same way with temperature. We may conclude that the SGS and the zero bias dip are only observed when $L < \ell_\phi(T)$.

The experimental values of Z (as deduced from the excess current measured for $V > 2\Delta/e$) fell in the range between 0.7 and 1, equivalent to a high transparency of the Al/GaAs interface: T = 70-50 %. Theoretically, the minimum value of Z is 0.4, as calculated from the mismatch between the Fermi velocities in the two materials and setting the barrier height H = 0. With Z = 1 and with the density of states at E_F in the doped GaAs $N(0) = 3n_e/2E_F = 2.47 \times 10^{44}$ $m^{-3}J^{-1}$, the ideal, theoretical value of $\rho_c(T<Tc)$ based on the BTK-model is $\rho_c(T<Tc) = (1 + 2Z^2)/2N(0)e^2v_F = 0.35 \times 10^{-12}$ Ω m^2, a value only a factor of 3 smaller than the measured value of 1.0×10^{-12} Ω m^2. This shows that the Al/GaAs/Al junctions investigated here are spatially very homogeneous (about one third of the junction is "active"). In most cases published so far, S/Sm/S junctions appear to have much smaller "active" areas.

IV Conclusions

We have demonstrated a novel and very simple technique to fabricate planar S-Sm-S structures in Al on δ-doped GaAs with high interface transparency (up to 70 %). Subharmonic energy gap structure (SGS), zero bias excess conductance and excess current at high voltage bias were observed. The two former features were only seen in junctions where the length of the semiconductor (GaAs) channel was shorter that the phase-breaking diffusion length in the channel material, $L < \ell_\phi(T)$, a characteristic length which at low temperature exceeds the coherence length in the semiconductor. The junctions were found to be spatially homogeneous.

In the future, similar junctions with shorter channel length should be fabricated and studied in order to further investigate the phase-coherent transport effects.

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