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An ultra low-power off-line APDM-based switchmode power supply with very high conversion efficiency

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ABSTRACT

This article describes the results from the research work on design of a ultra low power off-line power supply with very high conversion efficiency. The input voltage is 230V_{AC} nominal and output voltage is 5V_{DC}. With ultra low power levels is meant, a output power level in the area ranging from 50mW and up to 1000mW. The small power supply is intended for use as a standby power supply in mains operated equipment, which requires a small amount of power in standby mode.

INTRODUCTION

This article describes the final design and results from a Ph.D. project [1] at the Technical University of Denmark, DTU [2].
The motive for this work, with small and highly loss optimized power supply has its origin in a cooperative project between The Technical University of Denmark, the Danish Energy Agency [3] and three Danish electronics equipment manufacturers [4]. The purpose of this project was to investigate the leaking electricity issue and how to lower leaking electricity in common electrical equipment by using a separate high efficiency switch mode converter.

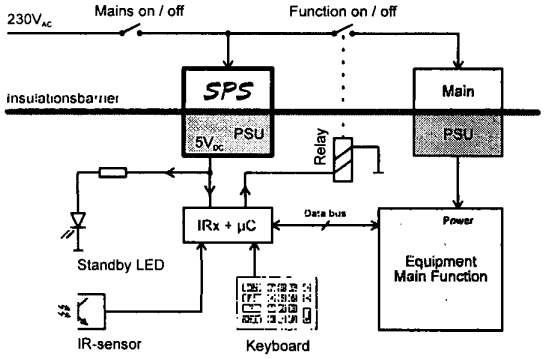

Figure 1 Intended use of the standby module

This article covers only the standby power supply shown as the SPS-block in Figure 1. Leaking electricity losses is also called standby power losses.

At the start of the standby power project the specifications for the small ultra low power standby power supply was defined as:

Target specification for the new low loss SPS-unit:

- **Input voltage:**
  230V_{AC} (195-265V_{AC})
  or
  115V_{AC} and 230V_{AC} (85V_{AC} - 265V_{AC})
- **Output voltage:**
  U_{out} 5V_{DC}
- **Output Power:**
  Min. load 50mW
  Max. load 1000mW
- **Efficiency:**
  At least 65% @50mW
  At least 80% @1000mW
- **Galvanic insulation due to:** Norm
- **Operating temperature:** 0-70°C
- **Volume less than or equal to:** 10cm^3
- **Robust:**
  (Electrical design, Manufacture, Technology)

The overall design should furthermore be carried out in a way so it both facilitates an easy construction by common of-the-shelf components and a later IC-design of the control circuit.

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DISCUSSION

One of the major problems in the design of power supplies for ultra low power is to keep the idle losses (constant losses) low in the power converters own internal circuit. Secondly the losses which is a function of the load current (variable losses) should depend in a reasonable way.
In order to get ahead the priority list for most important properties is defined as shown in the list below. The order in the list might suprise the reader, because the cost issue is the last item. But in order to ensure the fundemental research work it is put in as the last item, but of course there is close attention to this subject throughout the whole design work. Later, when a proper solution is found one can determine whether or not the final solution is useable and then make some trade off's (most likely on efficiency) to lower the costs.

Priority of design properties - in descending order:

Efficiency, **R**obustness, **F**acilitate later IC realization of the control circuit section, **F**acilitate a later mass produced module design, **C**omponents is common standard types with second sources, **N**o or few exotic components, **S**mallest possible physical volume, **L**owest possible cost.

If we for short a time take a look at the specification goals, it can be seen that the maximum total losses in the whole converter at full load (1000mW) can be 250mW but at the minimum load it can only be 27mW ! And this is something special, because the 27mW is the sum of the raw conversion losses and the idle loss in the control circuit. If we assume that load dependent losses are purely proportional with the load current. How much energy is then left for use in the control circuit if the efficiency specification should be satisfied?.

$$\eta(I_{out}) = \frac{U_{out} \cdot I_{out}}{U_{out} \cdot I_{out} + k_2 \cdot I_{out} + k_1} \qquad (1)$$

When the constants k_1 and k_2 are determined the following final formula is given:

$$\eta(I_{out}) = \frac{U_{out} \cdot I_{out}}{U_{out} \cdot I_{out} + 1.174 \cdot \frac{W}{A} \cdot I_{out} + 15.18mW} \qquad (2)$$

This shows what is left to the control circuit - only 15.18mW. Compared to an ordinary 6.2V zenerdiode which consumes about 6.2Vx5mA=31mW.

Figure 2 shows the efficiency for a good linear power supply using a loss optimized conventional mains transformer, which is compared to the calculated target efficiency given by formula (2). More efficiency comparisons for conventional topologies can be found in [5,6,7,8]

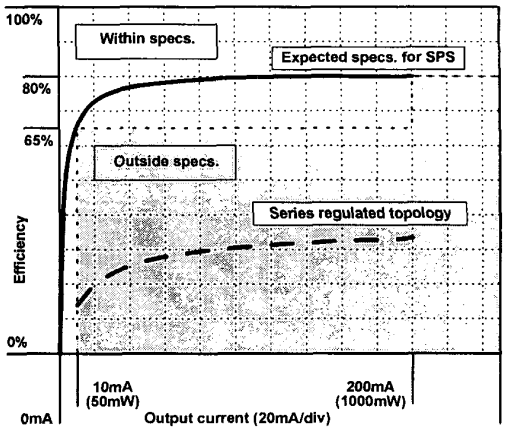

Figure 2 Efficiency comparison

ANALYSIS

Due to the special attention on high efficiency at very light load levels it is obviously that the control circuit should be designed and chosen in a way which uses low loss design techniques at the outmost extent in any of its circuit parts. It is also desirable that the overall control circuit in the power supply is kept as simple as possible because of the issues on price and reliability.

What conversion topology to use ?

As the result of a topology investigation [5], which was made as part of the project, It was concluded that a one-transistor flyback based topology was the most suitable for the converter. The dominant reasons for selecting this topology is found in its simplicity and because it does not require any high side driver for the switch element. Furthermore it is a well proven topology which is very robust when designed carefully.

What conversion principle to use ?

The next issue is to investigate the possibilities to improve efficiency enough to at least satisfy the expected specifications. If these efficiency levels is compared to obtained efficiency levels in flyback converters which are designed for higher power levels it should be possible to achieve efficiencies above 80%. But it is also known that the issue concerning idle losses is very critical because of the extreme low power level.

The most dominant losses in a flyback converter design for higher power levels using a constant and high switching frequency are:

At full load the most dominant losses usually are:

1. Conduction losses in flyback diode (V)
2. Parasitic cap. in the high voltage circuit (C)
3. Leakage inductance in transformer (V)
4. Core and copper losses (V)

At light load the dominant losses usually are:

1. Parasitic cap. in the high voltage circuit (C)
2. Control circuit (primary side) (C)
3. Reference circuit (secondary side) (C)
4. Leakage current in flyback diode (C)

(C) means constant loss and (V) means variable loss.

How to avoid or reduce constant losses:

If the disturbing losses cannot be completely eliminated, then what can be done? A way is to lower the losses to a absolute minimum by changing some or all the constant losses into variable losses.
Variable losses means losses which are proportional to the output power.
If this load/loss dependency can be implemented successfully in a low power flyback converter it is possible to keep the efficiency high over a very wide load range. With the use of this scheme the efficiency is only limited by the raw conversion efficiency, which in this low power case mainly is determined by the loss caused by threshold voltage in the flyback diode.

Eventually when the load gets very low and the internal idle losses are becoming comparable to the load, the efficiency will drop quickly.

The solution for better overall efficiency:

In the usual constant frequency and variable duty-cycle flyback design, the duty-cycle is regulated to maintain the correct energy transfer from primary to secondary and thereby keeping the output voltage constant. In this case a switch cycle is composed of a switch-on time (t_1) and switch-off time (t_2). If the converter is running in discontinuous conduction mode (DCM) t_2 itself is composed of freewheeling time (t_{2f}) and a dead time (t_{2d}).
Another way to maintain the correct energy transfer is to keep the on-time t_1 constant thereby transferring a constant energy package per switch cycle. In this case the converter can be designed to show the optimal efficiency in this well defined working point.
When this constant energy package transfer scheme is used the energy transfer must be controlled in another way, because the on-time is kept constant.
In the new proposed control principle, energy transfer is controlled by regulating the overall density of the transferred energy packages. The desired energy density can either be maintained by a repeated fixed size burst of energy packet or the frequency of single energy packages can be regulated. The first operating mode is called burst mode and the second one is the proposed **A**nalog **P**ulse **D**ensity **M**odulation (APDM) [9].

The APDM solution:

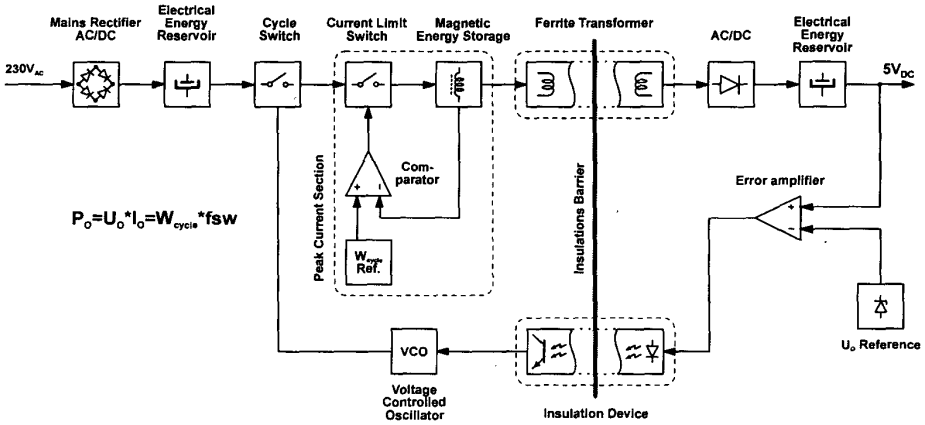

Figure 3 Overall block diagram for the APDM-based standby power supply

Because of the poor secondary ripple performance of burst mode the APDM principle is used to design the described standby power supply.

By using the APDM principle the most dominant constant loss, which is caused by the parasitic capacitance in the high voltage circuit, is now changed into variable losses.

It can be said, that the APDM based converter operates a short period at full power, where it achieves its best conversion efficiency. In the short full power period the output capacitor is charged. In the dead time the output capacitor delivers the energy to the load.

A noticeable feature of the APDM principle is that the output capacitor does not require any excess capacitance compared to a equal constant switching frequency converter.
If the APDM based converter is used in a environment where it sees relative large and fast step loads, extra capacitance might be needed to give the regulation circuit enough time to find it's new equilibrium.

To optimize the efficiency of the APDM-based converter further, the control circuit must be loss optimized to its outmost extent and especially its reference section which is also active in the dead time period.

To make the APDM-based converter even better a peak current detector is included. With this inclusion the energy packet size is maintained constant even when the input voltage is varying. The advantage is that a very large ripple can be locally compensated and thereby not disturbing the output voltage control loop. Furthermore this quality can be used as a way to reduce the primary link capacitor value or/and extend the power supply input voltage range.
The APDM design allows the supply voltage for the peak-current-detector circuit can be connected to the gate drive voltage, which means that the peak-current-detector is only active in the switch on time and thereby reducing the losses.

Figure 4 shows the basic principle of the APDM control circuit. The VCO (**V**oltage **C**ontrolled **O**scillator) controls energy transfer and the peak current detector ensures that a constant sized energy packages is transferred on each switch cycle even if the input voltage is not constant.

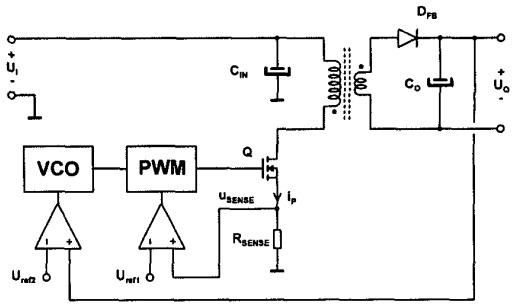

Figure 4 APDM control principle

How is the APDM design optimized?:
The method for designing a high efficiency power supply differs from the usual way to carry out such a design because of the expected low loss levels. In a ordinary design one will typically select a core size which is just big enough to transfer the energy whitout overheating the windings and core material.

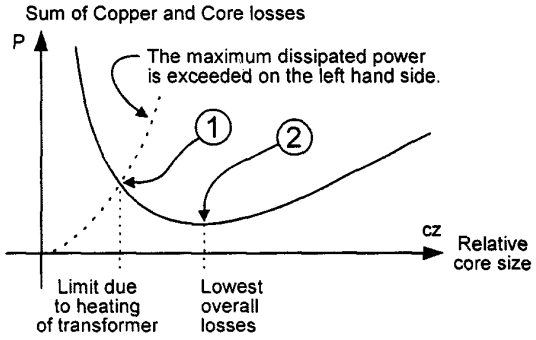

Figure 5 Rough comparison of optimization methods

In this project high temperatures is a word one do not want to hear about, because it also means excessive losses when it is compared to the desired efficiency specifications.
Figure 5 illustrates, how a usual core size optimized design differs from the low loss optimized design.
The curve shows losses as a function of relative core size at a constant amplitude of the flux density (B).
At the point marked '1' the core size is squeezed down to a minimum where losses causes the highest allowable temperature rise. The other point marked '2' is where the lowest losses is obtained.

Then, how can this power supply be designed when maximum allowable dissipation can not be used as a guide for the design? We have to find a function which calculates the overall loss figure for the whole converter in a given working point. In this way of design there are not any well defined parameters which can be used to perform an exact calculation in one step. There are many parameters and component data which all affects the overall losses.
To get further ahead it is necessary to select some parameters and component data and then optimize on the rest to find the best combination among them. Formula 3 shows the basic function which is used to seek out the combination for the best efficiency.

$$\eta(\bar{v}) = \eta(U_{in}, I_o, U_{refl}, t_{on}, cz, Sw_{cycles\_sec}, B_{max}) \qquad (3)$$

Description of parameters:

U_{in}	= Mains input voltage
I_o	= Output current
U_{refl}	= Reflected voltage on primary side
t_{on}	= On time at lowest input voltage
cz	= Relative core size
Sw_{cycles_sec}	= Req. energy packages per sec.
B_{max}	= Max. flux density in core

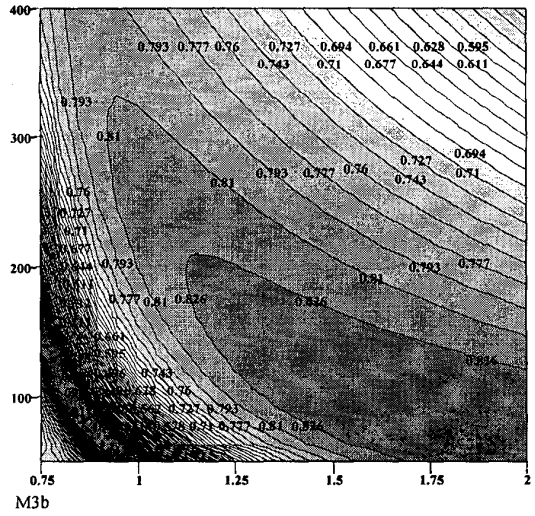

Figure 6 Efficiency as a function of relative core size cz and B_{max}

$$\eta(230V, 200mA, 122V, 18\mu s, cyx, 20kHz, B_{max}y) \qquad (4)$$

Formula 4 describes the simulated situation.
A efficiency simulation example is shown in figure 6.

All the calculated data applies to a design with a E16/8/5, N87 core and a minimum input AC-voltage of 195V_{AC} and nominal voltage at 230V_{AC}, B_{max} is 250mT and the voltage reflected at the primary winding is 122V when the flyback diode is conducting.

Calculated energy budget:

Circuit part	I_O=50mW		I_O=250mW		I_O=1000mW	
	µW	%	µW	%	µW	%
Mains rect.	0	0.00	0	0.00	0	0.00
Link capacitor	24	0.14	109	0.19	430	0.10
MOS-FET - t-on	0	0.00	0	0.00	0	0.00
MOS-FET - cond.	176	1.04	821	1.43	3229	1.54
MOS-FET - t-off	460	2.73	2107	3.66	8284	3.95
MOS-FET - Cds	982	5.83	4501	**7.81**	17696	**8.43**
MOS-FET - Cgs	139	0.82	637	1.11	2503	1.19
Current sense	98	0.58	447	0.78	1759	0.84
Cu Primary	124	7.36	567	0.98	2229	1.06
Cu Secondary	796	4.72	3647	6.33	14338	6.83
Core loss	1803	**10.70**	8261	**14.34**	32476	**15.47**
Leakage inductance	936	5.55	4290	**7.45**	16867	**8.03**
Parasitic cap. in coil	1654	**9.81**	7578	**13.15**	29793	**14.19**
Control circuit - primary	3289	**19.52**	3295	5.72	3315	1.58
Control circuit - secondary	2139	**12.69**	2139	3.71	2139	1.02
Aux-rectifier	332	1.97	246	4.27	228	0.11
Flybackdiode - Conduction	3414	***20.26***	16939	***29.40***	67655	***32.22***
Flyback diode - leakage current	43	2.55	48	0.08	64	0.03
Output Capacitor	443	2.63	1977	3.43	6957	3.31
Total Losses	16852	25.21	57609	18.73	209963	17.35
Output Power	50000	74.79	250000	81.27	1000000	82.65
Input Power	66852	100.00	307609	100.00	1209963	100.00

Table 1 Calculated energy budget

The simulation program is intended to show how the efficiency is affected under various operating situations and component selections - before the design of a actual physical circuit.

Table 1 shows the calculated losses in selected component and the overall efficiency. The calculation is shown for the lowest load at 50mW, at midrange load at 250mW and at full load at 1000mW.

Experimental results

Input ripple rejection:

In this design case the standby power supply is designed to compensate out a 200Vpp primary ripple voltage.

Figure 7 shows a 190.6Vpp 100Hz ripple voltage across the small (267nF@0V) ceramic link capacitor.

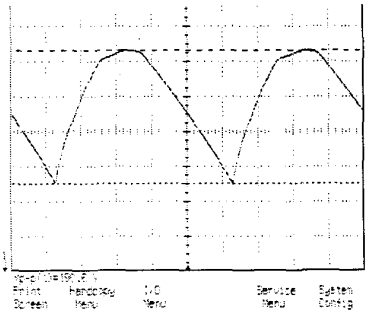

Figure 7 Ripple voltage on link capacitor at Io=200mA

Figure 8 shows the resulting 16.25mVpp 100Hz ripple voltage on the 5V-DC output voltage.

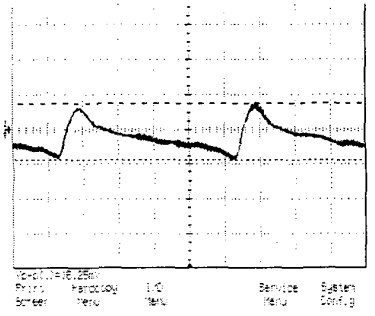

Figure 8 Output ripple voltage at Uin=230VAC and Io=200mA

The efficiency cost for this extreme ability to compensate for a very large ripple voltage is around two percent. As a desired side effect it is very easy to widen the input voltage range to e.g. 85VAC-265VAC. This range enhancement is done simply by adding a 4.7µF/385V electrolytic capacitor in parallel with the present ceramic link capacitor.

Table 2 shows the measured efficiency for the final APDM based converter when a constant 320VDC is applied as input voltage. The reason for applying a DC voltage when measuring efficiency is the fact of the extreme low power levels. As it can be seen the converter only consumes approximately 16µA when it runs without any load. (a common multimeter consumes 32µA because of its input resistance of 10Mohm)

U_O V	I_O mA	P_O mW	U_{IN} V	I_{IN} mA	P_{IN} mW	P_{Loss} mW	Cycl/ sec.	η %
5,069	0,000	0,00	320,40	0,0162	5,19	5,19	0,080	-
5,069	1,072	5,43	320,40	0,0367	11,76	6,33	0,160	**46,20**
5,069	2,293	11,62	320,40	0,0604	19,35	7,73	0,260	**60,05**
5,069	5,044	25,57	320,40	0,1104	35,37	9,81	0,500	**72,28**
5,069	7,399	37,51	320,40	0,1544	49,47	11,96	0,671	**75,82**
5,069	10,617	53,82	320,40	0,2156	69,08	15,26	0,943	**77,91**
5,069	22,570	114,41	320,40	0,4370	140,01	25,61	1,894	**81,71**
5,069	48,542	246,06	320,40	0,9205	294,93	48,87	4,065	**83,43**
5,069	71,249	361,16	320,40	1,3430	430,30	69,14	5,917	**83,93**
5,069	96,259	487,94	320,40	1,8060	578,64	90,71	7,937	**84,32**
5,069	156,110	791,32	320,40	2,9190	935,25	143,93	12,990	**84,61**
5,069	210,490	1066,97	320,40	3,9290	1258,85	191,88	17,360	**84,76**
5,069	259,080	1313,28	320,40	4,8240	1545,61	232,33	21,190	**84,97**

Table 2 Measured efficiency as function of output load

Comparison between measured and calculated loss:

Figure 9 compares the measured efficiency with the calculated. The calculation shows an efficiency about 2% lower than the measured. It is supposed that the difference lies in the use of worst case loss calculations for core losses, leakage inductance and paracitic capacitances. But in any way the calculated and measured data shows a very fine accordance even when considering the extreme low power levels.

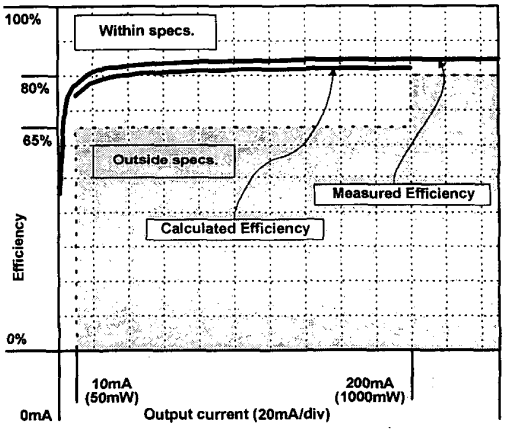

Figure 9 Comparison between calculated efficiency and measured efficiency, upper curve is measured efficiency

All efficiency measurements complies to a converter input voltage of 320VDC and an output voltage of 5VDC. When the efficiency is measured at 230VAC it might be up to 0.4% lower. Please remark that the final efficiency figures, which are stated in the conclusion is the ones with the worst case measurement uncertainty subtracted and the above mentioned loss due to rippel on the link capacitor.

All DC-measurement are made with HP-34401A Multimeters in 4-wire configuration.

Table 3 shows the measured efficiency sensibility for various input voltage levels.
As it can be seen the efficiency is only changing by 2% when the input voltage is changed in the range from 75V_{DC} and up to 450V_{DC}. This measurement documents that the efficiency only will be slightly affected when the input ripple voltage is very large.

U_O V	I_O mA	P_O mW	U_{IN} V	I_{IN} mA	P_{IN} mW	fsw cycl/s	η %
5,069	50,605	256,52	75,07	4,182	313,97	5,917	**81,70**
5,069	50,605	256,52	100,31	3,113	312,27	5,435	**82,15**
5,069	50,605	256,52	125,95	2,463	310,21	5,291	**82,69**
5,069	50,605	256,52	150,31	2,055	308,89	5,102	**83,05**
5,069	50,605	256,52	175,37	1,754	307,60	4,950	**83,39**
5,069	50,605	256,52	200,40	1,532	307,01	4,785	**83,55**
5,069	50,603	256,51	225,40	1,361	306,77	4,675	**83,62**
5,069	50,603	256,51	250,10	1,225	306,37	4,525	**83,72**
5,069	50,603	256,51	275,80	1,111	306,41	4,405	**83,71**
5,069	50,603	256,51	300,10	1,022	306,70	4,292	**83,63**
5,069	50,603	256,51	325,80	0,943	307,23	4,184	**83,49**
5,069	50,603	256,51	350,25	0,879	307,87	4,082	**83,32**
5,069	50,603	256,51	375,54	0,821	308,32	4,000	**83,20**
5,069	50,603	256,51	400,13	0,773	309,30	3,876	**82,93**
5,069	50,603	256,51	425,50	0,731	310,83	3,802	**82,52**
5,069	50,603	256,51	450,16	0,695	312,86	3,717	**81,99**

Table 3 Measured efficiency as function of DC-link voltage

Figure 10 Compares the measured efficiency and calculated efficiency as a function of the input voltage. The upper curve is the measured one. And as the previous comparison there is a very good accordance between calculated result and measured results.
The up to 2% difference in efficiency may be caused by loss differences in the transformer, the use of too pessimistic component values and model divergence.

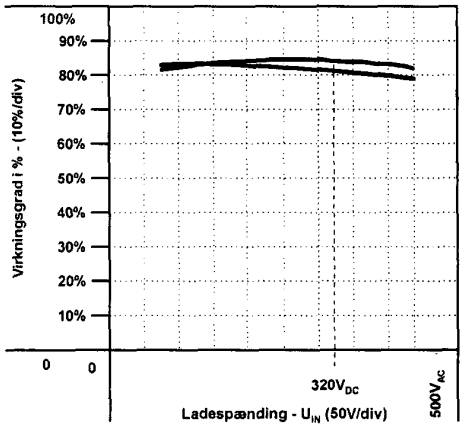

Figure 10 Comparison between calculated and measured efficiency as a function input voltage.

The final APDM based standby converter:

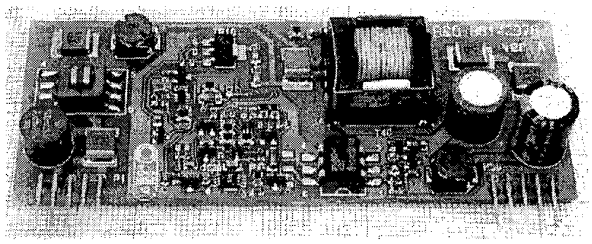

Figure 11 Picture of manufactured SPS-test module.

CONCLUSION

The final and fully functional design demonstrates an efficiency which reaches 76% at 50mW load and 83% at 1000mW load. The volumen of the shown test module is appoxemately 12 cm^3. The power supply demonstrates the expected high ripple rejection which allows a very small primary link capacitor. It is also demonstrated that the input voltage range can be extended to cover universal mains range simply by adding an 4.7µF/385V capacitor. It is succeded to design the control circuit in a way so it can easily be implemented by using cheap off-the-shelf components. Furthermore the control circuit is designed in a way, which facilitates a later custom IC-realization.

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