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Optimized Load Sharing Control by means of Thermal Reliability Management

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Abstract – As the demand for reliable power systems comprised of parallel-connected converter units continue to increase the need for optimized load sharing techniques rises accordingly. This fact is emphasized by a power system minimization trend that tends to shrink the available PCB area set aside for the power system. These contradictory trends feed the research in topics such as advanced thermal management and dynamic thermal management. Implementation of the latter topic usually requires the use of complicated controllers that continuously monitors the thermal working environment and key components within the system. If the thermal stress exceeds preset limits the controller react according to a predetermined sequence to minimize the damaging effects of excessive thermal stress.

This paper combines the dynamic thermal management with the load sharing. It is hereby effectively ensured that the parts count is kept to a minimum while providing a dynamic optimization of parameters such as average and absolute system temperatures as well as overall system reliability. The latter aspect is achieved by redistributing the current throughput of each converter, which in turn results in equal thermal conditions as opposed to well-known and widely used current sharing technique's intent to establish equal currents.

I. INTRODUCTION

With new applications for high-current low-output-voltage power systems emerging nearly every day the need for new and cost-efficient power system designs is a matter of course. As output voltage levels continue to decrease an approach that seems more and more attractive is the implementation of distributed power configurations with point-of-load power conversion. This technique distributes a high voltage to all parts of the system, thus minimizing the voltage drops throughout the distribution network. However, this configuration only solves the problem of power losses in the distribution network while the problems of high-current low-output-voltage conversion at the point-of-load remain a challenge. A common solution to the latter problem is parallel-connection of multiple converter units. This technique is attractive for a number of reasons. The first and most obvious is that it provides the designer with a simple technique for reliability improvements as redundancy quite

easily can be implemented. Another advantage of this particular technique is that it allows the designer to implement large power systems by means of off-the-shelf units, thus minimizing parameters such as design time and system costs. However, due to non-ideal parts each converter unit deviates from the ideal case, which makes a power system comprised of parallel-connected converters a rather poor performing system. To account for the non-ideal parts some form of load sharing is needed to ensure that each converter in the configuration delivers its share of the total output power.

In other words parallel-operation of multiple converters is employed when specifications require a highly reliable system, designable within a very short time frame and at low costs. However, to make full use of the system's potential load control is a *must*.

The steps involved in designing a power system are many and would by no means fit the page limit of this paper nor is it the intention of this paper to describe a detailed power system realization. However, in order to clarify some of the design choices described in subsequent sections a very short introduction to the initial design considerations will be given.

The first design consideration of importance to the N+1 redundant power system described in this paper is the number of converters to use. In the design of a N+1 redundant system the most straight forward implementation is the design of two identical converters each capable of supplying the maximum load current. However, this approach results in a 100% power 'overshoot' – meaning that the available system power is twice that required by the specifications. Increasing the number of converter units reduces this power 'overshoot'. For a N+1 redundant power system Figure 1 shows the percent-wise decrease in power 'overshoot' as the number of converter units increases. The other curve is an index that takes into account the decrease in converter unit cost price, the increase in circuit complexity and the increase in load sharing circuitry costs – all a function of the number of converter units. The index is based on component cost (pr. 1000 pieces) and standard load sharing implementation circuitry. It should be noted that the index curve in many situations will change as a function of the number of units when large scale manufacturing is employed and/or different load sharing techniques are used.

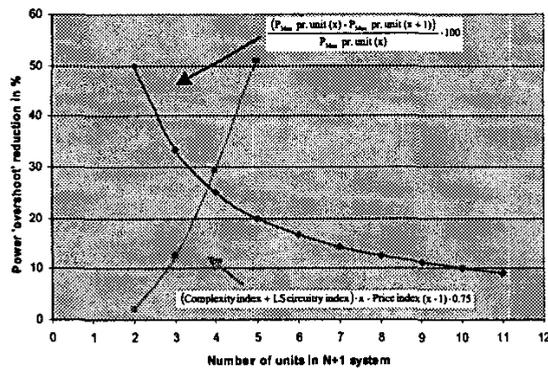


Figure 1 : Percent-wise decrease in power ‘overshoot’

From Figure 1 it can be seen that the two curves intersect somewhere between 3 and 4 converter units. This point is the optimum in the configuration at hand. However, as indicated above this optimum point is most likely to shift to either side along the axis of abscissa when other power system implementations are considered.

From a reliability point of view the number of converter units should be kept to a minimum. As an example using the data for the power system at hand a N+1 redundant system comprised of 4 converter units is 40% more likely to fail at any given time than a N+1 redundant power system comprised of 3 converter units. The same tendency holds when transitioning from a 3 converter system to a 2 converter system. However, due to the percent-wise larger increase in component count in the latter case the probability of system failure is 65% higher in a N+1 redundant 3 converter system than that of a N+1 redundant 2 converter system. From these calculations it can be seen that as the number of converter units increase a smaller and smaller gain in reliability is achieved when substituting an X unit system with an X-1 unit system.

The next design consideration of importance to this paper is the choice of load sharing technique. The most commonly used technique is the current sharing technique. This paper examines the current sharing technique as well as a new thermal load sharing technique. In each case the pros and cons will be discussed and a comparison of the two techniques will be presented in section “VI. RELIABILITY”.

II. POWER SYSTEM

Based on the intersection of the two curves shown in Figure 1 and the subsequent reliability issues concerning parallel-connection of multiple converter units the power system in this paper is comprised of N+1=3 parallel-connected buck converters each capable of supplying 15 A_{RMS} at an output voltage of 5V. The maximum load current I_{OUT} is 30 A.

With reference to Figure 2 the individual converter parameters in the parallel-configuration can be identified. I₁, T₁ are parameters associated with converter 1; I₂, T₂ are associated with converter 2 and I₃, T₃ are associated with

converter 3. These parameters form the basis of the thermal calculations as well as the reliability assessments.

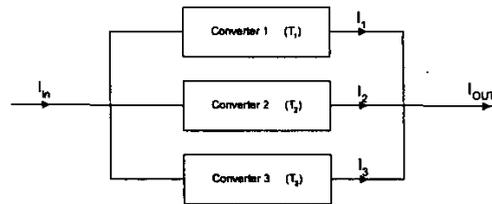


Figure 2 : N+1 redundant power system

All calculations are all based on the assumption that each buck converter is implemented with a single MOSFET transistor. In converter implementations with multiple MOSFET switches and/or synchronous rectification the overall impact of improper load sharing would be even more profound. A fact that can be deduced from the calculations in section “IV. EFFECTS OF PARASITIC ELEMENTS”.

Although a strictly theoretical analysis the following calculations establishes the foundation for rethinking the ‘obvious’ load sharing approach – the current sharing technique.

III. CURRENT SHARING

The most common and widely accepted technique for load sharing is the current sharing technique. The idea behind the technique is that equal stress and temperature is achieved with identical currents through each converter. In turn, this should result in optimized performance and reliability. In the ideal case with identical converter components and identical thermal operating surroundings this technique does indeed result in optimized performance and reliability. However, the ideal case is very rare and the result of implementing the current sharing technique is often less advantageous than predicted by the theoretical models.

Figure 3 shows the general case where a number of converters are paralleled and forced to supply an equal share of the total output current.

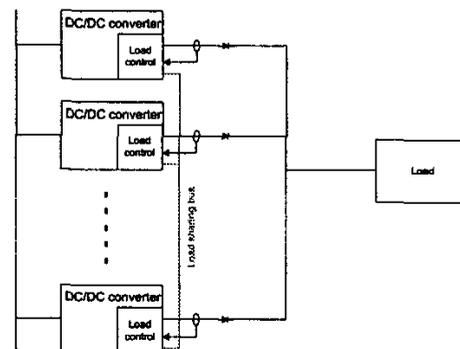


Figure 3 : Traditional current sharing technique

A more detailed illustration of the current sharing technique is depicted to the right in Figure 4 – where it can be seen that high side current sensing is required (in non-isolated systems) as well as dual supply rails for the control circuitry.

The illustration of I_{OUT} vs. Temperature in Figure 4 (lower left) is a representation of the maximum output current (I_{MAX}) as a function of system temperature. In most converter designs the horizontal line (I_{MAX}) determines the maximum safe output current and is often based on output current under worst-case temperature conditions.

The current sharing technique is thoroughly described in numerous papers, articles and application notes [4] - [7]. For this reason the description of this technique will be limited to that already presented. As a summary the pros and cons of the current sharing technique will briefly be discussed.

The advantages of the current sharing technique

compared to that of a system without any load sharing are many. Being a simple technique to implement the current sharing technique ensures that no single converter unit is stressed to the maximum. This is ensured by preventing any single converter from going into current limitation – due to for instance small variations in individual converter output voltages. The main drawback of the current sharing technique is the need for output current sensing. Sensing the output current is typically done by inserting a resistor in series with the converter output. This resistor causes additional power loss – although it can be kept to a minimum compared to for example the semiconductor losses of the converter – thus resulting in system heating.

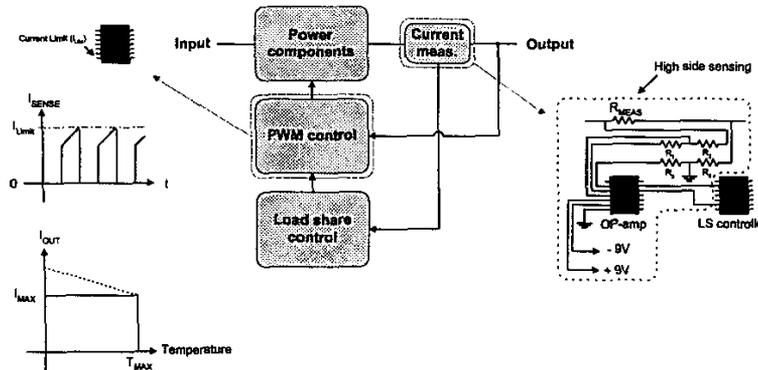


Figure 4 : Current sharing implementation and controller current waveform

IV. EFFECTS OF PARASITIC ELEMENTS

All electronic parts are associated with parasitic elements that deviates from the ideal-part models used in the initial system analysis. Since a description of all these parasitic elements would form the basis for an entire paper this section concentrates on addressing the parasitic elements associated with the MOSFET transistors. This simplification is justified by the fact that the MOSFET transistor in the power system at hand generates the most heat. Being the primary source for system heating the MOSFET transistor is also the primary cause of deteriorated system reliability.

To simplify matters even further in order to fit the page limit the analysis in this paper focuses on the conduction losses caused by the temperature dependent MOSFET ON-resistance. Although switching losses also depend on temperature [3] these losses contribute far less to the load sharing temperature deviation than the conduction losses.

According to transistor manufacturer’s datasheets the nominal value of the MOSFET ON-resistance $R_{DS(ON)}$ can vary by as much as $\pm 30\%$ from one batch of transistors to another. A fact that must be taken into account when thermal system issues are considered. However, the variation in $R_{DS(ON)}$ between transistors from the same batch is usually much smaller.

Figure 5 shows the MOSFET ON-resistance as a function of temperature for the MOSFET transistors used in the power system design shown in Figure 2.

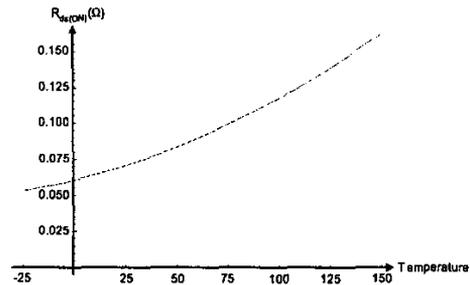


Figure 5 : MOSFET $R_{DS(ON)}$ temperature dependency

In Figure 5 it can be seen that the MOSFET ON-resistance increases from 70m Ω to 140 m Ω when the junction temperature increases from 25°C to 140°C.

By means of a simple example this section will show that utilization of the current sharing technique with intend to optimize the overall system reliability quite often results in imbalanced power loss distribution within the system.

MOSFET transistor power generation due to $R_{DS(ON)}$ can be expressed by the following equation:

$$P_{R_{DS(ON)}} = I_{RMS}^2 \cdot R_{DS(ON)} \tag{1}$$

The heat generated by the power loss calculated in (1) is transferred from the MOSFET casing and heat-sink to the ambient by means of convection and radiation. A mathematical description of this heat transfer can be established by the following two equations [2]:

$$P_{\text{Convection}} = 1,34 \cdot A \cdot \sqrt[5]{(T_{\text{Surface}} - T_{\text{Ambient}})^5} \quad (2)$$

$$P_{\text{Radiation}} = 5,7 \cdot 10^{-8} \cdot A \cdot (T_{\text{Surface}}^4 - T_{\text{Ambient}}^4) \quad (3)$$

In (2) the variable 'h' is the height of the heat-sink while the variable 'A' in both (2) and (3) denotes the area of the heat-sink. A graphical representation of (2) and (3) is shown in Figure 6 and Figure 7 respectively.

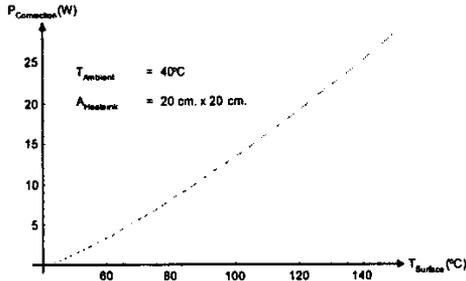


Figure 6 : Power dissipation caused by convection

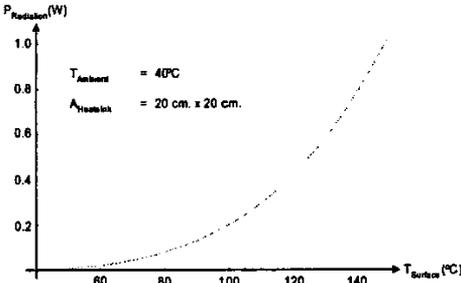


Figure 7 : Power dissipation caused by radiation

From Figure 6 and Figure 7 it can be seen that the heat transfer from MOSFET to ambient is almost solely due to convection.

In order to calculate the conduction losses the choice of MOSFET transistor must be recognized. For illustration purposes it is chosen to implement the three converters in the configuration with a transistor of nominal $R_{DS(ON)}$, a transistor of nominal $R_{DS(ON)} + 30\%$ and a transistor of nominal $R_{DS(ON)} - 30\%$ respectively. In a real-world implementation this scenario would be extremely rare although a difference in $R_{DS(ON)}$ among the three transistors should be expected.

Thermal equilibrium is obtained when heat generation equals heat dissipation. To assist in the estimation of MOSFET transistor temperature the thermal model shown in Figure 8 is established.

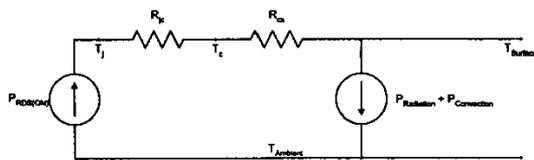


Figure 8 : Thermal system equivalent

Using (1), (2), (3) and the thermal model shown in Figure 8 an exact value for the conduction losses and MOSFET temperatures can be found:

$$T_j = 90.7^\circ\text{C} \quad T_s = 78.4^\circ\text{C} \quad P_{R_{DS(ON)}, \text{nom}-30\%} = 7.7\text{W} \quad (4)$$

$$T_j = 121.4^\circ\text{C} \quad T_s = 99.8^\circ\text{C} \quad P_{R_{DS(ON)}, \text{nom}} = 13.5\text{W} \quad (5)$$

$$T_j = 173.9^\circ\text{C} \quad T_s = 134.9^\circ\text{C} \quad P_{R_{DS(ON)}, \text{nom}+30\%} = 24.4\text{W} \quad (6)$$

As expected the temperature dependency of the MOSFET ON-resistance have a negative overall effect that contributes to a significant increase in conduction losses.

The calculated temperatures indicate that the MOSFET transistor with $R_{DS(ON), \text{nom}+30\%}$ operates very close to the recommended maximum temperature and is thus very likely to fail.

From the results in (4), (5) and (6) the average junction temperature for the 3 MOSFET transistors can be found to be 128.7°C while the associated average heat-sink surface temperature is 104.4°C .

V. THERMAL LOAD SHARING

The proposed thermal load sharing technique compensates for the imbalanced power losses that result from implementing the current sharing technique. By monitoring the temperature of the heat generating component (or components) the load current supplied by each converter in the parallel-configuration can be adjusted to take into account parameters such as parasitic elements, physical layout and working environment.

Using this technique each converter works at the same temperature, which in turn results in identical converter reliability in the parallel-configuration.

Figure 9 shows the thermal load sharing technique in a configuration where the MOSFET transistor heat-sink temperatures are monitored and fed back to the control circuitry. This configuration corresponds to the system considered in this paper.

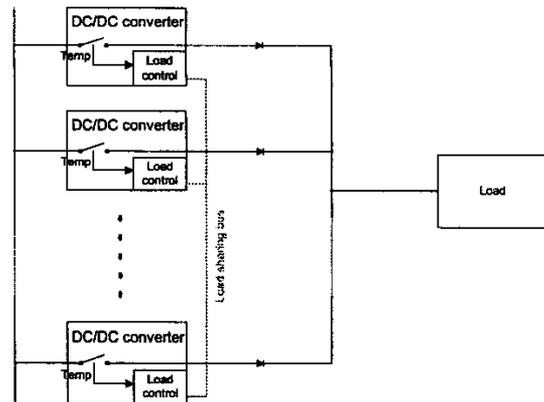


Figure 9 : Thermal load sharing technique

The real-world implementation of the thermal load sharing technique is straight forward, since the existing control circuitry employed by for example the current sharing technique can be used. The temperature sensing device is simply mounted at the most critical location within the device – in this case on the MOSFET transistor casing. The temperature signal is then fed back to the load share controller where it replaces the current signal. To ensure a system startup without running one or more converters into current limitation the signal from the current

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 measurement can be combined with the temperature information to create a load share controller that initially uses the current sharing technique. As the temperature of the individual converters change the output current information is offset by the temperature signal – thus maximizing system efficiency and reliability.

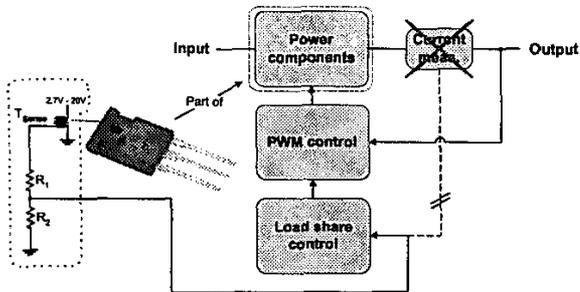


Figure 10 : Temperature sensor mounting

Using the same equations that were used to calculate the MOSFET transistor power losses and temperatures in section “IV. EFFECTS OF PARASITIC ELEMENTS” the load distribution for the thermal load share technique can now be established. It should be noted that the temperature was a variable in the current sharing calculations while the individual load currents were fixed parameters. In the case of thermal load sharing the temperature is fixed while the current distribution among the individual converters is the variable. The result is shown below:

$$I_{Rds(on), nom-30\%} = 11.7 \text{ A} \quad (7)$$

$$I_{Rds(on), nom} = 9.6 \text{ A} \quad (8)$$

$$I_{Rds(on), nom+30\%} = 8.7 \text{ A} \quad (9)$$

The average MOSFET junction temperature that results from distributing the load current as calculated in (7), (8) and (9) is 115.5°C. This is 13.2°C lower than the average junction temperature using the current sharing technique. Due to the fact that heat dissipation from heat-sink to ambient depends on source-to-ambient temperature difference the average surface temperature associated with the 115.5°C junction temperature is 95.7°C. This is 8.7°C lower than the average surface temperature in the current sharing case. Since the overall system reliability is a function of heat-sink surface temperature it can easily be seen that the probability of system survival is much better in the case of thermal load sharing.

Among the advantages of the thermal load sharing technique is its ability to optimize the system reliability at any given time, its system efficiency enhancing capabilities and its easy and cost-effective implementation. Another, perhaps less obvious, advantage of the thermal load sharing technique is its ability to control converters with different power ratings. Suppose a power system was comprised of multiple high power converters and a single low power converter. If the low power converter is being over-loaded its temperature would increase causing the thermal load share controller to require the remaining converters to supply more current, thus alleviating the over-loaded converter. A similar situation in a system employing the current sharing technique would quickly cause a converter malfunction.

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Even though very little system affect results, a disadvantage of the thermal load sharing technique that must be mentioned is the possibility of a slightly increase in individual converter failure rate. However, this drawback is by far compensated through the much lower average system temperature that results from the implementation.

VI. RELIABILITY

It is well known that system temperature is the single most important parameter in system reliability assessments. Minimizing the temperature rise increases the system reliability and quite often also results in better system efficiency. Therefore in order to assess the system reliability the component distribution of the printed circuit board must be known.

When considering the physical layout of the converter there is a trade-off assessment between the thermal aspects of the converter design and the electrical constraints of for instance the physical distance between MOSFET and controller IC. From a reliability point of view the IC should be positioned as far away from the heat generating MOSFET as possible. However, from an electrical point of view the IC should be positioned as close to the MOSFET gate terminal as possible – in order to minimize the effects of PCB trace inductance. As a compromise the layout shown in Figure 11 is chosen for the reliability assessment.

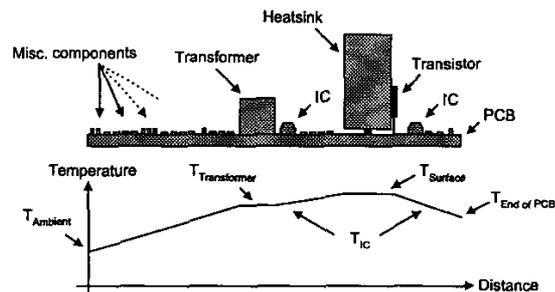


Figure 11 : System temperature distribution

Based on the above temperature distribution an assessment of the overall system reliability can be established.

Using the component data found in [1] the following failure rates (expressed as failures in 10^9 hours) for the three converters in the current sharing configuration can be calculated:

$$\lambda_{R_{ds(on)}, nom-30\%} = 4383 \text{ FIT} \quad (10)$$

$$\lambda_{R_{ds(on)}, nom} = 9042 \text{ FIT} \quad (11)$$

$$\lambda_{R_{ds(on)}, nom+30\%} = 27471 \text{ FIT} \quad (12)$$

The probability of survival for each converter is calculated by utilizing the exponential distribution:

$$\text{Prob} = e^{-2.10^{-9} \cdot (8760 \text{ hours})} \quad (13)$$

It should be noted that the calculated probability of converter survival is for a period of one year.

$$\text{Prob}_{R_{ds(on)}, nom-30\%} = 0.9623 \quad (14)$$

$$\text{Prob}_{R_{ds(on)}, nom} = 0.9238 \quad (15)$$

$$\text{Prob}_{R_{ds(on)}, nom+30\%} = 0.7861 \quad (16)$$

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 Combining the binominal coefficients for the probability that all converters work with that of one converter fails results in the following system reliability:

$$\text{Prob}_{\text{System}} = 0,9740 \quad (17)$$

Expressing this probability in terms of system unavailability the following probability of annual down-time can be established:

$$\bar{P} = 1 - \text{Prob}_{\text{System}} = 1 - 0,9740 = 0,0260 = \underline{2,60\%} \quad (18)$$

Performing the same reliability calculations for the thermal load sharing technique provides a foundation for a system performance comparison. Since the temperatures in this case are the same for all three converters they have identical failure rates:

$$\lambda_{\text{Thermal}} = 7819 \text{ FIT} \Rightarrow \text{Prob}_{\text{Thermal}} = 0,9338 \quad (19)$$

Based on (19) the overall system reliability can be calculated:

$$\text{Prob}_{\text{System}} = 0,9874 \quad (20)$$

Expressing (20) in terms of unavailability:

$$\bar{P} = 1 - \text{Prob}_{\text{System}} = 1 - 0,9874 = 0,0126 = \underline{1,26\%} \quad (21)$$

Comparing (18) and (21) it can easily be seen that the probability of system malfunction for the thermal load sharing technique is less than half that of the current sharing technique. Calculating the percent-wise decrease in system unavailability one finds that the proposed technique reduces the annual down-time probability by 51.6%. This is a significant reduction caused simply by considering the parasitic elements of the MOSFET transistors. Had the converters been positioned in different working surroundings the effect could have been even more profound.

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 VII. CONCLUSION

This paper has provided the foundation for a new thermal load sharing technique that at any given time ensures optimum reliability, performance and efficiency. A comparison between the thermal load sharing technique and the common and widely accepted current sharing technique is provided and the pros and cons in each case have been discussed.

Reliability estimations have been provided as analytic evidence of the superior reliability of the thermal load sharing technique. Among the advantages of the thermal load sharing technique is optimized reliability, minimization of MOSFET losses resulting in an increase in overall system efficiency and simple implementation. A disadvantage of the thermal load sharing technique is the possibility of a slight increase in individual converter failure rate. However, this fact is by far compensated through the much lower average system temperature that results from the implementation.

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