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Advantages of Using a Two-Switch Forward in Single-Stage Power Factor Corrected Power Supplies

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Abstract:
A Single-Stage power factor corrected power supply using a two-switch forward is proposed to increase efficiency. The converter is operated in the DCM (Discontinues Conduction Mode) and it will be shown that this operation mode insures the intermediate DC-bus to be controlled only by means of circuit parameters and therefore independent of load variations. The DCM operation often has a diminishing effect on the efficiency but by use of the two-switch topology high efficiency with minimum circuit complexity can be achieved in this mode.
A 500W 70V prototype of the two-switch boost-forward PFC power supply has been implemented. The measured efficiency is between 85% and 88.5% in the range 30W-500W and the measured power factor at full load is 0.95.

1 Introduction

The introduction of the EN61000-3-2 specifications has resulted in a wide range of new active PFC-circuits. To reduce component count and productions cost the focus on the Single-Stage approach has been great.
The block scheme in figure 1b shows the Single-Stage approach. In the Single-Stage approach only the output voltage is controlled by the control system. Therefore the topology used to implement the PFC-cell must be of one that will inherently perform this function. The most commonly used topology to perform the PFC in the Single-Stage approach is the DCM (Discontinuous Conduction Mode) boost-converter. The DC/DC-cell must perform the conversion from the DC-bus voltage to the desired output voltage and secure the galvanic isolation.
One of the challenges in the Single-Stage approach is to control the DC-bus voltage without increasing the complexity of the converter.

In this paper the proposed converter will be driven in the DCM for both cells. This mode of operation has the benefit of controlling the DC-bus voltage independent of load-current. The trend in the Single-Stage approach is going towards driving the cells in the CCM (Continuous Conduction Mode) to increase efficiency and reduce the need for EMI-filtering [1], [2]. With the proposed topology it will be shown that high efficiency and low complexity can be achieved in the DCM.

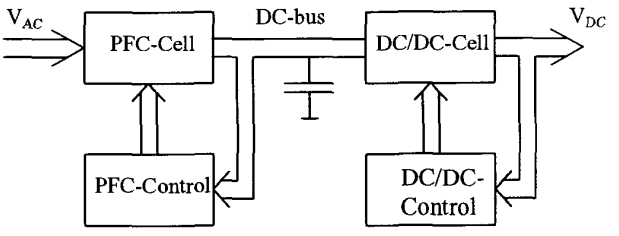

Figure 1a. Two-Stage Converter. Separate Control of PFC and DC/DC Conversion.

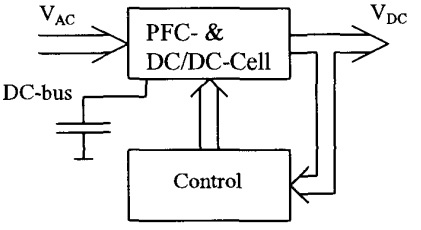

Figure 1b. Single-Stage Converter. DC/DC Control Circuit

2 Single-Stage Boost-Forward PFC Topology

An important aspect of the Single-Stage approach is the ability to perform as good as or better than two-stage approach with respect to efficiency. Achieving higher efficiency over the two stage solution is difficult because optimisation of the Single-Stage converter usually comprise either the PFC ability or the DC/DC conversion. Another aspect of the Single-Stage approach is the stressing of the circuit components. For the Single-Stage circuit in figure 2 the critical component regarding loss of efficiency on the primary side is the switch Q. It must process the current from both the boost- and the forward-section. To keep losses to a minimum a low on-resistance switch is required. This again affects the switching qualities of the device increasing these losses.
To achieve a high PF the power drain from the mains has to be pulsating (power proportional to $\sin^2(\omega t)$ gives PF=1).

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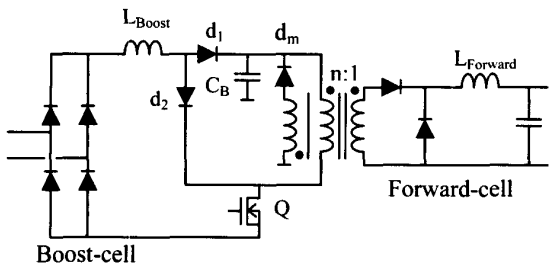

Figure 2. Single-Stage Power Supply Using Boost-Forward Topology.

If the output voltage of the converter is to be tight regulated the pulsating power has to be decoupled internally. In the converter of figure 2 the pulsating power is decoupled by the storage capacitor C_B.
The DC-bus voltage at this node, V_{CB}, is subjected to the power balance between the boost- and the forward-cell. There are 4 possible operating modes for the converter of figure 2 and depending on the actual mode the DC-bus voltage V_{CB} will adjust accordingly.

2.1 CCM for Both Cells

For the converter of figure 2 this mode of operation is not very interesting because of the poor PF qualities of the continuous-current boost cell operated with constant switch on-time. As shown in [2] the DC-bus voltage is independent of load variations and is controlled by the steady state transfer function of the two cells. The CCM of the cells can only be sustained to a certain power level. Going from CCM to DCM will change the power balance, thus affecting the DC-bus voltage.

2.2 CCM Boost, DCM Forward

Operating with constant switch on-time the CCM boost operation is not interesting as stated in section 2.1.

2.3 DCM Boost, CCM Forward

When the Forward cell is operated in CCM and the boost cell is kept in the DCM the DC-bus voltage becomes dependent on load conditions. It has been shown in [3] that the DC-bus voltage increase dramatically when the forward cell is going towards the DCM.

2.4 DCM for Both Cells

As shown in [4] the DC-bus voltage in a Single-Stage boost-flyback topology, operated in DCM, can be determined by investigating the power balance between input and output. The result of this investigation was that the DC-bus voltage was found to be independent of load variations and only dependent on the line voltage and the ratio between the boost- and the flyback-inductance. Using this method on the boost-forward topology the DC-bus voltage can be determined.
The converter efficiency is assumed to be 100%:

$$P_{IN} = P_{OUT} \tag{1}$$

The input-power of the boost-cell is given by:

$$p_{IN}(t) = \frac{v_{IN}^2(t) \cdot D^2 \cdot T \cdot \left(\frac{V_{CB}}{V_{CB} - v_{IN}(t)} \right)}{2 \cdot L_{Boost}} \tag{2}$$

where D is the duty-factor, V_{CB} is the DC-bus voltage, $v_{IN}(t)$ is the time variant line voltage and T is the switching period.
Averaging over one half period of the line frequency, input power can be expressed as:

$$P_{IN} = \frac{\sum_{n=1}^{N} \hat{V}_{IN}^2 \cdot \sin^2\left(\frac{n \cdot \pi}{N}\right) \cdot \left(\frac{V_{CB} \cdot D^2 \cdot T}{V_{CB} - \hat{V}_{IN} \cdot \sin\left(\frac{n \cdot \pi}{N}\right)} \right)}{2 \cdot L_{Boost} \cdot N} \tag{3}$$

$$N = \frac{2 \cdot f_{Line}}{f_{Switch}} \tag{4}$$

where V_{IN} is the peak value of the line voltage, n indicates the nth switching period, f_{Switch} is the switching frequency and f_{Line} is the line frequency.
One would like to use the integral-form instead of the summation in Eq. (3), but there is no closed form solution to this equation when solving for the DC-bus voltage V_{CB}. Thus, Eq. (3) must be solved numerical.
The output power is given by:

$$P_{OUT} = \frac{V_{CB} \cdot (V_{CB} - n_{12} \cdot V_{OUT}) \cdot D^2 \cdot T}{2 \cdot n_{12}^2 \cdot L_{Forward}} \tag{5}$$

where n_{12} is the turns ration and V_{OUT} is the output voltage.
Using Eq. (1), (3) and (5):

$$\frac{L_{Boost}}{L_{Forward}} = \frac{n_{12}^2 \cdot \frac{1}{N} \cdot \sum_{n=1}^{N} \frac{\hat{V}_{IN}^2 \cdot \sin^2\left(\frac{n \cdot \pi}{N}\right)}{V_{CB} - \hat{V}_{IN} \cdot \sin\left(\frac{n \cdot \pi}{N}\right)}}{V_{CB} - n_{12} \cdot V_{OUT}} \tag{6}$$

From Eq. (6) one sees that the DC-bus voltage V_{CB} is dependent on the boost-forward inductor-ratio, the turns

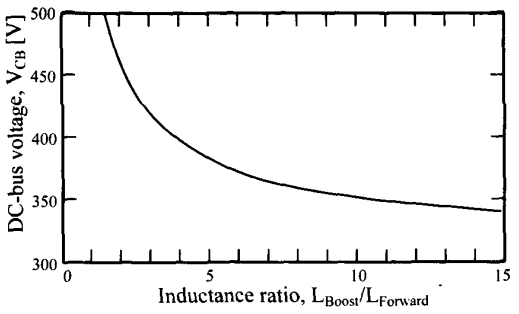

Figure 3. DC-Bus Voltage as a Function of Boost-Forward Inductor Ratio. The Plot Applies for V_{AC} = 230V, V_{OUT} = 70V and n_{12} = 1.5.

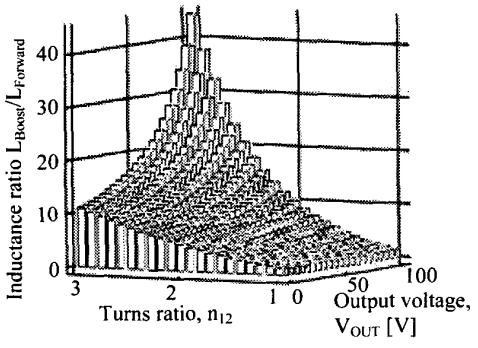

Figure 4. Boost-Forward Inductance Ratio as a Function of the Turns Ratio and Output Voltage. The Plot Applies for V_{AC} = 230V and DC-Bus Voltage V_{CB} = 400V.

ratio, the line-voltage and the output voltage but not on load conditions.

In figure 3 the variation of the DC-bus voltage at different inductance ratios can be seen. Normally the line voltage is given and the DC-bus voltage is dictated by the availability of good high voltage devices (MOSFET's, storage capacitors etc.). Figure 4 displays the inductance ration as a function of both the turns ratio and the output voltage. Unfortunately for the boost-forward topology the transformer turns ratio and the output voltage of the forward cell are also determining factors when calculating the DC-bus voltage as opposed to the boost-flyback topology analyzed in [4].

2.5 The Two-Switch Boost-Forward Topology

Instead of using the single-switch topology of figure 2 the two-switch forward can be used to reduce voltage stress and improve efficiency (figure 5). Both the single-switch and the two-switch boost-forward topology are part of the Single-Stage family presented in [4] and [5].

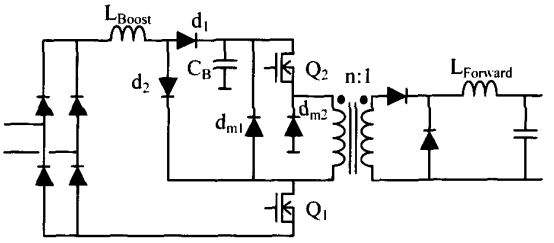

Figure 5. Single-Stage Power Supply Using the Two-Switch Boost-Forward Topology.

When using the two-switch forward in figure 5 instead of single-switch cell, the need for rectifier d_2 becomes obsolete. The resetting of the magnetizing current effectively clamps the switch-voltage to the DC-bus. When taking the magnetizing current path into account further component reduction is possible. After the shortening of d_2 one sees that rectifier d_{m1} is in parallel with d_1 making d_{m1} obsolete. This gives us the simplified version of the two-switch boost-forward of figure 6.

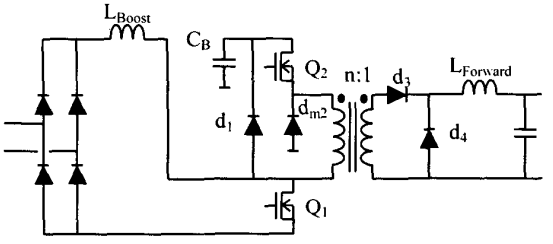

Figure 6. Simplified Version of the Single-Stage Power Supply Using the Two-Switch Boost-Forward Topology.

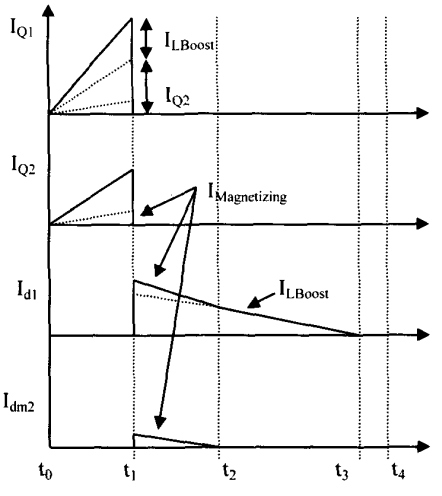

Figure 7. Primary Side Current Waveforms for the DCM Two-Switch Boost-Forward Topology of Figure 6.

3. Circuit Operation

As shown in section 2.4 the DCM operation of both cells will control the DC-bus voltage independent of load variations. Also, the DCM boost will offer a control/correction of the power factor [6].

Figure 7. shows the current waveforms of the primary side semiconductors for the converter in figure 6 when the DCM operation are employed. Circuit operation is simple and straightforward.

t_0: Q_1 and Q_2 turns on. Rectifier d_3 is forward biased while d_1, d_{m2} and d_4 is reversed biased. Energy starts building up in the Boost inductor, Forward inductor and the primary inductance of the transformer.

t_1: Q_1 and Q_2 turns off. The Boost inductor current is directed trough d_1 to the capacitive energy storage together with the magnetizing current. The Forward inductor current begins to flow in d_4 as d_3 is reversed biased. The magnetizing current from Q_2 starts to flow trough d_{m2}.

t_2: The resetting of the transformer is complete, thus turning off d_{m2}

t_3: Energy stored in the Boost inductor during the interval t_0-t_1 has been delivered to the energy storage capacitor.

t_4: A new switching period begins.

Besides the stored magnetizing energy also leakage energy will be returned to the DC-bus making transformer design simple.
The cost of using the two-switch forward over the single switch forward is the need for the extra switch and high side drive circuit. By use of a push-pull controller like the UC3825 or similar and a gate-drive transformer a cost effective gate-drive circuit can be implemented.

4. Performance of the Two-Switch Topology

It is well known in design of regular DC/DC-converters that higher efficiency can be achieved by using two-switch topologies even though the current is processed by two switches. The need for lower voltage-rated devices allows the use of transistors where the on-resistance versus the switching qualities is relatively better than higher voltage rated devices. For MOSFET's rated above 100V the major contributor to the channels on-resistance ($R_{DS(on)}$) is the extended drain region, which is strongly related to the breakdown voltage (V_{BR}) of the device. It can be shown that the relation between $R_{DS(on)}$ and breakdown voltage can be expressed as [7]:

$$R_{DS(on)} \propto \frac{V_{BR}^{2.5}}{A} \qquad (7)$$

, where A is the die area.

A 1000V MOSFET would have 5.6 times higher $R_{DS(on)}$ than a 500V MOSFET with the same die area. If the high voltage rating is needed the use of IGBT's becomes more attractive. But because of the DCM operation of both cells the switching losses are confined to turn off losses only (except the discharging of the parasitic drain-source capacities of the MOSFET's). The fact that the IGBT's typically are associated with relatively high turn off losses may result in unacceptable overall efficiency.

Throughout this section the leakage- and magnetizing currents will be disregarded.

If you look at the two-switch topology in an ordinary DC/DC converter you can easily convert the expected reduction of on-resistance into how much you can reduce the conduction losses. Comparing a single-switch and a two-switch topology using the same total die area in the switches and assuming that the ON-resistance is proportional to the channel width the reduction in conduction losses can be calculated to:

$$\frac{P_{Conduction,1\,Switch}}{P_{Conduction,2\,Switch}} = \frac{I_{Sw,RMS}^2 \cdot R \cdot 5.6}{I_{Sw,RMS}^2 \cdot R \cdot 2 \cdot 2} = 1.4 \qquad (8)$$

,where R is the on-resistance for the low-voltage rated device.

Eq. (8) corresponds to a 40% increase of the conduction losses in the single-switch approach.

The switching losses will also be reduced. Using only half the die area will reduce the parasitical capacitances and therefore increase the switching speed. Assuming that the channel width is proportional to the switching speed the switching losses per device will be reduced with a factor of two.
In the single-switch case the drain-source voltage will have to be changed from zero to the supply voltage before the switch current starts to ramp towards zero. In the two-switch case the current will start this action when the drain-source voltage reaches half the supply voltage. A realistic guess would be that the over all switching losses are reduced with a factor of two.

The effects of using a two-switch forward instead of a single-switch forward with respect to efficiency are obvious. When the two-switch topology is employed in the single-stage PFC approach (figure 6) the effect on the efficiency is a bit more troublesome to present in a clear manner. The lower switch Q_1 in figure 6 has to carry both the forward and the boost current, as shown in figure 7. In the following section a way

of quantifying the effects of using the two-switch configuration as opposed to a single-switch will be presented.

Because of the forward cell being operated in the DCM the peak-current in the upper switch, Q_2, can be expressed as:

$$\hat{I}_{Q2} = \frac{2 \cdot P_{out}}{V_{CB} \cdot D} \tag{9}$$

The RMS-current flowing through Q_2 can then be expressed as:

$$I_{Q2,RMS} = \hat{I}_{Q2} \cdot \sqrt{\frac{D}{3}} = \frac{2 \cdot P_{OUT} \cdot \sqrt{\frac{D}{3}}}{V_{CB} \cdot D} \tag{10}$$

The current flowing through Q_1 is the sum of the switch-current, I_{Q2}, and the boost-inductor current. The later varies in amplitude with the input line voltage over one half line period:

$$\hat{I}_{LBoost}(n) = \frac{\hat{V}_{IN} \cdot \sin\left(\frac{n \cdot \pi}{N}\right) \cdot D \cdot T}{L_{Boost}} \tag{11}$$

The input power is given by Eq.(4). Isolating L_{Boost} from Eq.(4) and inserting this expression into Eq.(11) the peak inductor current can be expressed in terms of input power:

$$\hat{I}_{LBoost}(n) = \frac{2 \cdot P_{IN} \cdot \sin\left(\frac{n \cdot \pi}{N}\right)}{D \cdot \hat{V}_{IN} \cdot Sum1} \tag{12}$$

where

$$Sum1 = \frac{1}{N} \cdot \sum_{n=1}^{N} \left(\sin^2\left(\frac{n \cdot \pi}{N}\right) \cdot \frac{V_{CB}}{V_{CB} - \hat{V}_{IN} \cdot \sin\left(\frac{n \cdot \pi}{N}\right)} \right) \tag{13}$$

The RMS-current in Q_1 can the be expressed as:

$$I_{Q1,RMS} = \sqrt{\sum_{n=1}^{N} \left(\left(\hat{I}_{Q2} + \hat{I}_{LBoost}(n) \right)^2 \cdot \frac{D}{3} \right)} \tag{14}$$

$$\Updownarrow$$

$$I_{Q1,RMS} = \sqrt{\sum_{n=1}^{N} \left(\left(\left(\frac{2 \cdot P_{OUT}}{V_{CB} \cdot D} \right) + \left(\frac{2 \cdot P_{IN} \cdot \sin\left(\frac{n \cdot \pi}{N}\right)}{\hat{V}_{IN} \cdot D \cdot Sum1} \right) \right)^2 \cdot \frac{D}{3} \right)}$$

Introducing the term k as the ration between DC-bus voltage and the peak AC line voltage and taking the converter efficiency (η) into account Eq. (14) can be expressed as:

$$k = \frac{V_{CB}}{\hat{V}_{In}} \tag{15}$$

$$I_{Q1,RMS} = \sqrt{\cdot \frac{1}{N} \sum_{n=1}^{N} \left(\frac{k \cdot sin\left(\frac{n \cdot \pi}{N}\right)}{\eta \cdot Sum1} + 1 \right)^2} \cdot \frac{2 \cdot P_{OUT}}{D \cdot V_{CB}} \cdot \sqrt{\frac{D}{3}}$$

$$\Updownarrow \tag{16}$$

$$I_{Q1,RMS} = \sqrt{\cdot \frac{1}{N} \sum_{n=1}^{N} \left(\frac{k \cdot sin\left(\frac{n \cdot \pi}{N}\right)}{\eta \cdot Sum1} + 1 \right)^2} \cdot I_{Q2,RMS}$$

In the ordinary DC/DC converter with a two-switch topology the conduction losses are same for the two switches as stated earlier. A way of characterizing the difference in the conduction losses in the two-switch single-stage PFC converter is to investigate the ratio of the RMS^2 currents because of the proportionality to the conduction losses.

$$RMS^2_{Ratio} = \left(\frac{I_{Q2,RMS}}{I_{Q1,RMS}} \right)^2 = \left(\frac{1}{N} \sum_{n=1}^{N} \left(\frac{k \cdot sin\left(\frac{n \cdot \pi}{N}\right)}{\eta \cdot Sum1} + 1 \right)^2 \right)^{-1} \tag{17}$$

Using the same notation as in Eq.(8) the conduction losses in the two-switch single-stage PFC can be expressed as:

$$P_{Conduction,2Switch} = 2 \cdot R \cdot I^2_{Q1,RMS} + 2 \cdot R \cdot I^2_{Q1,RMS} \cdot RMS^2_{Ratio}$$

$$\Updownarrow \tag{18}$$

$$P_{Conduction,2Switch} = 2 \cdot R \cdot I^2_{Q1,RMS} \cdot \left(1 + RMS^2_{Ratio}\right)$$

Comparing the conduction losses of the single- and the two-switch approaches as in Eq.(8), the conduction loss ratio in the single-stage PFC can be expressed as :

$$\frac{P_{Conduction,1Switch}}{P_{Conduction,2Switch}} = \frac{2.6}{\left(1 + RM^2_{Ratio}\right)} \tag{19}$$

The RMS^2_{Ratio} given by Eq.(17) is plotted in figure 8 as a function of the ratio k (Eq.(15)). When the boost cell is operated in the DCM with a constant switch on-time, the

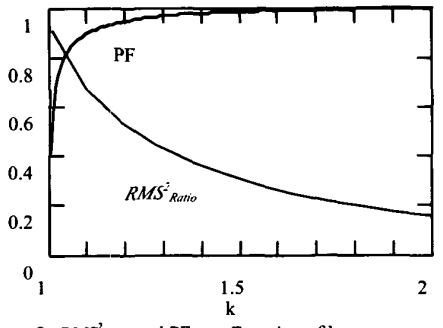

Figure 8. RMS^2_{Ratio} and PF as a Function of k

theoretical PF can be determined by the ratio k. The exact equations are given in [6] so the result of the calculations will only be plotted in figure 8 together with the RMS^2_{Ratio}.
Example: If the line voltage is 230V ($325V_{Peak}$) and the DC-bus voltage is 400V, then the ratio $k = 1.23$. This value of k translates into a PF = 0.95 and a $RMS^2_{Ratio} = 0.5$. Using Eq.(19), the reduction in conduction losses can be found:

$$\frac{P_{Conduction,1\,Switch}}{P_{Conduction,2\,Switch}} = \frac{2.6}{(1+0.5)} = 1.73 \qquad (20)$$

The result of Eq.(20) states that the conduction losses of a single-switch approach would give rise to an increase in the conduction losses of 73% as opposed to a two-switch solution using the same chip die area.

5. Key Design Parameters

The key element in designing the converter of figure 6 is to choose a desired DC-bus voltage V_{CB}. To keep the boost-cell in DCM operation the duty-factor is limited to:

$$D_{Max} = \frac{V_{CB} - \hat{V}_{IN}}{V_{CB}} \qquad (21)$$

Under all circumstances the duty-factor D must be below 0.5 because of the two-switch forward.
By taking into account the efficiency of the converter, the boost-inductor value is given by the desired output power:

$$L_{Boost} = \frac{\sum_{n=1}^{N} \hat{V}_{IN}^2 \cdot \sin^2\left(\frac{n\cdot\pi}{N}\right) \cdot \left(\frac{D^2 \cdot T \cdot V_{CB}}{V_{CB} - \hat{V}_{IN} \cdot \sin\left(\frac{n\cdot\pi}{N}\right)}\right)}{2 \cdot \frac{P_{OUT}}{\eta} \cdot N} \qquad (22)$$

The minimum value of the turns ratio n_{12} to keep the two-switch forward in the DCM is given by:

$$n_{12,Min} = \frac{V_{CB}}{V_{OUT}} \cdot D_{Max} \qquad (23)$$

To reduce the RMS-currents on the secondary side and minimize losses the best choice of n_{12} is close to the minimum value of Eq (23). On the other hand a minimum value of n_{12} causes use of higher voltage-rated rectifiers on the secondary side.
When the turns ratio has been selected the forward inductor can be calculated. Assuming converter efficiency of 100% will result in a DC-bus voltage smaller than expected. The reason for this, is that energy lost in the converter will affect the power balance. The calculated inductance ration given by Eq. (6) should be adjusted with the expected efficiency of the converter:

$$\left(\frac{L_{Boost}}{L_{Forward}}\right)^* = \left(\frac{L_{Boost}}{L_{Forward}}\right) \cdot \eta \qquad (24)$$

6. Experimental Results

To verify the abilities of the converter a prototype of the two-switch Boost-Forward PFC has been tested. A design of a 500W 70V output converter for 230V line input voltage (50Hz) has been implemented. The design and circuits parameters are:

$V_{CB} = 400V$, $n_{12} = 1.5$, $L_{Boost} = 63\mu H$, $L_{Forward} = 19\mu H$, $f_{Switch} = 100kHz$, $Q_1 = Q_2 =$ IRFP450LC, $d_1 =$ STTA8060, $d_3 = d_4 =$ BYT115.

As seen in figure 9 high efficiency is achieved over the full power range of the converter. Efficiency is over 88% from 80W – 320W and at full output power 86% is achieved. If more rugged power switches are used the efficiency at the high power levels can be increased but this will compromise the efficiency at the low levels. The idle power consumption is very low (< 2W) making the converter ideal for applications with large load variations.

The DC-bus voltage was measured to 397V-405W over the full power range.

The current waveform at full output power (485W) is shown in figure 10. With respect to the EN61000-3-2 this waveform will be classified as class D thus the relative limits of harmonic current applies. In figure 11 the harmonic content of the current is compared with the limits given by EN61000-3-2 at P_{IN} = 564W. The measured current harmonics are well below the limits.

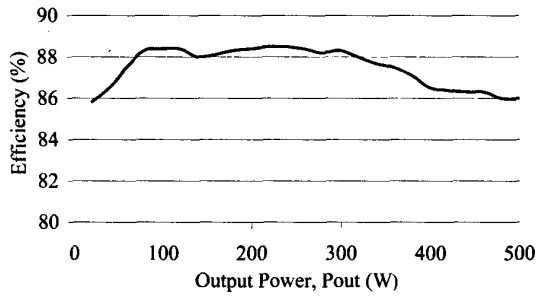

Figure 9. Measured Efficiency as a Function of Output Power.

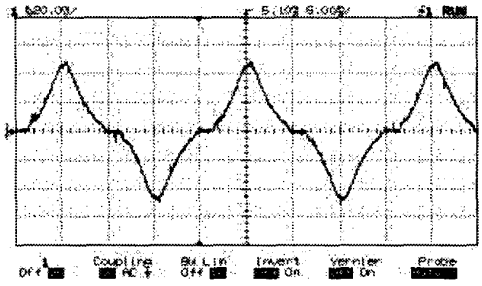

Figure 10. Measured Line Current of the Experimental Boost-Forward Converter at 564W Input. The PF was Measured to 0,947. Vertical Spacing: 2A/div, Horizontal Spacing: 5ms/div.

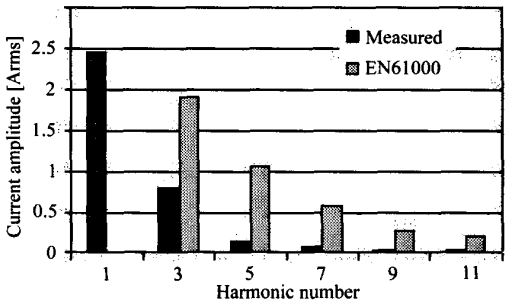

Figure 11. Measured Current Harmonics at 564W Input Power and the Limits Given by EN61000-3-2 Class D.

7 Conclusion

This paper draws the attention to the properties of the two-switch boost-forward topology as a high efficient Single-Stage PFC power supply. Further more the two-switch topology makes it possible to achieve high efficiency in the medium to high power range. Experimental results have shown efficiency above 85% in the power range of 30W-500W with good power factor and compliancy with the European norm EN61000-3-2.

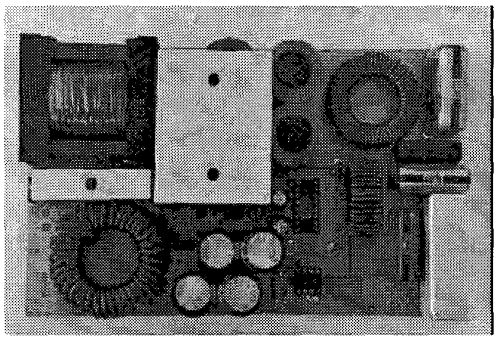

Figure 12. The Experimental Two-Switch Boost-forward Single-Stage PFC Power Supply.

Acknowledgments

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