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Digitally Controlled Envelope Tracking Power Supply for an RF Power Amplifier

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***Abstract* – A new Digital Self-Oscillating (DiSOM) modulator is presented in this paper. The advantage of the DiSOM is that it allows the sampling frequency of the digital compensator to be higher than the switching frequency, but it also has the ability to shape the quantization noise on the switching output due to clock frequency quantization. An envelope tracking power supply for an RF Power Amplifier (RFPA) can help improve system efficiency by reducing the power consumption of the RFPA. To show the advantage of the DiSOM over traditional counter based Digital PWM modulators two designs were compared in both simulation and by experiment. The results shows that the DiSOM could give an increase in open loop bandwidth by more than a factor of two and an reduce the closed loop output impedance of the power supply by a factor of 5 at the output filter resonance frequency.**

I. INTRODUCTION

The efficiency of an RF Power Amplifier (RFPA) transmitting an amplitude modulated signal can be improved by using an envelope tracking power supply that tracks the envelope of the RFPA. For a given instantaneous output power level, the RFPA supply current is constant and the power consumption is proportional to the input voltage. By adapting the supply voltage of the RFPA to the RF output amplitude the power consumption of the RFPA can be reduced considerably. Fig. 1 shows a block diagram of how a RFPA can be combined with an envelope tracking supply. The baseband processor and modulator block generates the RF input for RFPA and the RF envelope signal, which is used as a reference for the tracking power supply. The tracking power supply is in this case digitally controlled. The tracking power supply generates an output voltage proportional to the reference signal. The bandwidth of the tracking power supply is important in two ways. Firstly high control loop bandwidth makes it possible for the tracking power supply to generate an output voltage with short rise and fall times. Secondly high control loop bandwidth will result in low output impedance which is important so as not to distort the RF output because of fluctuations in the RFPA supply voltage. For the same reason it is desirable to have low ripple voltage on the power supply output which would generally be solved by using a large output capacitance and high switching frequency. If on the other hand the tracking power supply must be able to track a high frequency reference signal a large output capacitor is undesirable.

Several papers have proposed solutions for similar application using either analogue or digital control schemes [1-4]. The output voltage and power ranges of the different solutions previously published vary largely and it is therefore hard to make comparisons. Reference [1] presents a combination of a digitally controlled DC/DC converter and an RFPA for battery powered applications. The DC/DC converter does not track the envelope of the RF output but is used to optimize the DC supply voltage to achieve maximum efficiency. Envelope tracking power supplies are presented in [2-4] with closed loop bandwidth ranging from 3.5kHz to 50kHz. The preferred converter in [2] and [4] is a four phase interleaved buck converter. This converter topology was chosen in order to reduce output voltage ripple whereas [4] uses a single Buck stage with a 4^{th} order output filter. The digitally controlled solution of [3] has the lowest open loop control bandwidth and shows the need for a better digital control solution.

In this paper a new Digital Self-Oscillating Modulator (DiSOM) is presented enabling the design of a high bandwidth digitally controlled envelope tracking power supply. The advantage of the DiSOM is that it allows the digital compensator to sample the output voltage at a sample frequency which is higher than the switching frequency. To show the advantage of the DiSOM over more traditional counter based digital PWM modulators (DPWM) two designs have been simulated and tested experimentally. The first design is based on the Texas Instruments Digital Signal Controller (DSC) TMS320F2801, which has a special high resolution counter based DPWM, and the second design is based on the DiSOM modulator implemented in an FPGA.

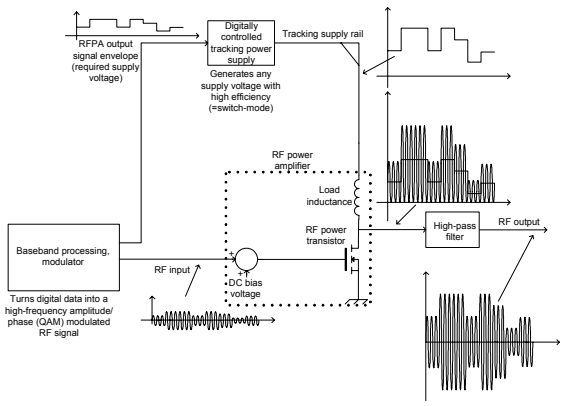

Fig. 1: Block diagram of RFPA system with tracking power supply

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TABLE I lists the basic specifications of the tracking power supply and the RFPA used in the comparison of DiSOM versus DPWM. The specifications does not address a specific application but was selected to represent a typical RFPA application on which it would suitable to compare the DiSOM against the typical counter based DPWM.

TABLE I
RFPA AND TRACKING POWER SUPPLY SPECIFICATIONS

Parameter	Value
RFPA output power - Continuous wave	80W
RFPA supply voltage	12 – 28V
RFPA supply current – average	1A
RFPA supply current – peak	5A
Frequency range of interest	DC – 50kHz

No specific design goals have been set for other important parameters such as output impedance and reference to output bandwidth and the goal is to achieve the best possible performance, i.e. the lowest possible output impedance and the highest possible reference to output bandwidth.

II. THE DISOM MODULATOR

Designing a digital PWM modulator with high switching frequency and high duty cycle resolution has been the subject of intense research in the past years. Many different solutions have been proposed and they almost all have in common that the basic carrier is generated by a counter [5-7]. Fig. 2 shows a block diagram together with a representation of the basic operation of a counter based digital PWM modulator (DPWM). The PWM output is generated by the S-R latch which is set to high when the counter value is equal to zero. The duty cycle value *d(n)* is read into the shadow register at the beginning of the switching period, i.e. at the same time the PWM output is set to high. The shadow register is used to avoid spurious switching in the middle of switching period if *d(n)* is changed by the digital compensator. The PWM output is reset to low when the counter value is equal to the duty cycle value in the shadow register. The counter is a free running counter that will reset to zero when it reaches a predefined value, which controls the duration of the switching period. The maximum sampling frequency of the digital compensator is limited to the switching frequency because the shadow is updated once per switching period. In practice it is possible to sample the output voltage at a higher rate than the switching but it will not improve the control loop bandwidth of the switching converter since the update rate of the control signal is limited by the shadow register.

The basic operation of the counter based DPWM in Fig. 2 is shown below the block diagram. At the time the counter is reset to zero the value of *d(n)*, i.e. 6, is read into the shadow register. Even though the value of *d(n)* is changed from 6 to 4 in the middle of the first switching period the duty cycle is still 6/8 (0.75) because of the shadow register. In the next switching period the duty cycle is 4/8 (0.5).

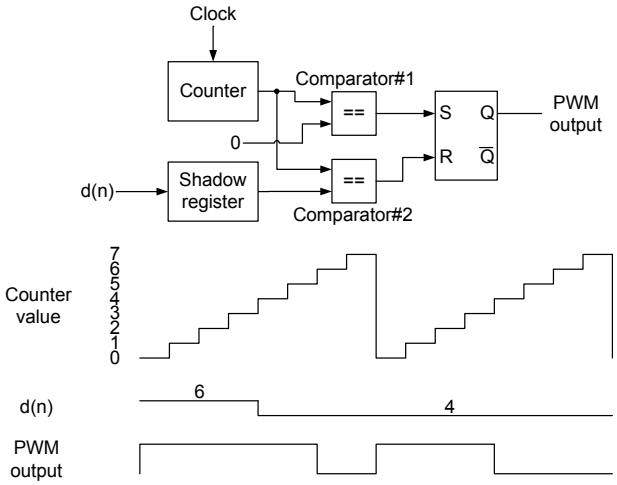

Fig. 2: Block diagram and priciple of operation for counter based DPWM

A block diagram of the Digital Self-Oscillating Modulator is shown in Fig. 3. This is just one of a family of Digital Self-Oscillating Modulators described in [8]. The general features of the DiSOM family is that it includes one or more control loops that include the switching output in the control loop and it has no free running counter to set the switching frequency. The DiSOM of Fig. 3 is characterised by being a purely digital modulator that receives a duty cycle command (*Ref*) from en external source, typically the digital compensator that calculates the required duty cycle to adjust the output voltage to the reference setpoint.

The DiSOM consists of three main blocks. The first block is a comparator with hysteresis that generates the switching output based on the input signal, that is called the carrier. The carrier is generated by the main forward block (MFW), which in this case is a digital integrator. The integrator input is the difference between the signal generated by main feedback block (MFB) and the *Ref* input. In this case the MFB is a simple multiplication with no frequency dependency.

Fig. 4 shows an example of the carrier signal and switching output of the DiSOM modulator for three different duty cycle values. The carrier is a trianguler wave form as would be expected since the integrator is integrating a square wave. One of the defining features of the DiSOM is that the switching frequency is dependent of the duty cycle. The switching frequency can be expressed as a function of the duty cycle

$$f_{sw}(D) = \frac{2^n \cdot f_{clock}}{Window} \cdot \left(D - D^2\right) \qquad (3)$$

where D is the duty cycle, n is the number of bits used to represent the *Ref* input, f_{clock} is the clock frequency of the integrator and *Window* is the hysteresis window [9].

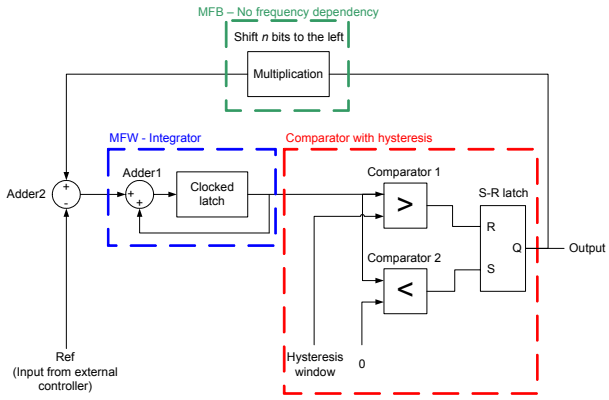

Fig. 3: Block diagram of the DiSOM modulator

The structure of the DiSOM modulator allows the *Ref* input to be changed at any time. If the *Ref* input is changed during a switching period it will affect the slope of the carrier but it will not directly affect the switching output.

Another important feature of the DiSOM is that the switching output is fed back to the integrator whereby any noise due to clock frequency quantization is integrated. Thus the DiSOM is automatically correcting for quantization noise on the switching output. It can be compared to a noise shaper used in digital audio to reduce total harmonic distortion. The choice of transfer function for the MFW and MFB can be used to shape the quantization noise spectrum on the switching output.

III. DPWM VERSUS DISOM

Two different control schemes for the envelope tracking power supply are presented in this section. The first design is based on the Texas Instruments TMS320F2801 Digital Signal Controller (DSC) and uses the counter based high resolution DPWM module included in the DSC. The TMS320F2801 has a clock frequency of 100MHz and includes peripherals such as six high resolution DPWM modules and a 12 bit Analogue to Digital Converter (ADC) with a sampling time of 160 ns.

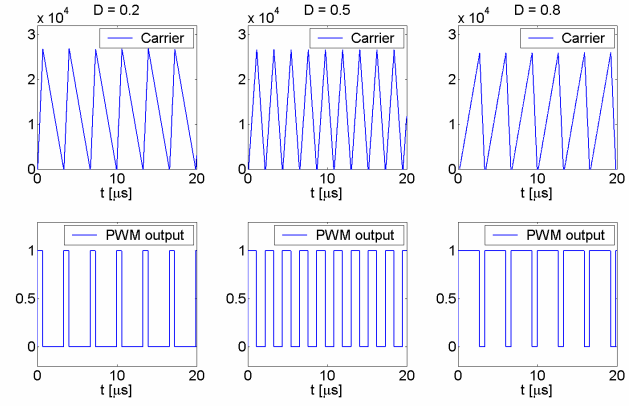

Fig. 4: DiSOM waveforms for three different duty cycle values

Fig. 5 shows a block diagram of the first design. The power conversion stage is a Buck converter with synchronous rectification. The output voltage is subtracted from the analogue reference voltage before the error voltage is sampled by the ADC of the TMS320F2801. The analogue reference is lowpass filtered in order to avoid large overshoot and ringing on the output voltage. The phase margin of the control loop would typically have to be greater than 90 degrees if a square wave reference is applied directly to the compensator and no overshoot is allowed. By performing the initial subtraction of the output and reference voltage the ADC only needs to sample one voltage, i.e. the error voltage, rather than both the reference voltage and the output voltage. If a digital reference was supplied it would be preferable to sample the output voltage directly and do the subtraction in the DSC.

A digital PID compensator with two zeroes and an integrator (see (2)) has been written in C code and it has an execution time of approximately 1µs including the 160ns sampling time of the ADC. The control algorithm samples the error signal at the beginning of a switching period and calculates the duty cycle before the beginning of the next switching period.

$$G_{comp}(z) = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2}}{1 - z^{-1}} \qquad (2)$$

The second design is the DiSOM based design with a custom designed digital compensator implemented in an FPGA. The FPGA used is the LCMXO1200C from Lattice Semiconductor and it has a clock frequency of 50 MHz. The FPGA development board used in the prototype is a 10 bit pipelined ADC (ADC10065) from National Semiconductors.

Once again the output voltage is subtracted from the reference in an analogue difference amplifier as in the DPWM based design. This method was actually adapted because the pipelined ADC has an input voltage range from 0.95V to 1.95V. The pipelined ADC therefore would not be able to measure an attenuated version of the output voltage directly since it can not measure voltages down to zero Volts.

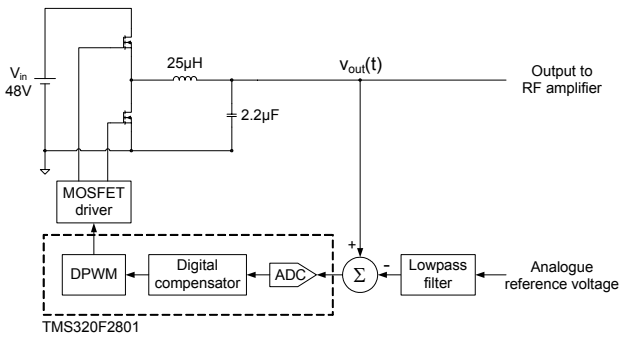

Fig. 5: Block diagram for the TMS320F2801 DSC based design

The digital PID compensator of the DiSOM based design has the same basic transfer function as the DPWM based design but it is implemented using lookup tables rather than a hardware multiplier/accumulator module. The lookup tables stores the results of the three multiplications of b_0, b_1 and b_2 with the current and past error signals. A special ADC decoding scheme has been implemented to reduce the size of the lookup tables (see Fig. 7). The idea behind the decoding scheme is that high resolution is needed when the error signal is close to 0 but as the error increases it is acceptable to increase the quantization steps. Alternatively the error signal could have been limited to a small range around 0 but it was found that this slowed down the step response of the converter if a large step occurs on the reference. The internal resolution of the digital PID compensator is 24 bits and the ADC decoding schemes has 85 values, resulting in a total memory allocation for the lookup tables of 765 bytes. A detailed description of a similar lookup table based PID compensator can be found in [9].

The main difference between the two designs is that the sampling frequency of the DiSOM based implementation is twice that of the DPWM based design and that the computational time of the digital compensator is shorter for the DiSOM based design. The system specifications for the two digital controller implementations are given in TABLE II.

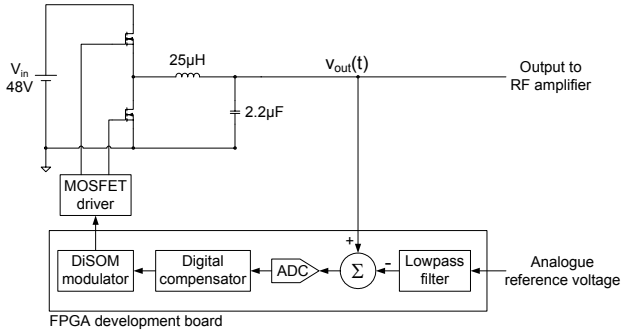

Fig. 6: Block diagram for the DiSOM based design

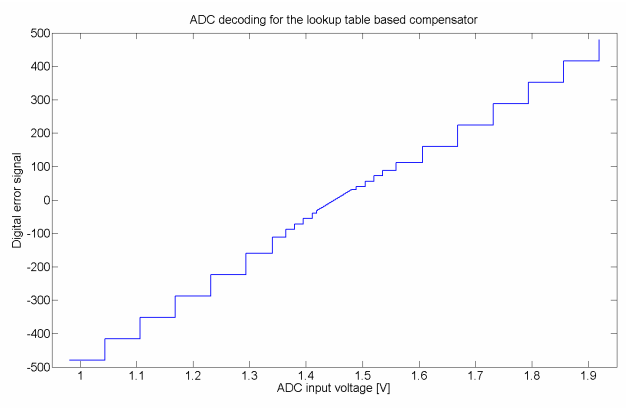

Fig. 7: ADC decoding scheme for the look table based compensator

TABLE II
DIGITAL CONTROLLER PARAMETERS

Parameter	DPWM	DiSOM
Clock frequency	100 MHz	50 MHz
Sampling frequency	500 kHz	1 MHz
Switching frequency	500 kHz	500 kHz*
Duty cycle command resolution	13.6 bit	10 bit
PID compensator internal resolution	32 bit	24 bit
Sampling + computational time	2 µs	200 ns
b_0	20.875	4.875
b_1	-39.1875	-9.28125
b_2	19.625	4.5

*Nominal switching frequency @ D = 0.5. Hysteresis window = 25600

IV. SIMULATIONS AND EXPERIMENTAL RESULTS

A set of hardware specifications for the envelope tracking converter have been selected and the system has been simulated in Matlab/Simulink before the prototype hardware was build and tested. The input voltage is 48V and the output voltage range is 10 to 30V. The output filter inductor is 25µH and the output capacitor is 2.2µF which gives a filter resonance frequency of 21.5kHz. All simulations and measurements have been made under no-load conditions, which is the worst case condition for the control loop.

The Matlab/Simulink models for the DPWM and DiSOM design are switching models and take into account such things as quantization in the fixed point calculations, computational delays and the series resistance of the inductor to make the model as accurate as possible.

Fig. 8 shows the output ripple voltage as a function of duty cycle. The simulation has been performed by setting the reference voltage to a level that corresponds to the specified duty cycle and measuring the peak-peak ripple voltage. The simulation has been performed a number of times to generate the plot of in Fig. 8. The simulation of the output ripple shows that the maximum ripple voltage of the DPWM design is 100mV while the maximum ripple voltage of the DiSOM design is 350mV. This is clearly in favour of the DPWM design and the reason it has lower ripple voltage for duty cycle values close to 0 and 1 is that the switching frequency is constant. The switching frequency of the DiSOM design falls to approximately 150kHz for duty cycle values of 0.1 and 0.9 (see Fig. 9) whereas the switching frequency of the DPWM is constant at 500kHz. It should be noted that the duty cycle will vary from 0.2 to 0.6 in the defined output voltage range and that the maximum ripple voltage in this case is approximately 200mV. The ripple voltage is in general quite high for the application and it would be advantageous to increase either the switching frequency or the size of the output capacitor to improve the performance of the system.

The loop gain and output impedance and step response have both been simulated and tested experimentally. Fig. 10

shows a picture of the prototype PCBs of the DiSOM based design. The same Buck converter power stage was used with the Texas Instruments TMS320F2801 ezDSP board and a small PCB with the analogue difference amplifier for the DPWM based prototype.

The simulation and measurement results for the loop gain are presented in Fig. 11 and Fig. 12 for the DPWM and DiSOM solutions. The resonance frequency of the output filter is slightly higher in the measurements, which is due to component tolerances. The open loop bandwidth and phase margin of the DPWM prototype are 43.2kHz and 30.7 degrees respectively and the gain margin is 3.9dB at a frequency of 66.5kHz. For the DiSOM prototype the open loop bandwidth is 97.2kHz with a phase margin of 36.3 degrees. The gain margin of the DiSOM prototype is 4.6dB at 178kHz. The DiSOM prototype outperforms the DPWM prototype by more than a factor of 2 in terms of open loop bandwidth.

The simulation and measurement results for the output impedance are shown in Fig. 13. The peak output impedance for the DPWM prototype is 10Ω and for the DiSOM prototype it is 1.4Ω, which is an improvement by a factor of 7. The output impedance of the DiSOM prototype is approximately 5 times lower at the output filter resonance frequency.

One of the big questions still to be answered regarding digital control of DC/DC converters is whether it can outperform analogue control. Reference [10] presents three different analogue control solutions for an envelope tracking power supply with similar specifications as those used in this paper. The open loop bandwidth and output impedance of the DiSOM prototype is comparable to the poorest of the three analogue control solutions, but there is still some way to go before it can compete with state-of-the-art analogue control solutions.

The simulated step responses of the DPWM and DiSOM solution (see Fig. 14) shows an approximate rise time of 60µs but with the difference that the step response of the DiSOM solution is smooth monotonously rising while the DPWM solution has some ringing. The simulated step response of the DPWM and DiSOM solution corresponds well with the measurements of Fig. 15 and Fig. 16.

The rise time of the step response is limited by the lowpass filter that lowpass filters the reference voltage. The lowpass filter in both designs has a cut off frequency of 10kHz, which limits the rise time to approximately 60µs as both simulations and measurements show. Faster step responses could therefore be achieved by increasing the cut off frequency but at the cost of some overshoot and ringing on the output voltage. Faster step response is not necessarily required [11] depending on the specific application the envelope tracking power supply is designed for, but it will help improve overall system efficiency in some applications.

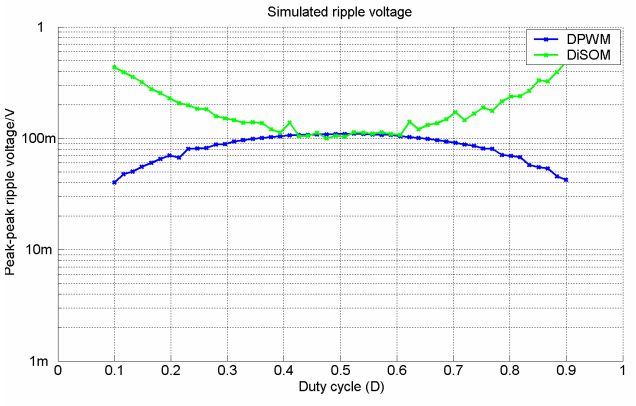

Fig. 8: Simulated ripple voltage versus duty cycle

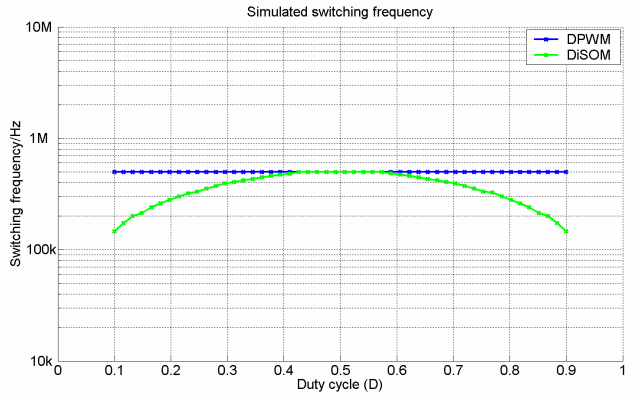

Fig. 9: Simulated switching frequency versus duty cycle

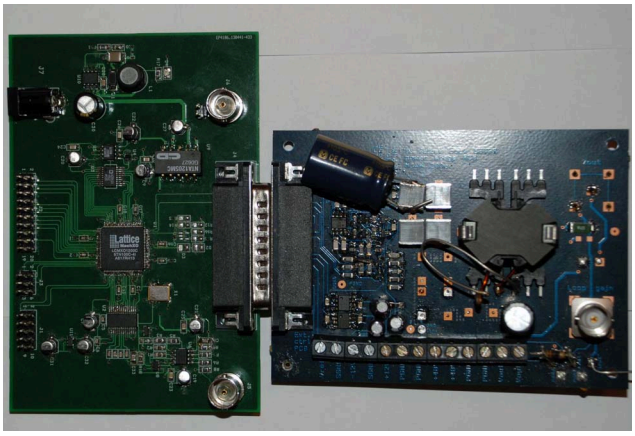

Fig. 10: Prototype PCB for the DiSOM solution. FPGA development board (right) and Buck converter power stage (left)

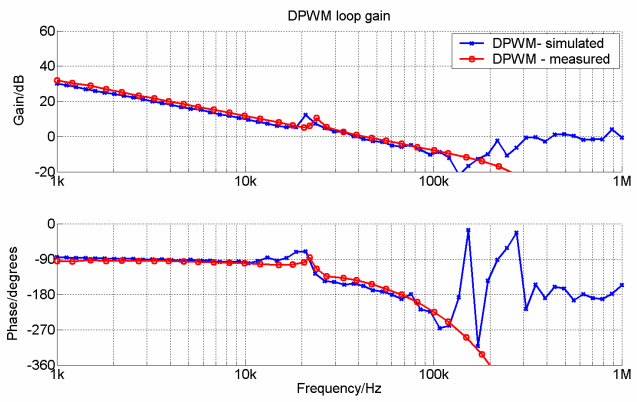

Fig. 11: Simulated and measured loop gain for the DPWM implementation

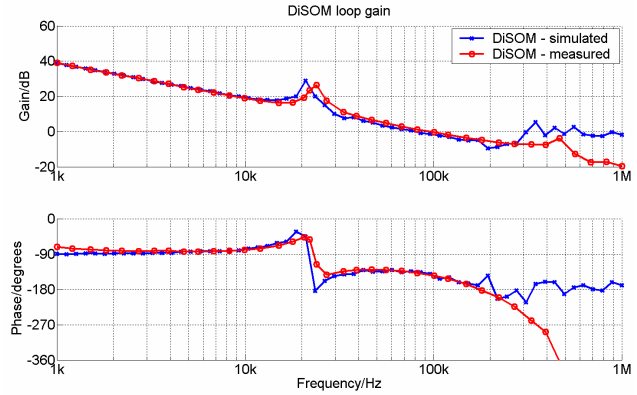

Fig. 12: Simulated and measured loop gain for the DiSOM implementation

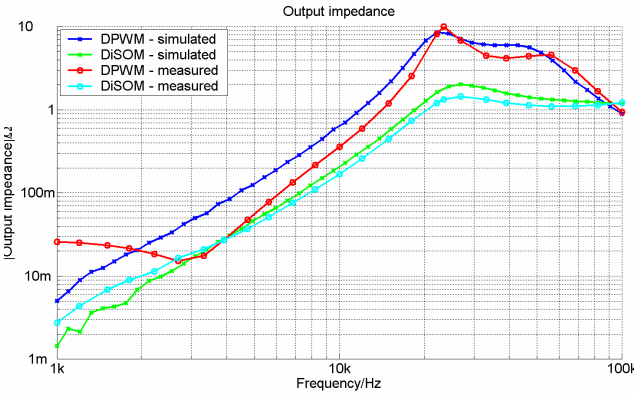

Fig. 13: Simulated and measured output impedance versus frequency

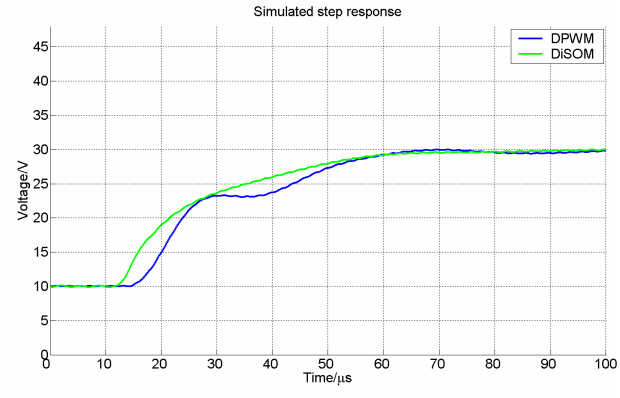

Fig. 14: Simulated step response

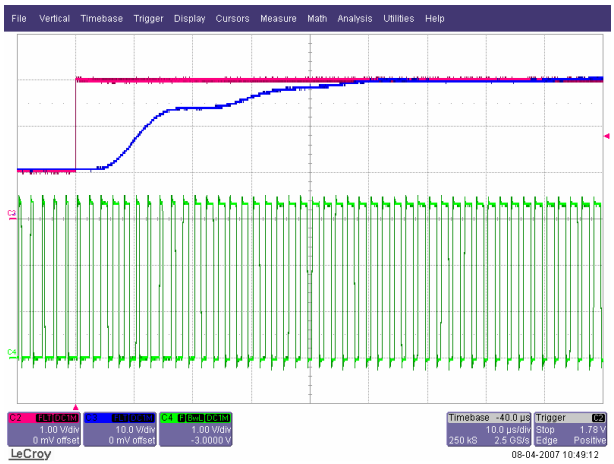

Fig. 15: Positive reference step for the TMS320F2808 DSP based design
C2: Reference voltage (1 V/div)
C3: Output voltage (10 V/div)
C4: High side PWM signal (1 V/div)
Time scale: 10 µs/div

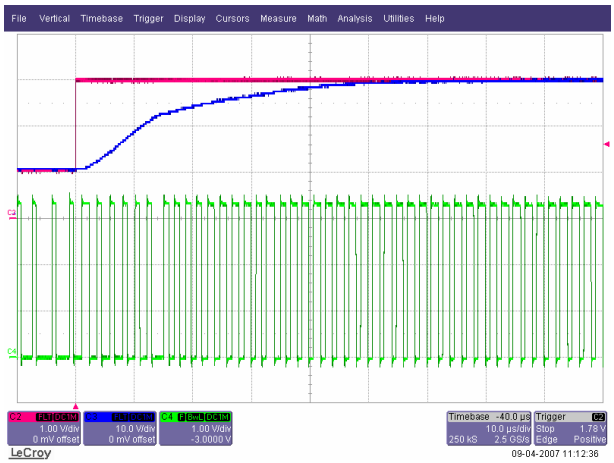

Fig. 16: Positive reference step for the DiSOM based design
C2: Reference voltage (1 V/div)
C3: Output voltage (10 V/div)
C4: High side PWM signal (1 V/div)
Time scale: 10 µs/div

V. CONCLUSION

A new Self-Oscillating modulator (DiSOM) has been presented and it has been shown that the DiSOM modulator allows higher sampling frequencies in a digital control scheme for a DC/DC converter than the traditional counter base Digital PWM (DPWM) modulator.

An envelope tracking power supply for an RF Power Amplifier has been designed and a counter based DPWM control scheme has been compared with the DiSOM based control scheme in simulations and by experimental verification.

The comparison shows that it is possible to more than double the open loop bandwidth with the DiSOM based design. The maximum output impedance of the DiSOM based prototype design is more than 7 times lower than that of the DPWM based prototype.

The step response of the envelope tracking converter has a rise time that is limited because the reference voltage is passed through a lowpass filter with a cut off frequency of 10kHz. The step response of the DiSOM based design is monotonously rising whereas the DPWM based design has some ringing on the step response.

The maximum ripple voltage was twice as high for the DiSOM based design compared to the DPWM based design. The reason being, that the switching frequency is dependent on the duty cycle of the PWM signal and falls towards zero for duty cycles of 0 and 1. It is possible to make the switching frequency of the DiSOM constant by changing the hysteresis window as a function of the duty cycle command or with a phase locked loop.

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