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# Black Silicon realized by reactive ion etching (ICP) without platen power

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**Abstract** -- Reflectance and minority carrier lifetime were measured for black silicon textured by different inductively coupled plasma (ICP) reactive ion etching processes without any capacitively coupled power (platen power). Reflectance was reduced to below 5% after 2 minutes and below 4% after 3 minutes etch time, with several accessible routes to lower reflectance identified. Black silicon wafers were passivated by atomic-layer deposited (ALD)  $\text{Al}_2\text{O}_3$  and minority carrier lifetime was measured to 2.1 ms for 2 minutes texturing, while minority carrier lifetimes were well below 1.0 ms for etch times in the 5-20 min range. Samples measured immediately after ALD activation, show minority carrier lifetime above 3 ms for RIE process time between 1.5 and 3 min and between 2.5 and 3 ms for etching times above 3 min. These results indicate that ultra-low reflectance and minority carrier lifetime on par with those of the best passivated solar cells to date may be achieved after texturing for just 2 min.

**Keywords** -- black silicon, minority carrier lifetime nanostructures, reactive ion etching, reflectance.

## I. INTRODUCTION

Black silicon [1, 2] has shown great potential as a texturing method for silicon (Si) photovoltaics due to ultra-low reflectance for mono- and multi-crystalline Si at normal and varying incident angle [3]. In particular the use of mask-less reactive ion etching (RIE) has yielded promising solar cell efficiencies for laser-doped selective emitter solar cells [4], TOPCon passivated [5] and interdigitated back contact cells [6] with power conversion efficiencies in the range 18-22%. Furthermore, RIE texturing has commercial potential, since it is a mask-less, single-step process, which potentially makes it scalable. Black silicon may be used for efficient texturing of diamond-wire cut multi-crystalline Si wafers and also very thin Si cells, both of which could play a significant role in the future solar cell market. However, the limiting factor of black Si solar cell efficiency seems to be increased surface recombination resulting in lower power conversion efficiencies compared to the best conventionally-textured Si solar cells. The increased surface recombination arises from the etch damage induced during the RIE texturing process. Recently, improved minority carrier lifetime results were realized by reducing the capacitively coupled (platen) power in the ICP RIE process [7, 8], thus reducing surface damage and as a result reducing surface recombination. A logical continuation of this promising result would be to completely remove the platen power from the etch process,

and rely exclusively on the inductively coupled (coil) power. Based on state-of-the-art results for black silicon realized by RIE it is not obvious whether such process may produce sufficiently low reflectance and how the minority carrier lifetime of wafers would compare to that of other RIE texturing processes. This paper investigates reflectance and minority carrier lifetime of Si surfaces textured by RIE with varying platen power and etching time.

## II. METHODS

All wafers were 150 mm, 500  $\mu\text{m}$  thick CZ p-type Si (100). Wafers were textured using an ICP RIE tool (MP0637) from SPTS with a process temperature of 0°C,  $\text{SF}_6$  and  $\text{O}_2$  plasma with gas flow ratio of  $\text{SF}_6:\text{O}_2 \sim 1:1$  at 74 mTorr pressure. The coil power was fixed at 1500 W, except in the case where 100 W platen power was used and the coil power was set to 0 W. Platen power was varied between 0 and 100 W and process time was varied between 1 and 20 min.

After texturing the wafers were cleaned using a standard RCA procedure where the final HF dip was omitted in order to keep a chemically grown  $\text{SiO}_2$  layer. Wafers were passivated with  $\text{Al}_2\text{O}_3$  using a thermal atomic layer deposition (ALD) R200 tool from Picosun. The ALD process was 380 cycles using water and TMA as precursors in all cases. The process temperature was 200 °C. After passivation, samples were annealed in a Tempress furnace at 400°C for 10 minutes.

Minority carrier lifetime was measured with a Freiberg Instruments MDPmap tool. Lifetime values were extracted at an injection level of  $10^{15} \text{ cm}^{-3}$  and averaged over a 100 mm diameter area in the center of each 150 mm wafer, due to known edge effects of the passivation process.

The total (diffuse + specular) optical reflectance  $R$  was measured using a UV spectrophotometer (UV-2600, Shimadzu Co.), equipped with an integrating sphere and using a 200 nm Al film on Si as reference.

## III. RESULTS

Figure 1 shows SEM-images of the Si surface after 3 minutes RIE texturing. The nanostructures are conical-like

hillocks with structure heights of  $\sim 200$  nm and pitch between structures of  $\sim 200$  nm.

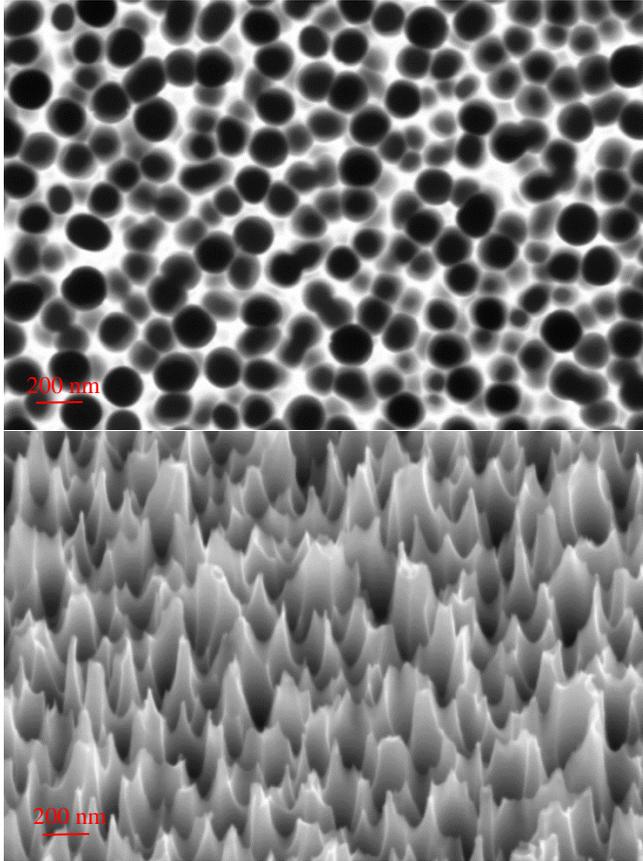


Fig.1. Top: Top-view scanning electron microscope (SEM) image from the top of the Si surface after 3 min etch time, without platen power. Bottom: Same surface imaged at a  $40^\circ$  tilt.

Figure 2 shows total (diffuse + specular) reflectance as function of wavelength in the range 300-1200 nm measured at normal incidence for different RIE process times.

For the sample with 1.5 min RIE texturing reflectance is above 5% for wavelengths in the range 300-700 nm and above 10% for wavelengths above 700 nm, whereas the sample with 2 min texturing reflectance is reduced to below 5% in the entire relevant wavelength range 300-1100 nm. The bottom panel of Fig. 2 shows that  $R$  decreases to below 4% in the entire wavelength range when RIE process time is increased above 3 minutes.

The measured reflectance is slightly higher than what has been obtained previously using ‘standard’ RIE texturing [2-8]. Although the focus of this work is the elimination of platen power from the RIE process to obtain acceptable reflectance and minority carrier lifetime as a result, it is worth mentioning a few plausible causes for the slightly higher reflectance values: (1) Mirror-polished CZ Si wafers were used in this work. These wafers have a higher reflectance than saw-damaged removed, solar-grade Si wafers. (2) The reference sample used for the reflectance

measurement was a Si wafer coated with  $\sim 200$  nm Al, which is not a reference yielding 100% reflectance, although this was assumed in the data treatment. This deviation accounts for an over-estimation of reflectance of  $\sim 0.5\%$  points.

(3) Only the  $\sim 30$  nm  $\text{Al}_2\text{O}_3$  deposited by ALD was used as anti-reflective coating. We expect that  $R$  can be decreased further by *e.g.* depositing  $\sim 45$  nm PECVD  $\text{SiN}_x\text{:H}$  on top of the  $\text{Al}_2\text{O}_3$ .

Figure 3 shows minority carrier lifetime as function of RIE process time. The measurements were done immediately after the annealing, subsequent to ALD passivation, and then again after  $\sim 200$  hours in order to evaluate the stabilized minority carrier lifetime. Minority carrier lifetime was measured several times during the 200 hours in order to verify that the lifetime values did in fact stabilize.

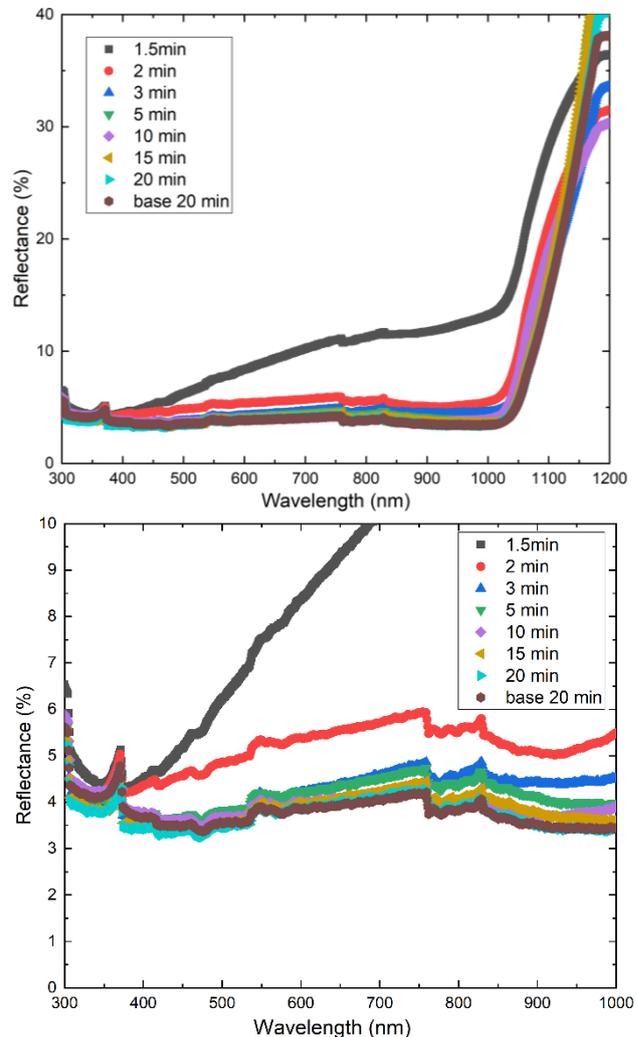


Fig.2. Reflectance as function of wavelength for Si wafers RIE-textured for different times. The bottom graph shows the same measurements in the range 300-800 nm. The reflectance is below 3% for all samples with etch time above 2 min. ‘Base 20 min’ indicates the surface textured using platen power.

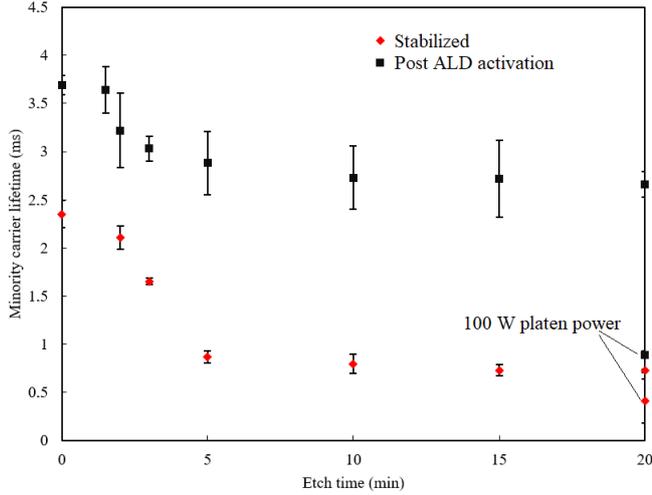


Fig.3 Minority carrier lifetime as function of RIE process time measured immediately after annealing of the ALD-passivated samples (black squares) and after ~ 200 hours of stabilization (red diamonds).

For the stabilized measurements, the lifetime is above 2.1 ms for 2 min and above 1.6 ms for 3 min RIE process time, but below 1.0 ms for etching times between 5 and 20 min. The minority carrier lifetime of the polished reference sample is 2.35 ms. Within standard deviations the minority carrier lifetime of the sample textured for 2 min is comparable to that of the planar, non-textured sample. The minority carrier lifetime of the sample with 100 W platen power is significantly lower than the sample without platen power at the same etching time (20 min). These results illustrate the effect of platen power on the resulting minority carrier lifetime of RIE-textured samples. Furthermore, based on combined reflectance and minority carrier lifetime measurements, it appears that RIE texturing for 2-3 min provides a good compromise between optical and electrical properties.

For the post-ALD activation measurements, the minority carrier lifetime is above 3 ms for RIE process time between 1.5 and 3 min and between 2.5 and 3 ms for etching times above 3 min. The minority carrier lifetime of the polished reference sample is 3.75 ms for comparison, while the lifetime of the sample with 100 W platen power is below 1 ms, which follows the trend for the stabilized measurements.

The significant difference between the lifetime values measured immediately after activation of the  $\text{Al}_2\text{O}_3$  passivation layer and after a stabilization period indicates that even higher minority carrier lifetimes are obtainable if the degradation of the ALD  $\text{Al}_2\text{O}_3$  film, assumed to cause the decrease in measured lifetime over time, is avoided. Assuming that the degradation is related to water adsorption in the alumina film, a possible solution could be to add a capping layer such as PECVD  $\text{SiN}_x\text{:H}$ , which would act as a barrier for water vapor, besides improving the anti-reflective properties of the stack.

In order to determine the surface recombination velocity (SRV) of the differently textured front surfaces, the following equation is used

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_b} + \frac{(S_f + S_r)}{W}, \quad (1)$$

where  $\tau_{\text{eff}}$  is the effective minority carrier lifetime,  $\tau_b$  is the bulk lifetime,  $W$  is the sample thickness and  $S_f$  and  $S_r$  are the SRV of the front and rear surfaces, respectively.

The first term Eq. 1 may be neglected assuming that  $\tau_b \gg \tau_{\text{eff}}$ . The thickness of the wafers was 500  $\mu\text{m}$ . For the stabilized measurements, SRV on the front of the sample textured for 2 minutes is  $S_f \sim 13$  cm/s, taking into account the non-textured SRV of the rear  $S_r \sim 11$  cm/s and re-writing Eq. 1 to

$$S_f \cong \frac{W}{\tau_{\text{eff}}} - S_r. \quad (2)$$

For etching times above 5 min,  $S_f$  is in the range 47-59 cm/s.

For the post ALD activation measurements SRV is below 10 cm/s for the samples textured for 2-3 min, and between 10 and 12 cm/s for 3-20 min texturing, while SRV of the sample with 100 W platen power in this case is 49 cm/s.

#### IV. CONCLUSION

Reflectance and minority carrier lifetime was measured for black silicon textured by different reactive ion etching processes with and without the use of platen power. Reflectance was reduced to below 5% after 2 min and below 4% after 3 min RIE process time, where three routes were identified for further reduction of the reflectance. Black silicon wafers passivated by ALD  $\text{Al}_2\text{O}_3$  show a minority carrier lifetime of 2.1 ms and SRV of 13 cm/s after 2 min texturing. Minority carrier lifetimes were well below 1.0 ms and SRV above 47 cm/s for RIE process times above 5 min. When measured immediately after ALD activation, minority carrier lifetimes were as high as 3.7 ms and SRV below 10 cm/s.

The results indicate that low reflectance and high effective minority carrier lifetimes enable the achievement of high-efficiency Si solar cells after just 2 min RIE texturing.

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