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DERIVATION AND ANALYSIS OF A LOW-COST, HIGH-PERFORMANCE ANALOGUE BPCM CONTROL SCHEME FOR CLASS-D AUDIO POWER AMPLIFIERS

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This paper presents a low-cost analogue control scheme for class-D audio power amplifiers. The scheme is based around bandpass current-mode (BPCM) control, and provides ample stability margins and low distortion over a wide range of operating conditions. Implementation is very simple and does not require the use of operational amplifiers. Small-signal behavior of the controller is accurately predicted, and design is carried out using standard transfer function based linear control methodology. Effectiveness of the approach is demonstrated via a 60W/8Ω single-ended switching amplifier with THD+N of typically 0.02%.

I. INTRODUCTION

Class-D audio power amplifier technology is presently under continuous development, and improved techniques and products appear frequently. Advantage is taken of the very high efficiency (in comparison with linear amplifiers) while inherent problems with distortion and EMI are brought under control through the application of specialist knowledge.

Within the field of self-oscillating analogue control of class-D audio power amplifiers, a lot of high-performance schemes have been demonstrated [1], [2], [3], [4] each with different levels of complexity, distortion, and control loop stability. In comparison with all-digital solutions, the self-oscillating analogue controllers still provide the highest performance since amplifier power stage and output filter non-linearities can be relatively easily compensated for. All-digital solutions, on the other hand, presently need to rely on very accurate PCM-to-PWM converters and power stages, as well as low-distortion output filters, to achieve low distortion.

This paper presents an analogue control scheme that emphasizes simplicity, low cost, and unconditional stability. The approach is based on hysteresis control [5] and bandpass current-mode control [6] and is analyzed and explained from a small-signal point-of-view. The paper furthermore attempts to provide a transparent example of class-D amplifier controller design.

II. BASIC APPROACH

In order to minimize cost of the amplifier, the zobel network normally used to control output filter Q has to be removed. This leaves a potentially undamped output filter, which can be perfectly dealt with using a combination of inductor current and output voltage feedback. The drawback in using current feedback is the requirement for current measurement via a resistive device. This is typically lossy, noisy, and expensive and therefore not suitable for this application. An alternative, where the DC component of the measured current is unimportant, is using current estimation via inductor voltage integration [7], [8]. True integration of the inductor voltage is impossible [7] due to the lack of DC feedback, so integration effectively has to mean low-pass-filtering. This can be done with a single RC filter, which is inarguably a low-cost solution. It is assumed that adding a simple extra winding to a machine-wound inductor will not increase cost noticeably.

Using current estimate feedback and output voltage feedback, the closed-loop system is thus potentially well damped without resistive sensing or filter damping. The use of band-limited current feedback is the logical reason behind the use of the "bandpass current-mode" term.

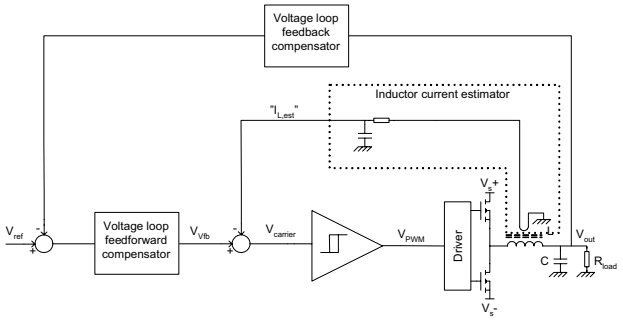

Figure 1 Basic structure of the proposed control scheme

III. DERIVATION OF PROPOSED CONTROL SCHEME

The basic control scheme derived so far is shown in Figure 1, consisting of estimated inductor current feedback and output voltage control via a suitable compensator. The following questions need answers, not in prior art:

- How does the closed BPCM loop behave from a small-signal point-of-view?
- How should the current estimator time constant be chosen?
- What should the voltage loop compensator look like?

The BPCM loop considered is shown in Figure 2.

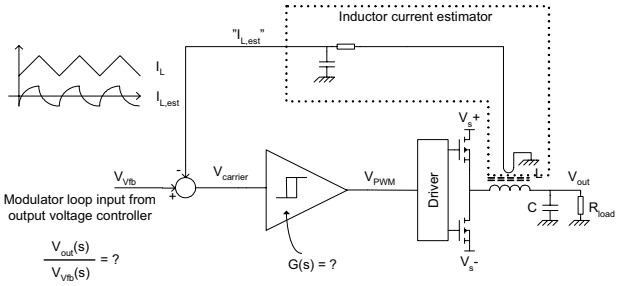

Figure 2 Principal BPCM loop as proposed

The model of the hysteresis comparator/power stage used in [7] has been found to lead to poor matching between expected and measured closed-loop parameters with loop parameters as found in switching amplifiers. The assumption that the hysteresis comparator/power stage behaves as a PWM modulator (as per [9]) thus appears invalid:

$$G(s) = \frac{\langle V_{PWM} \rangle(s)}{\langle V_{carrier} \rangle(s)} \neq \frac{V_s}{V_{carrier,peak}}$$

Being a non-linear component, the hysteresis comparator cannot be straightforwardly converted to a linear model, although methods (such as describing function analysis) do exist. An indirect, argumentative method is used instead to find a suitable small-signal model for the hysteresis comparator, when used in the considered application.

Assuming that a fixed carrier signal is present, offsetting this by an infinitesimal amount will cause the comparator output to go either high or low, since one of the hysteresis limits is no longer reached. It thus appears that the hysteresis comparator small-signal gain is *infinite* while a carrier signal is present (at least at DC) This argumentation is illustrated in Figure 3.

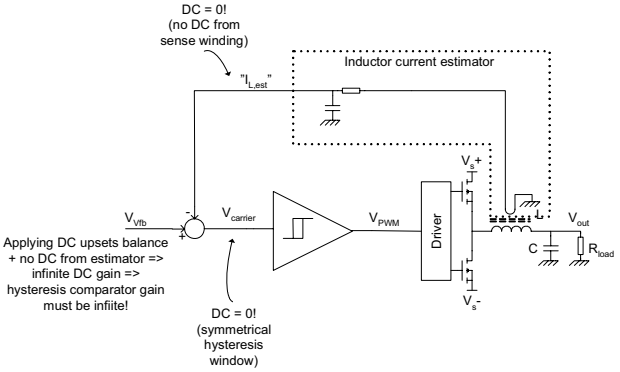

Figure 3 Derivation of hysteresis comparator/power stage small signal model.

Using this knowledge, the BPCM controlled power stage and output filter can be modelled as shown in Figure 4.

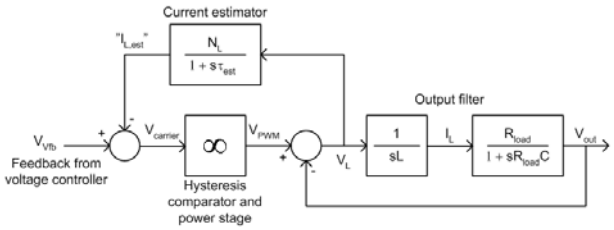

Figure 4 Derived small-signal model of comparator, power stage and output filter with hysteretic BPCM control.

The model shown has the following parameters:

Inductor voltage sense winding ratio	N_L
Current estimator time constant	τ_{est}
Output filter inductance	L
Output filter capacitance	C
Load resistance	R_{load}

The closed-loop transfer function of the BPCM loop can, for any hysteresis comparator small-signal transfer function, *G(s)*, be written as:

$$G_{BPCM,cl}(s) = \frac{V_{out}(s)}{V_{Vfb}(s)}$$

$$G_{BPCM,cl}(s) = \frac{G(s)\cdot(1+s\tau_{est})\cdot R_{load}}{\left(1+s\frac{L}{R_{load}}+s^2CL\right)(1+s\tau_{est})\cdot R_{load} + G(s)\cdot N_L \cdot sL\cdot(1+sR_{load}C)}$$

Assuming that $G(s)=\infty$ (as argued), this reduces to:

$$G_{BPCM,cl}(s) \cong \frac{(1+s\tau_{est})\cdot R_{load}}{N_L \cdot sL\cdot(1+sR_{load}C)}$$

A number of useful observations can be made:

- $G_{BPCM,cl}(s)$ only has real poles/zeros (i.e. output filter Q is a non-issue)
- $G_{BPCM,cl}(s)$ can be turned into an integrator by choosing $\tau_{est}=R_{load}C_{out}$ (pole-zero cancellation)
- Switching frequency has no impact on closed-loop behaviour of the BPCM loop.

By choosing components so that $\tau_{est}=R_{load}C_{out}$, voltage loop compensation can be minimal, relying only on gain blocks.
By providing enough raw gain from the closed BPCM loop, these gain blocks can implemented as resistive attenuators, with associated low cost and simplicity, as shown in Figure 5.
Well-behaved closed loop amplifier response is also ensured in this way, since the system effectively only contains a single pole. The impact of load (R_{load}) variation on closed-loop behaviour is assumed to be manageable.
Figure 6 shows the small-signal model of the proposed

controller, while shows a low-cost implementation.

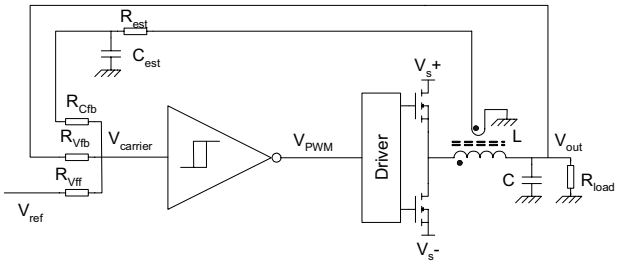

Figure 5 Low-cost implementation of proposed controller

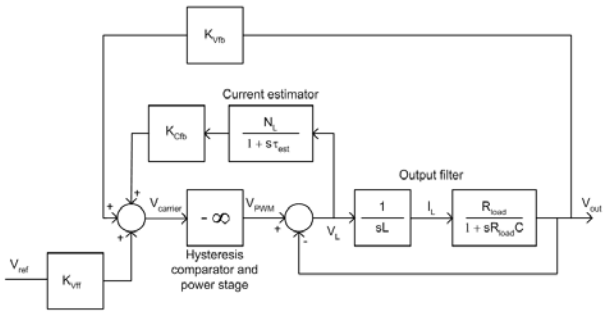

Figure 6 Small-signal model of proposed controller

The BPCM loop transfer function is affected by the introduction of K_{Cfb}:

$$G_{BPCMcl}(s) \cong \frac{(1+s\tau_{est})\cdot R_{load}}{K_{Cfb}\cdot N_L \cdot sL\cdot(1+sR_{load}C)}$$

This model forms the basis for all further linear modelling work presented in this paper.

Assuming that source impedance, amplifier output impedance and current estimator output impedances are small, the following expressions for controller gains K_{Cfb} K_{Vfb}, K_{Vff} will apply:

$$K_{Cfb} = \frac{R_{Vfb} \parallel R_{Vff}}{(R_{Vfb} \parallel R_{Vff}) + R_{Cfb}}$$

$$K_{Vfb} = \frac{R_{Cfb} \parallel R_{Vff}}{(R_{Cfb} \parallel R_{Vff}) + R_{Vfb}}$$

$$K_{Vfb} = \frac{R_{Vfb} \parallel R_{Cfb}}{(R_{Vfb} \parallel R_{Cfb}) + R_{Vff}}$$

The amplifier closed-loop gain A_V, assuming the above as well as sufficient open-loop voltage-loop gain, is simply:

$$A_V \cong -\frac{R_{Vfb}}{R_{Vff}}$$

As would also apply for a standard inverting opamp-based amplifier. The current estimator time constant τ_{est} is finally, assuming that $R_{Cfb} >> R_{est}$, given by

$$\tau_{est} = R_{est} C_{est}$$

This model forms the basis for all further linear modelling work presented in this paper.

Selection of gains and estimator time constant is constrained by non-linear phenomena in addition to standard bandwidth/gain requirements, as will be discussed in the following.

IV. PROTOTYPE DESIGN

The effectiveness of the proposed control scheme is best illustrated in a design with a relatively low (by class-D amplifier standards) output filter cutoff frequency. The output filter cutoff frequency is set at 35.3kHz, which coincides with convenient filter component values. These values, along with other relevant design parameters, are listed in the following table.

Output filter inductance	L	20.25µH
Inductor voltage sense winding ratio	N_L	2:9 ≈ 0.22
Output filter capacitance	C	1µF
Nominal load resistance	$R_{load,nom}$	4.7Ω
Closed-loop gain	A_v	20dB
Supply voltage	+/-V_s	+/-40V
Idle switching frequency	$f_{sw,idle}$	300kHz

The nominal load resistance is set to allow convenient selection of current estimator components in order to achieve $\tau_{est}=R_{load}C_{out}$, leading to $R_{est}=100\Omega$, $C_{est}=47nF$. These values also ensure a relatively low output impedance of the estimator, as required with this realization.

The modelled BPCM closed-loop transfer function with these values is shown in Figure 7. The closed loop clearly behaves as an integrator at a load resistance slightly above 4Ω, as it should. It can also be noted that, provided that enough voltage loop open-loop gain is provided, voltage loop stability margins will be excellent at all loads within the considered range.

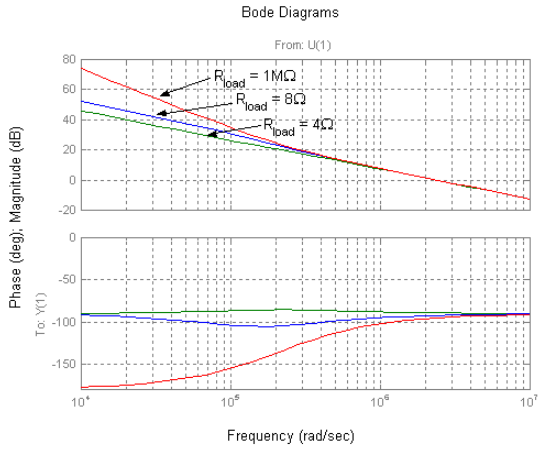

Figure 7 BPCM loop closed-loop frequency responses for varying load resistances

Determining the actual voltage loop gain constants is a matter that requires attention to *carrier distortion* [1], [2]. The idea presented in [1] is that the modulation process achieves maximum linearity when the produced carrier is perfectly triangular. In this system, the carrier composed of components from the inner (BPCM) control loop and the outer (voltage) control loop.

Balancing of current estimator and voltage loop feedback gains, while achieving the desired switching frequency can be straightforwardly achieved through iterative simulation work.

For the considered design example, relevant simulation waveforms are shown in Figure 8.

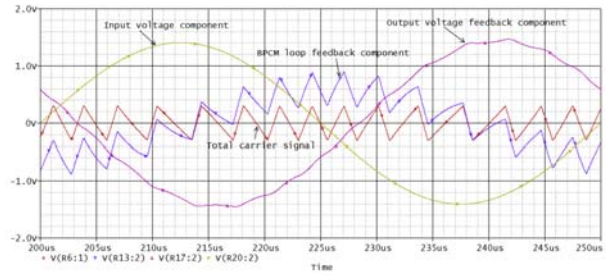

Figure 8 Simulated, optimized carrier signal and its subcomponents in prototype amplifier design. Amplifier producing 20kHz sinewave output at M=0.75 with 8Ω load.

The complete set of component values found for the design is shown in the following table:

R_{est}	100Ω
C_{est}	47nF
R_{cfb}	2kΩ
R_{Vfb}	10kΩ
R_{Vff}	1kΩ

The resulting open-loop and closed-loop frequency characteristics are shown in Figure 9 and Figure 10. With the controller gains as forced by carrier linearity considerations, closed-loop –3dB cutoff is around 20kHz with 4Ω load, while the worst-case phase margin is close to 45° when the amplifier is unloaded. Amplifier bandwidth is thus adequate for audio, while stability is unconditional.

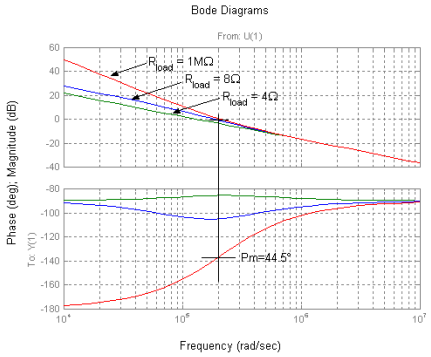

Figure 9 Open-loop Bode plots for prototype amplifier design, showing worst-case phase margin

The step response of the closed-loop linear model with all its assumptions is shown in Figure 11. This can be directly

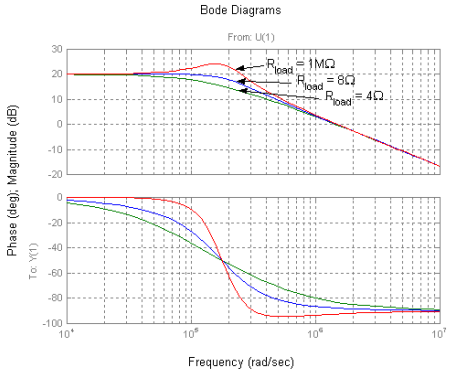

Figure 10 Closed-loop Bode plots of prototype amplifier design

compared to the simulated step responses where the simulation model corresponds to Figure 5. Results are in good agreement indicating that the small-signal model used has sufficient accuracy for dynamic behaviour prediction. An entirely different matter is BPCM loop error suppression capability (i.e. as found by calculating the loop sensitivity function), which realistically cannot be infinite, which logically results from having an infinite gain inside the loop. BPCM loop oscillation can likewise not be explained using the presented model.

Linear modelling of the hysteresis comparator is in other words *not* an outdebated (if at all debated?) topic.

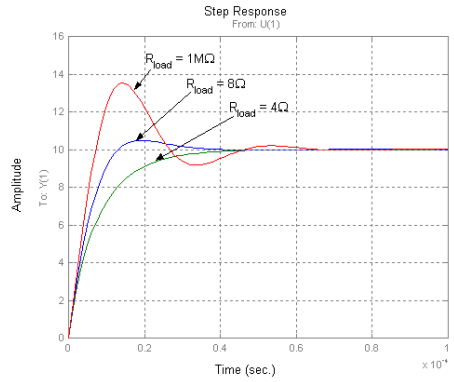

Figure 11 Step-responses of prototype amplifier design as predicted by linear modeling

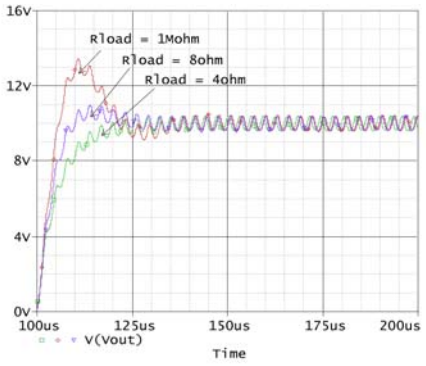

Figure 12 Simulated step responses of prototype amplifier design

VI. ACHIEVED PRACTICAL RESULTS

A prototype amplifier has been constructed on a 2-layer PCB with single-side component placement, as shown in Figure 13. The relatively large number of components is due to the fact that the PCB has provisions for the implementation of more complex control schemes.

Figure 13 The prototype amplifier in its test bench

To conclude the investigation of dynamic response modeling, the measured step response corresponding to the modeled and simulated step responses is shown in Figure 14. This result is in good agreement with the already predicted responses. The easiest comparison to make is between no-load overshoot, which is measured to about 32%, simulated to about 29%, and modeled to about 35%. The deviation between simulated and measured switching frequency (and thus, ripple voltage) is due to the absence of comparator/power stage delays in the simulation model.

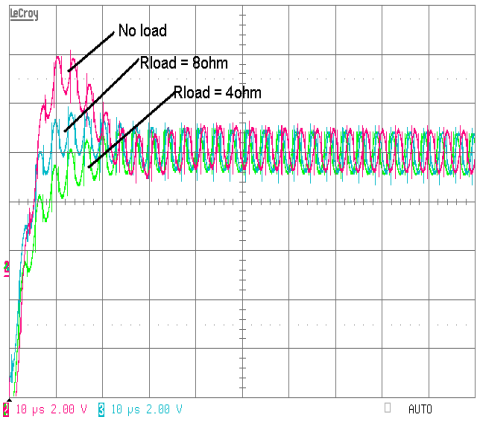

Figure 14 Measured step response of prototype – 2V/div and 10µs/div

Distortion performance is indicated by the THD+N measurements shown in Figure 15 and Figure 16. Although not state-of-the-art [1], [3], the results are very reasonable, and THD+N stays around 0.02% within the area of operation. Signal frequencies are chosen to allow direct comparison with other published results, e.g. [1]. Worth noting is the fact that THD+N is not worse at 6.67kHz than at 1kHz which is the case for certain other control schemes. Additionally, low distortion is achieved with modest voltage loop gain, as indicated by the relatively low closed-loop bandwidth.

Clipping with 4Ω load occurs at lower power than otherwise expected, this is due to current limiting in the power supplies used.

Since power stage/comparator chain implementation generally contributes significantly to the overall THD+N performance of a class-D amplifier, details are given in the following table as a reference:

Total delay (approx.)	160ns
Dead time (approx.)	50ns
Driver	HIP2100 (Intersil)
MOSFETs	FDD3672 (Fairchild)
Gate resistance	Minimal (only parasitics)

The results presented have in other words been achieved using a standard, average-performance power stage/comparator chain (relative to integrated power stages, such as those provided by TI). THD+N performance of the prototype shows significant sensitivity to variation in negative power stage supply

decoupling, indicating that higher performance is possible by circuitry improvements.

The relatively long dead time used results in little power stage shoot-through and low idle losses. The case temperature of the TO-252 packaged MOSFETs settles at around 30°C above ambient during idle operation, corresponding to total idle losses in the MOSFETs of around 1W.

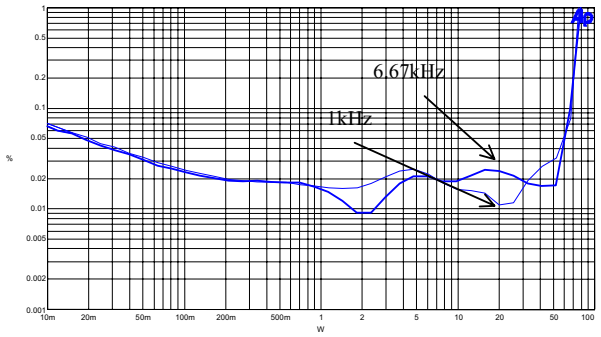

Figure 15 THD+N ratio of prototype amplifier with 8Ω load at 1kHz and 6.67kHz, 80kHz measurement bandwidth

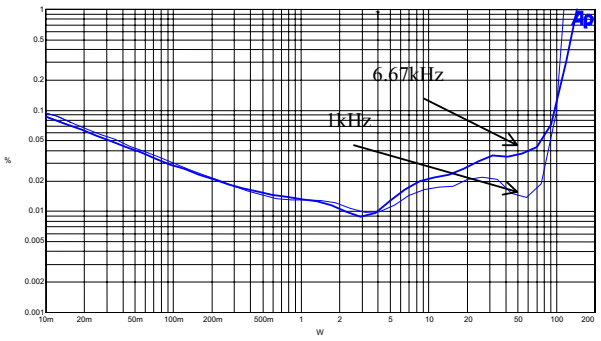

Figure 16 THD+N ratio of prototype amplifier with 4Ω load at 1kHz and 6.67kHz, 80kHz measurement bandwidth

The measured frequency response of the amplifier is shown in Figure 17, and a zoom of the predicted response is shown in Figure 18 for easy comparison. For 4Ω and 8Ω, results are in good agreement with the linear model whereas peaking is less than expected with open load. Output capacitor losses and/or modelling inaccuracies are probable causes. Output capacitor losses will especially cause increased removal of energy from the output filter LC circuit, thereby decreasing its Q.

The deviation of mid-band gain of about –0.7dB is partially due to generator output impedance and input buffering (accounts for –0.26dB), the remaining –0.44dB are almost within limits set by 1% resistor tolerance (+/-0.35dB).

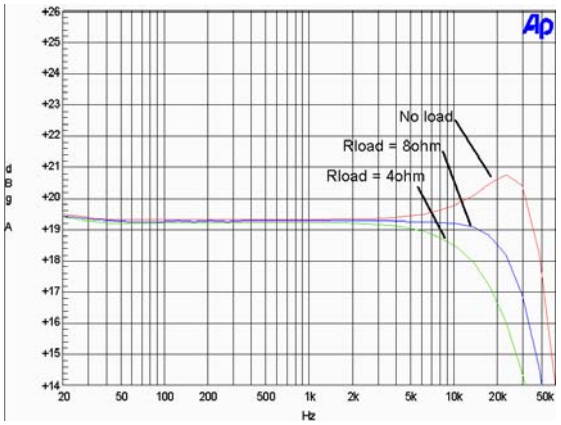

Figure 17 Frequency response of prototype amplifier at V_{out}=10V_{peak} into 4Ω, 8Ω and open load, >500kHz measurement bandwidth.

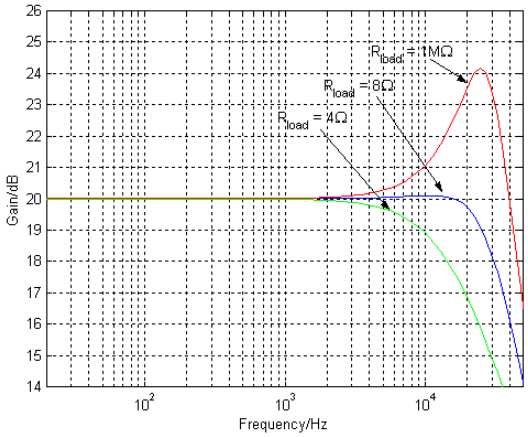

Figure 18 Predicted frequency response of prototype amplifier (zoom of Figure 10, top)

VII. CONCLUSION

This paper has presented a small-signal model of a self-oscillating control loop, which allows accurate prediction of the dynamic behaviour of the complete amplifier. This tool can be used as a supplement to simulation, especially for troubleshooting during the control system design process. The small-signal model also allows overall design rules to be firmly established.

Used in combination with prior art, the small-signal model based method has been demonstrated capability to lead to well functioning, predictable amplifier designs.

The proposed BPCM based control scheme places itself in the low-cost, high-performance category among amongst analogue, self-oscillating control systems for buck-type converters.

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