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Fabrication of 3D Air-core MEMS Inductors

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MEMS inductors are used for e.g. RF MEMS and microelectronics. A new application is for power electronics in switched mode power supplies (SMPS). High-performing MEMS power inductors, which can be integrated with integrated circuits (IC), are required for future power supply on chip (PwrSoC) [1].

Examples of PwrSoC applications are power adaptors for LED illumination or the “Internet of Things”.

We report an air-core MEMS inductor. Our process is scalable and universal for making inductors with versatile geometries e.g. spiral, solenoid, toroid, and advanced inductors that are impossible to make by wire-winding technology. As all process temperatures are below 200 °C, the inductors can be integrated into CMOS wafers by MEMS post processing.

Our inductor design is optimized for very high frequency (30MHz to 300MHz) SMPS with 12V, 1A output. The inductor is a suspended air-core toroid secured to the substrate by fixtures (Fig 1b). Our design has near-ideal performance because the electromagnetic flux is confined in the toroid, leading to minimal electromagnetic interference (EMI) cross-talk with active CMOS devices in case of wafer level integration or packaging. Furthermore, the air-core design also minimizes high-frequency eddy-current losses in the Si substrate that would otherwise be significantly larger than the conduction loss (10 times more at 100MHz) [2]. We analytically modelled and simulated our toroidal inductor with COMSOL for an optimal inductor design. The models account for high frequency skin and proximity effects, and we studied the influences on resistance and inductance as a function of frequency between DC and 300 MHz.

The fabrication process includes 3 main stages, 12 steps and 4 lithography masks (Fig 2). Firstly, we etch through the Si wafer using AZ MIR 701 resist/atomic layer deposition (ALD) Al2O3 masks (stage 1, step 1-4) to create Si through-silicon vias (TSVs) by deep reactive ion etching (DRIE). The aspect ratio is 11. After removing etching masks, Al2O3 and SiO2 are then deposited on the wafer using ALD and PECVD, respectively. Stage 2 consists of 3 copper (Cu) plating steps: (5) plating top layer and to “close” the TSVs, (6) bottom-up plating to fill the TSVs and (7) plating 30µm bottom layer. E-beam evaporated 10nm Cr/100nm Au is used as seed layers. The windings are patterned by Cu wet-etching using a resist mask, and the Si-core inductor is obtained (8). In stage 3, we selectively remove the Si core by DRIE, as illustrated in step 9-12. In step 10, because of the 30 µm height variation caused by the Cu winding structures, photoresist is spray-coated and patterned to etch SiO2 and Al2O3. The Si is exposed and we remove the silicon core in the last 2 steps. The air-core inductor is held in place by Si fixtures (Fig 1b), that are fabricated by combining DRIE, ALD, and utilizing aspect ratio dependent etching effect (ARDE) [3].

A selected result from our analytical model is shown in Fig. 3a. Efficiency (η) is presented as a function of toroidal geometry (turns, outer radius) with a η = 90 % plane. This was used as a design guideline for selecting inductor geometry so that η > 90 %. We have successfully fabricated Si-core inductors (Fig 3b), and are now working towards finalizing the air-core inductor (Fig 1a), that are fabricated by combining DRIE, ALD, and utilizing aspect ratio dependent etching effect (ARDE) [3].

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We have initiated innovation activities for our inductors. A multidisciplinary team of master students investigates the markets and establishes a business plan. http://memsinductors.com.

References:

Figure 1. 3D Illustrations of air-core toroidal inductor chip (a), and Si fixture after removing Si core (b).

Figure 2. Cross-sectional illustration for fabrication process flow.

Figure 3. 3D plot of calculated inductor efficiency as a function of number of turns and outer radius (a). Si-core toroidal inductor chip in the probe station (b). (c) 30-µm-diameter, 350-µm-tall Cu-filled TSV after step 6, (d) wet-etched Cu top windings, (e) optimized semi-anisotropic profile (d>b) for Si core removal.