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Capacitor-Free, Low Drop-Out Linear Regulator in a 180 nm CMOS for Hearing Aids

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Abstract—This paper presents a capacitor-free low dropout (LDO) linear regulator based on a new dual loop topology. The regulator utilizes the feedback loops to satisfy the challenges for hearing aid devices, which include fast transient performance and small voltage spikes under rapid load-current changes. The proposed design works without the need of an off-chip discrete capacitor connected at the output and operates with 0-100 pF capacitive load. The design has been implemented in a 0.18 µm CMOS process. The proposed regulator has a low component count and is suitable for system-on-chip integration. It regulates the output voltage at 0.9 V from 1.0 V - 1.4 V supply. A current step load from 250-500 µA with an edge time (rise and fall time) of 1 ns results at ∆V_{out} of 64 mV with a settling time of 3 µs when C_L = 0. The power supply rejection ratio (PSRR) at 1 kHz is 63 dB.

I. INTRODUCTION

Linear voltage regulators are important components in today’s integrated circuits. For on chip power management, where multiple supply voltages are used, low drop-out (LDO) voltage regulator play an important role. Improving power management will help to extend the battery life and could increase the use of portable devices. As the industry is pushing towards complete system-on-chip (SoC) design solutions, including improving power management, LDO voltage regulators play an important role. Linear regulators have some advantages over switch mode power supplies as they provide lower output noise, less electromagnetic emission, high PSRR and are easy to integrate on-chip within a small area while maintaining an accurate output voltage.

In portable devices such as hearing aids there is a strict requirement on area consumption. The number of discrete components must be minimized, as the electronics must fit in the ear canal. Implementing a capacitor free LDO regulator will help to reduce the overall size by eliminating the large output capacitor and increase the reliability of the system. On the other hand, for a voltage regulator without a on-chip capacitor (usually referred as capacitor-free or capacitor-less) the designer has to design a stable circuit without a large capacitor that sets the dominate pole. In this application the estimated capacitance of load circuitry is between 0-100 pF. The absence of an output capacitor gives rise to issues in the transient response, ∆V_{out} (undershoot and overshoot) that will be larger and there will be an increase of the recovery time (settling time). Moreover a large output capacitor ensures stability as it will set the dominant pole and acts as a supply for the frequency components of the current load, I_L, outside the bandwidth of the regulator.

Removing the external capacitor requires to overcome the transient response and stability issues mentioned. There have been a number of capacitor-free topologies suggested in earlier articles. This previous research mainly focus on improving the transient performance [1] - [2]. One approach is to use active feedback and slew-rate enhancement circuit [3]. Another approach is a LDO structure with a three-stage amplifier and damping-factor-control frequency compensation [1] or utilizing voltage spike detection [4]. All those approaches and others result in a rather complex design, large area and normally high quiescent current.

In this paper, Section II presents the circuit description and introduces the two regulation loops and its design details. Section III discusses the simulation results. Discussion of performance comparison with former work are presented in Section IV. Finally, the conclusions of this paper are given.
II. CIRCUIT DESCRIPTION

The new design proposed in this work is based on a principle similar to [5], employing two control loops and a PMOS pass transistor configured as a common source (CS) amplifier. Refer to Fig. 1 for the circuit diagram of the proposed regulator. The design specifications target the following parameters. The regulator is supplied by nominal voltage of 1.2 V and outputs a voltage of 900 mV. The load current, $I_L$, is 250-500 µA which is stepped with a 1 ns rise and fall time. $\Delta V_{out}$ is 64 mV during current step load and the circuit consumes 10.3 µA quiescent current. The capacitance $C_L$ represents the load of up to 100 pF.

The fast loop consists of a differential amplifier stage, driving the common source (CS) amplifier, which includes the pass transistor (Q1) and 2 resistors. The PMOS transistors in the differential stage (Q2 and Q3) are controlled by the slow loop containing the operational amplifier. The proposed design does not contain any large passive devices and has a low count of transistors. The simplicity allows for easy and area efficient implementation, while demonstrating good performance. Moreover, reaching stability is simpler compared to other designs due to the low number of poles and zeros. The following sections describe the two control loops in detail. The circuit was biased from two different current sources for debugging proposes. The full circuit diagram can be found in Fig. 2.

A. Principle of Operation of the Fast Loop

The fast loop directly regulates the gate of the pass transistor. Its purpose is to suppress the spikes in the output voltage, $V_{out}$, which is due to a step in the load. The overall performance of the regulator is impacted by the amplitude of the voltage spikes and the recovery time. By assuming the fast loop constitutes an underdamped system, the gain bandwidth product (GBWP) of the open loop gain will be inversely proportional to the settling time $T_s$. Therefore we will design the fast loop to have large GBWP. There is a trade-off between the circuit quiescent current in the fast loop stage, to the GBWP of the loop. As can be seen in Fig. 1, this loop starts at the gate of Q4 and ends at the drain of Q1.

The open loop transfer function, $A_{OL}(s)$, is described in (1). In order to analyze the loop, the equation was divided into two parts, CS stage ($H_1(s)$) described in (2) and differential stage ($H_2(s)$) described in (5). From the analysis of the transfer function it can be realized that the parasitic capacitance and resistance of the pass transistor (Q1) dominate the poles $\omega_{p1}$ (3) and $\omega_{p2}$ (6). The gate-source capacitance is $C_{gs1}$ and $C_{gd1}$ is the gate-drain capacitance of Q1. The output resistance is represented by $r_{ds1}$ and $g_{m1}$ is the transconductance of Q1. The analysis was done with a load capacitance $C_L$ to understand its impact on the system, therefore in the zero load case $C_L = C_{gd1}$. In this work the maximum value of the load capacitance was 100 pF as expected in hearing aids.

\[
A_{OL}(s) = H_1(s)H_2(s) \quad (1)
\]
\[
H_1(s) = -g_{m1}R_t \frac{1}{(1 + \frac{1}{\omega_{p1}^2})(1 + \frac{1}{\omega_{p2}^2})} \quad (2)
\]
\[
\omega_{p1} = \frac{1}{C_tC_t + g_{m1}R_tC_{gd1}} \quad (3)
\]
\[
\omega_{p2} = \frac{1}{R_t(R_sC_{gs1} + C_{gd1}) + C_tC_t} \quad (4)
\]

Where: $R_t = \frac{r_{ds1}}{R_1 + R_2}$; $C_T = C_L + C_{gd1}$

The differential stage and common source stage set the gain of the fast loop. By maximizing $g_{m1}$ we can achieve higher gain for the CS stage. The poles and zeros were selected in the design of the fast loop to achieve high GBWP. The
The fast loop gain of the fast loop is defined by

$$ H_2(s) = \frac{-g_{m5} R_{diff}}{(1 + \frac{s}{\omega_p})(1 + \frac{s}{\omega_m})} $$

(5)

$$ \omega_p \approx \frac{1}{R_{diff} C_{gd1}} $$

(6)

$$ \omega_m \approx \frac{g_{m5}}{C_g} $$

(7)

$$ \omega_z \approx \frac{2g_{m5}}{C_g} $$

(8)

Where: $C_g = C_{gs1} + C_{gs2}$; $R_{diff} = r_{ds1} \parallel r_{ds5}$

The resistors $R_1$ and $R_2$ bias Q1. Moreover they are used to set the gate voltage of Q4 and keep the transistor in saturation. The quiescent current in the differential stage should be minimized. By choosing W/L as mentioned for Q1 the output capacitor of this stage will mainly be the pass transistor gate capacitance, $C_{q1}$, which will be larger than the capacitors at the other nodes. The differential stage gain that is set mainly by the output resistance of transistors Q3 and Q5. Another aspect is the power supply rejection ratio which can be increased by using larger length for transistors Q2-Q5. The loop gain of the fast loop is defined by

$$ L(s) \approx A_{OL}(s) \frac{R_2}{R_1 + R_2} $$

(9)

When current step loads are applied, ringing can occur on the output of the regulator due to low phase margin of the loop response. Therefore it is desirable to keep the phase margin of $L(s)$ above 75 degrees at maximum expected load capacitance.

### B. Principle of Operation of the Slow Loop

The role of the slow loop is to control the gate voltage of transistors Q2 and Q3 and thereby stabilize the DC level at $V_{out}$. A two stage operational amplifier (OpAmp) with Miller capacitor has been utilized for this function. The slow loop is designed to consume a low quiescent current and will have low power consumption. Transistors Q11 to Q18 and the miller compensation capacitor constitute the OpAmp as can be seen in Fig. 2. The slow loop starts at the gate of Q12, then through the OpAmp, proceed from the gate to the drain of Q3 and then from the gate to the drain of Q1. In order not to degrade the frequency response of the fast loop, this OpAmp has a unity gain frequency approximately two decades below that of the fast loop, Therefore the dominant pole of the OpAmp was placed at a low frequency, at 100 Hz

![Figure 3. Simulated open loop frequency response of the slow and fast loops, without extracted parasitics. $C_L = 0$ and $I_L = 0$](image)

The design compromises of the slow and fast loop discussed above lead to the device dimensions, quiescent currents and transconductance presented in Table I. The total quiescent current is 10.3 µA. A value of 4 pF was chosen for $C_C$.

### III. Simulation Results

The proposed capacitor-free LDO linear voltage regulator has been implemented in a 180 nm CMOS process. The presented results are based on the post layout simulation. The bias current in the CS stage was 1.0 µA, current of 8.256 µA was distributed at the differential stage and 1.05 µA to the
OpAmp, giving a total quiescent current consumption of 10.3 µA.

The layout is presented in Fig. 4 and has been designed with measures 174 µm x 68 µm. Common centroid matching and dummy devices have been used. The pass transistor Q1, differential stage, resistors and the compensating capacitor can be seen in the layout figure.

Post-layout simulation has been performed. Fig. 3 shows the open loop frequency response of the slow and fast loops at $C_L = 0$ and zero load current. The slow loop unity gain frequency is approximately two decades below that of the fast loop as we required. The PSRR is shown in Fig. 6, its dc values with and without the load capacitor is 63 dB at 1 kHz, under the typical case.

The transient response of the capacitor-free LDO voltage regulator for a current step of 0 - 250 µA with a rise and fall time of 1 ns is shown in Fig. 5. The simulation was preformed with and without $C_L$. $\Delta V_{out}$ without a load capacitance is 64 mV, while for $C_L = 100$ pF the spikes reach 56 mV. It should be noted that a smaller current step or lager edge time will decrease the spikes. Fig. 7 presents the transient analysis with different voltage supplies. The design was sent for fabrication, we expect to present result at the conference.

IV. PERFORMANCE COMPARISON

The presented theory and results of the proposed LDO linear voltage regulator show that external capacitor can be replaced by the design proposed. This design is suitable to supply low current to internal circuitry like needed in hearing aids. The design is simple to implement, with small area, which makes it ideal for a system-on chip. Simulations show good performance when compared with known capacitor-free topologies. For the purpose of comparison with other regulators we define a figure of merit (FOM) from [2]. This is used for standardized comparison in capacitor-free regulators as in the table. For this parameter, the smaller the FOM, the better the transient response of the regulator.

$$FOM = K \frac{\Delta V_{OUT,pp} I_Q}{\Delta I_{out}}$$  \hspace{1cm} (10)

Where, $\Delta V_{OUT,pp}$ is the sum of the undershoot and overshoot and $K$ is the edge time ratio which is defined by

$$K = \frac{\Delta t \text{ used in the measurement}}{\text{smallest } \Delta t \text{ among the designs for comparison}}$$
The unit of the FOM is volt as noted in Table II. The $K$ factor depends on the designs considered for comparison, because the edge time of our work is the smallest, it $K$ factor is equal to 1.

The performance comparison between the proposed design and some selected published LDOs is shown in Table II. The FOM of the proposed design when comparing to similar designs is the second lowest. Our design has the smallest chip area, with the second lowest quiescent current of 10.3 µA while the load capacitance can be as large as 100 pF. Not only does the proposed regulator consume low power, but it provides a low dropout voltage and fast settling time.

Table III presents the results for the typical and worst case corners. Although the spikes and settling time has increased from the typical case the results are still quite similar.

### V. Conclusion

We have demonstrated a new capacitor-free low-dropout linear regulator for hearing aids in 180-nm CMOS technology. The structure, post-layout simulation and performance comparing have been provided. The proposed regulator has proven a good transient performance. The internal compensating capacitor is as small as 4 pF and the chip total area is 0.012 mm². The LDO voltage regulator can operate with supply voltage between 1.0 - 1.4 V while having a quiescent current of 10.3 µA and small $\Delta V_{\text{out}}$ due to the two regulation loops. The achieved specification of the proposed LDO makes it suitable for hearing aids and similar SoC applications.

### References


