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Evaluation of 600V Superjunction Devices in Single Phase PFC Applications under CCM Operation

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***Abstract*— This paper presents a power density/efficiency evaluation in single phase power factor correction (PFC) applications operating in continuous conduction mode (CCM). The comparison is based on semiconductor dynamic characterization and a mathematical model for prediction of the conducted electromagnetic interference (EMI). The dynamic characterization is based on a low inductive double pulse tester (DPT). The measured switching energy is used in order to evaluate the devices performance in a conventional PFC. This data is used together with the mathematical model for prediction of the conducted electromagnetic interference. The method allows comparing different devices and evaluating the performance as a function of the PFC power density and efficiency.**

Keywords— Power factor correction, continuous conduction mode, EMI prediction.

I. INTRODUCTION

Power factor correction circuits are widely use in industrial and household applications to fulfill the power factor and harmonic standards. These types of circuits are traditionally used in continuous conduction mode configuration [1], [2]. This operation mode presents lower component current stress than critical or boundary conduction modes (BCM) which are actually preferred for low power levels because of their control simplicity [3]. The main disadvantage of continuous conduction mode PFC is the rectifier reverse recovery loss [2] which limits the converter operating switching frequency and consequently its power density. However, the latest achievements in semiconductor technology including the adoption of wide bandgap semiconductor materials makes it possible to eliminate this reverse recovery problem [4], [5], [6] allowing higher converter operating switching frequencies. Moreover, the recently introduced wide bandgap gallium nitride (GaN) transistors with a higher electrical field strength and electron mobility than Si based switches [7] makes it possible to reduce the device die size decreasing the parasitic capacitances. This reduction of die size enables higher operating switching frequencies to further increase the converter power density while reducing the cost without deteriorating the efficiency. This paper presents a design oriented methodology for power factor corrector implementation based on double pulse tester (DPT) dynamic characterization and a conducted EMI prediction model. In this way it is possible to evaluate the switch-diode pair energy loss across half a line cycle. At the same time, the inductor size can be estimated based on the maximum energy storage requirement $E = 1 / 2 \cdot I_{peak}^2 \cdot L$. The input filter requirement can be evaluated based on the calculated quasi peak and average noise from the calculated harmonics across half the line cycle. This work performs an evaluation of state of the art 600V superjunction silicon (Si) devices in combination with silicon carbide rectifiers (SiC). The devices performance is evaluated for various input inductor values and switching frequencies.

II. DYNAMIC CHARACTERIZATION

The evaluation of the semiconductors switching behavior can be performed based on analytical models [8], [9], [10]. However, this is an arduous work that is technology dependent. In this work, the devices dynamic characterization is performed in a low inductive DPT. This circuit is the basic configuration used to evaluate the dynamic performance of different semiconductor technologies under clamped inductive load operation. The basic schematic is presented in Fig.1. The typical operating waveforms of the DPT are shown in Fig. 1. At the time interval t_0 the MOSFET is turned and the inductor current increases up to the desired current level. Once the desired level is reached, the MOSFET is turned off at t_1. At t_2 and t_3 the MOSFET is turned on and turned off again and the associated energy loss is measured for the desired current level.

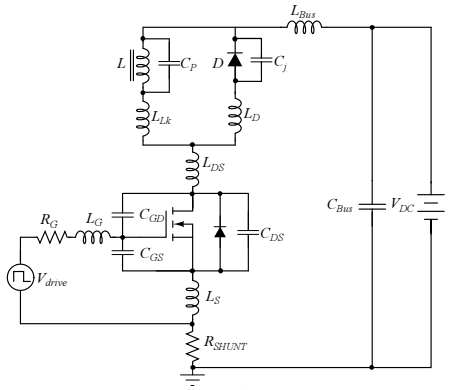

Fig. 1 DPT schematic with parasitic components

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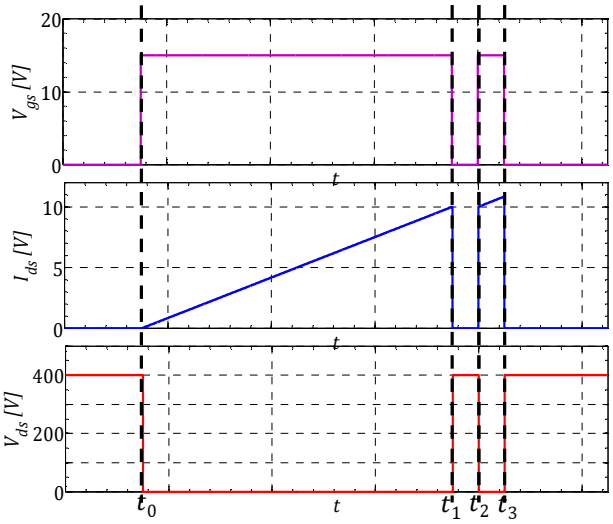

Fig. 2 DPT typical operating wavefoms

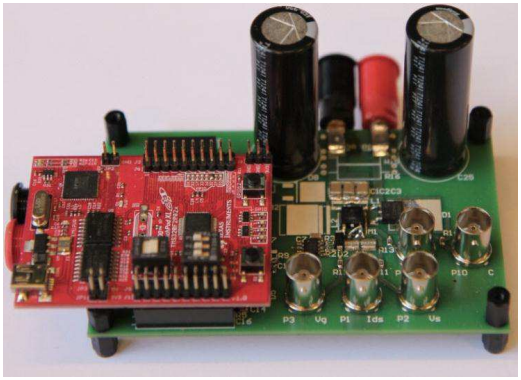

Fig. 3 DPT Experimental prototype

In order to perform the semiconductors characterization, a DPT prototype has been designed paying special attention to minimize the parasitic inductances and capacitances in the switching loop [11], [12] [13]. The main switch current is measured using a flat current shunt structure as presented in [14] to minimize the parasitic inductance inserted in the loop and maximize the current measurement bandwidth. The implemented prototype (Fig. 3) is based on the a DSP evaluation board Piccolo Launchpad XL and can accommodate both Dpak and PQFN packages for the main switch and the diode.

III. CONDUCTED EMI PREDICTION MODEL

A conducted EMI estimation is necessary to evaluate the input filter requirement of the converter. The level of attenuation required according to the standards will determine the input filter corner frequency and consequently its volume. The analyzed topology in this work, is the conventional boost derived PFC rectifier shown in Fig. 4. The input inductor current waveforms can be derived by looking at the volt/second balance across the component as shown in Fig. 5. The MOSFET M on time D_1 can be calculated according to [15] as presented in (1) for continuous conduction mode and (2) for discontinuous conduction mode, where $M = V_o/V_{in}$ and $K = 2L_{IN} \cdot T_S/R_L$. The transition from discontinuous to continuous conduction mode the two modes can be estimated by evaluating the input current condition $I_{in} \leq D_{cont}T_S V_{IN}/2L_{IN}$. The diode D conduction time can be calculated as $D_2 = 1 - D_{cont}$ for continuous and $D_2 = K \cdot M/D_{dis.}$ for discontinuous conduction modes. If the input current is sampled at different points in time, is possible to calculate the inductor current using piecewise linear definition as shown in Fig. 6. Then, by using (3) the inductor current frequency harmonic content at each time interval is calculated.

$$D_{cont} = (M-1)/M \cdot \quad (1)$$

$$D_{discont} = \sqrt{K \cdot M \cdot (M-1)} \cdot \quad (2)$$

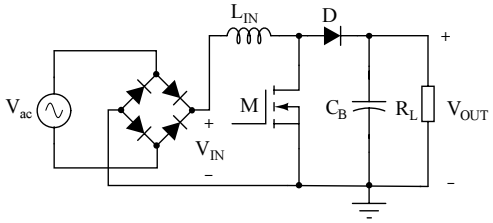

Fig. 4 Conventional single phase PFC circuit

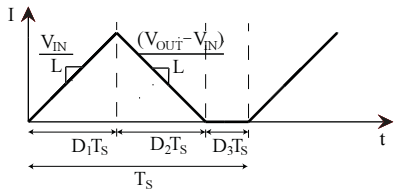

Fig. 5 Inductor current waveform

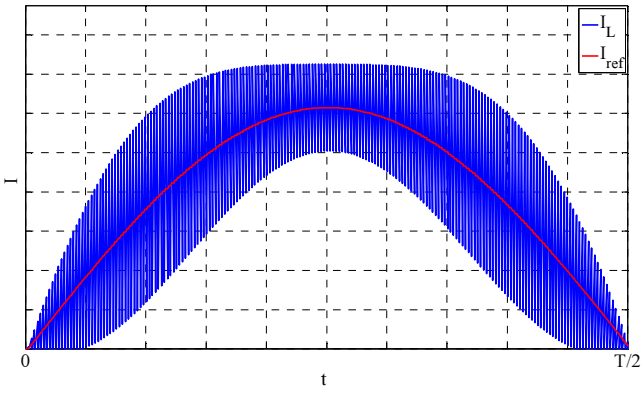

Fig. 6 Calculated inductor current following the current reference through half line cyle

$$I_L(t) = a_0/2 + \sum_{n=1}^{N}(a_n \cos(2\pi nt/T_s) + b_n \sin(2\pi nt/T_s)) \quad (3)$$

Once the inductor current harmonics have been calculated it is possible to estimate the EMI receiver quasi-peak and average readings. As shown in Fig. , the inductor current harmonics are first multiplied by the LISN network differential gain which can by approximated by (4) where the equivalent impedance Z_C is calculated as $Z_C = Z_B \| (1/sC_3 + R_3)$ where $Z_B = (sL_1 + 1/sC_1 + R_1) \| (1/sC_2 + R_2) + sL_2$.

$$G_{LISN}(f) = \frac{V_A}{I_L} = \frac{Z_c}{R_3 + 1/sC_3} \cdot R_3 \quad (4)$$

Then, the EMI receiver sweeps the frequency range of interest by using a near Gaussian filter which transfer function can be approximated as (5) as presented in [3]. The envelope detector will detect the harmonic peak value through half line cycle from which the average and the quasi peak values can be extracted. However, the quasi-peak value is based on a quasi-peak detector which transfer function is nonlinear. The output of this quasi-peak detector can be calculated as shown in [3]. By using a dissection method like a dichotomy algorithm or method of division in halves applied over the charge balance on the capacitor (6) were the discharge resistance is known to be 160 times the charge resistance value.

$$G_{IF}(f, f_{IF}) = e^{-(f-f_{IF})^2/c^2} \text{where } c = 4.5e^3/\sqrt{ln2} \quad (5)$$

$$\sum_1^n \int_{a_n}^{b_n} \frac{V_{envelope} - V_{quasi}}{1} = \int_0^{T_s/2} \frac{V_{quasi}}{160} - \sum_1^n \int_{a_n}^{b_n} \frac{V_{quasi}}{160} \quad (6)$$

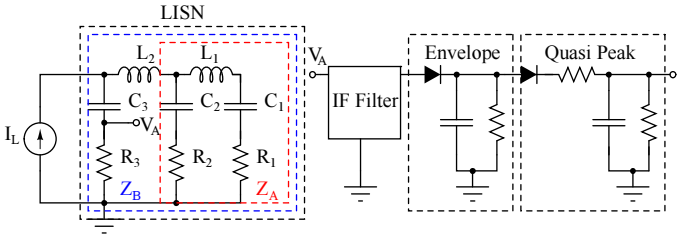

Fig. 7 LISN network, envelope and quasi peak detector schematics

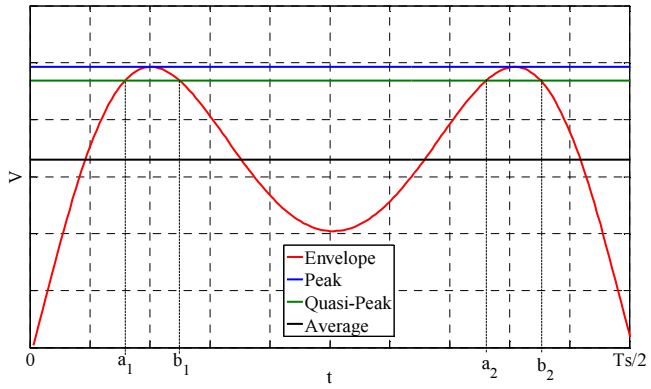

Fig. 8 Envelope, peak, quasi peak and average signals for the inductor current first harmonic across half line cycle

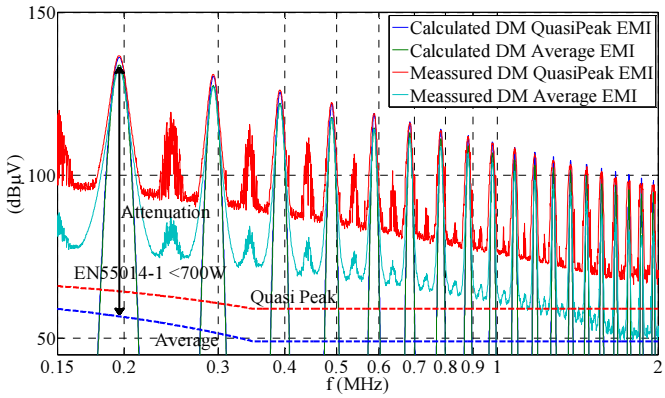

Fig. 9 Calculated vs. measured quasi peak and average conducted EMI

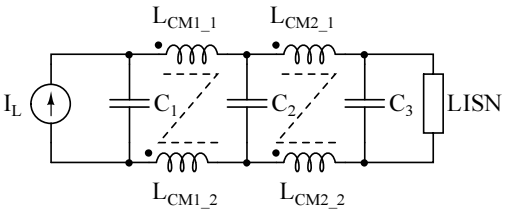

Fig. 10 Two stage pi filter loaded with the lisn network

The quasi peak value is calculated finding the charge balance condition in the capacitor by integrating the capacitor charge and discharge currents across half line cycle. In the same way, the peak value will be the envelope absolute maximum value, and the average is obtained by averaging the envelope through half line cycle as shown in Fig. 8. Fig. 9 presents the calculated and the measured quasi peak and average values for a CCM PFC operating at $V_{IN} = 230V_{rms}$ and $V_{OUT} = 386V$ with an inductance value $L_{IN} = 1150\,\mu H$ and an output power level $P_{OUT} = 200W$. After obtaining the calculated converter EMI quasi peak and average values, is possible to calculate the necessary amount of attenuation required to fulfill the limits established by the standard. In this work, a two stage π filter (Fig. 10) is selected for the evaluation. This type of filter with attenuation equal to 100dB/dec will set the necessary filter corner frequency for the necessary amount of attenuation required.

IV. Evaluation

In this section, two state of the art superjunction devices with three SiC rectifiers are evaluated for a PFC application under the following conditions: $V_{IN} = 230V_{rms}$, $V_{OUT} = 400V$ and $P_{OUT} = 200W$ The selected superjunction devices have $130m\Omega$ and $230m\Omega$ on resistances, and the SiC diodes have a continuous forward current capability of 6, 8 and 10 A. As it can be observed in Fig. 11, the diode selection does not modify the MOSFET turn off loss. At zero current level, the amount of measured energy will be equal to the stored energy in the MOSFET output capacitance that will be dissipated at the MOSFET turn on. In this case, the device with the larger die presents a higher turn off loss. According to Fig. 12 both MOSFET present a very similar turn on loss. As it can be seen, at the turn on the energy stored in the diode output capacitance will create a current level independent turn on loss.

By performing an interpolation on the obtained characterization data, the semiconductor switching losses can be obtained through half line cycle and averaged to calculate the total semiconductor switching loss. In the same way, the semiconductor conduction loss is calculated (7) by using the manufacturer MOSFET on resistance (R_{DS}) and by extracting the diode threshold voltage (V_T) and dynamic resistance (R_D) from the characteristic I-V curve.

$$P_{cond.} = I_{M,rms}^2 \cdot R_{DS} + I_{D,avg} \cdot V_T + I_{D,rms}^2 \cdot R_D \quad (1)$$

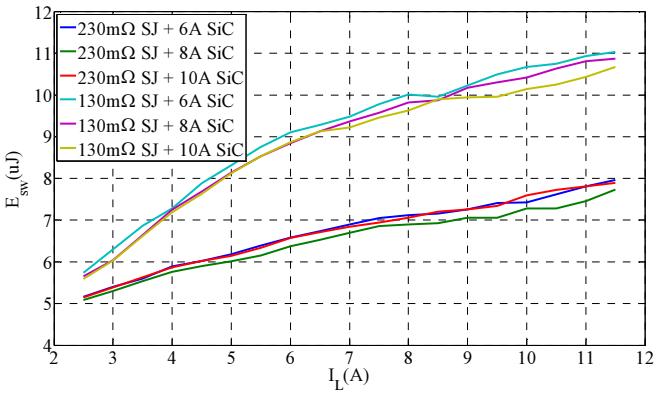

Fig. 11 DPT turn off energy loss as a function of the inductor current level

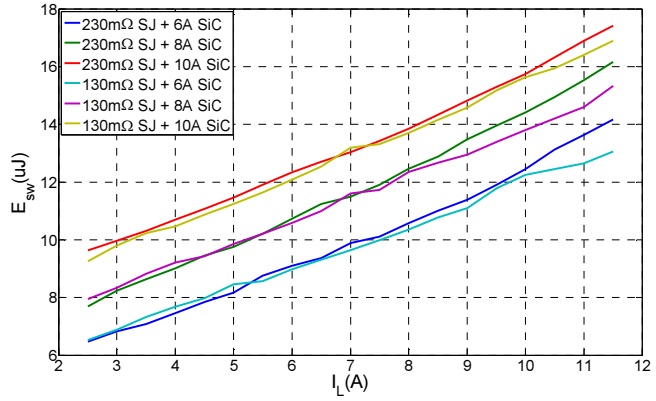

Fig. 12 DPT turn on energy loss as a function of the inductor current level

The total semiconductor efficiency loss can be plotted then as a function of the converter switching frequency for different input inductor values as shown in Fig. 13. At low frequency values, the semiconductor loss will be increased because the semiconductor current stress will be increased by increasing the inductor ripple current and the time the converter operates in discontinuous conduction mode (DCM) through the line cycle. As the converter switching frequency increases, the semiconductor switching loss is increased but the conduction loss is decreased creating a semiconductor minimum loss for each inductor value. The inductor current stress ($I_{L,rms}^2$) can be plotted to obtain a figure of the inductor winding losses

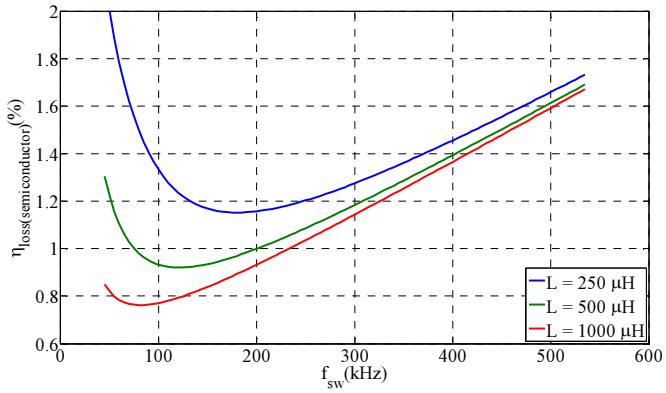

Fig. 13 Semiconductor total efficiency loss (130 mΩ superjunction MOSFET + 6A SiC diode) as a function of the converter switching frequency

Fig.14 shows how the stress diminishes as a function of the converter frequency and inductance value. However, this is not a valid measure for comparison because the inductor winding resistance will change as a function of the inductance value and the energy storage requirement. Fig. 15 shows the maximum calculated inductor energy storage requirement ($I_{L,peak\_max}^2/2L$). As it can be observed, as in the current stress case, the value decreases as the switching frequency increases reaching an absolute minimum as the inductor ripple approaches zero.

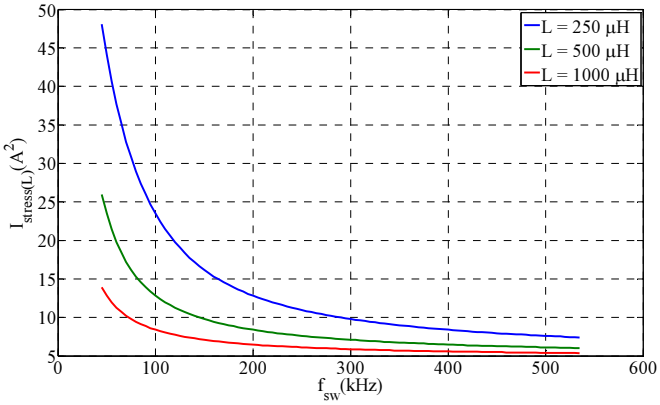

Fig. 14 Inductor current stress as a function of the converter switching frequency

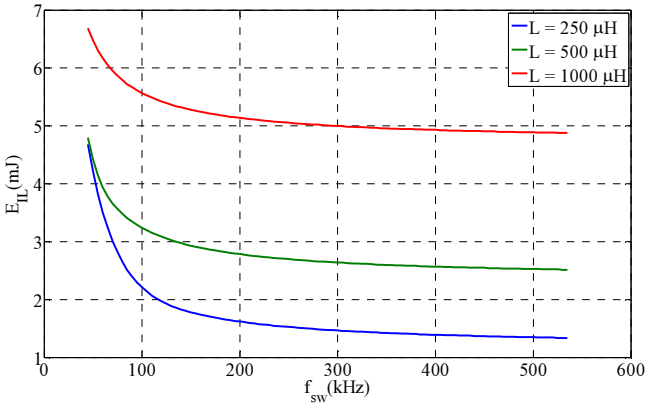

Fig. 15 Inductor energy storage requirement as a function of the converter switching frequency

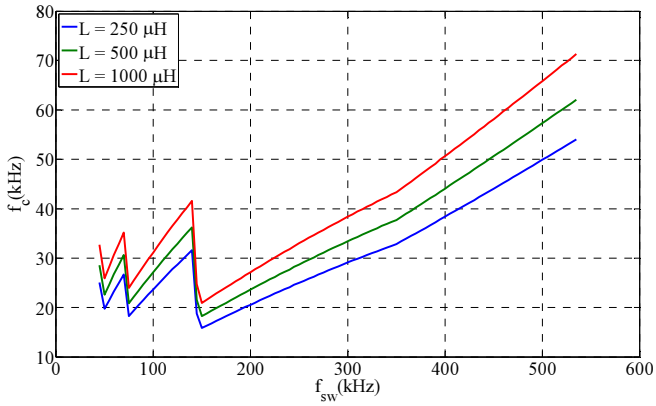

Fig. 16 Input filter corner frequency as a function of the converter swiching frequency

Fig. 16 presents the input filter corner frequency requirement. Obviously, the volume of this filter is affected by the input inductor ripple, and consequently its energy storage requirement. Therefore the only viable way of increasing the converter power density, is by increasing the converter switching frequency. The filter corner frequency presents local minimum values at 50, 75 and 150 kHz due to the 150 kHz limit of the standard. When the converter operating switching frequency approaches these frequencies, the third, second and first harmonic of the converter operating switching frequency hit the measurement frequency range increasing the input filter attenuation requirement. This is the reason why a common practice in industry is to design converters operating just below these frequency levels to limit the switching loss while minimizing the input filter volume.

Fig. 17, 18 and 19 show the calculated semiconductor loss for the $130m\Omega$ MOSFET with the $10A$ diode and the $230m\Omega$ MOSFET with the 6 and $10A$ diodes respectively. As it can be observed, the smaller superjunction device performs better than the $130m\Omega$ version at switching frequencies higher than 150 kHz due to the smaller turn off loss. It is only at very low frequency and for the large inductance value, when the lower channel resistance of the $130m\Omega$ device offers a small advantage over the smaller device. The predominant conduction losses correspond to the diode. This can be observed by the fact that even considering the increased turn on loss, when a larger diode is used, the efficiency loss is increased for the whole frequency range evaluated.

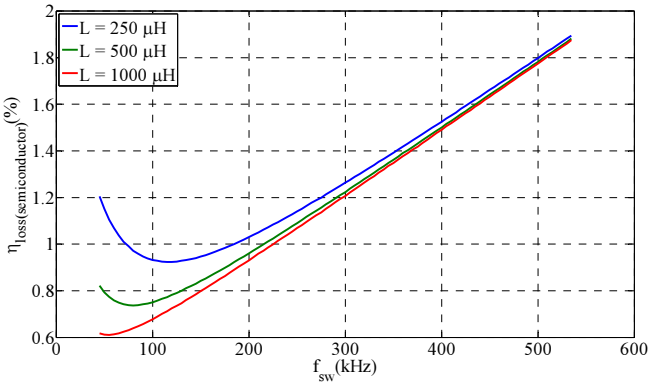

Fig. 17 Semiconductor total efficiency loss (130 mΩ superjunction MOSFET + 10A SiC diode) as a function of the converter switching frequency

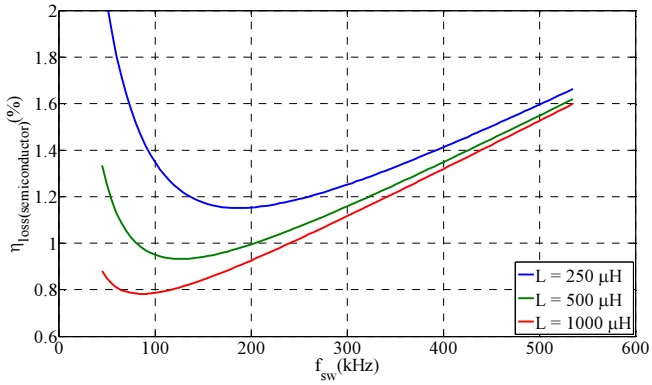

Fig. 18 Semiconductor total efficiency loss (230 mΩ superjunction MOSFET + 6A SiC diode) as a function of the converter switching frequency

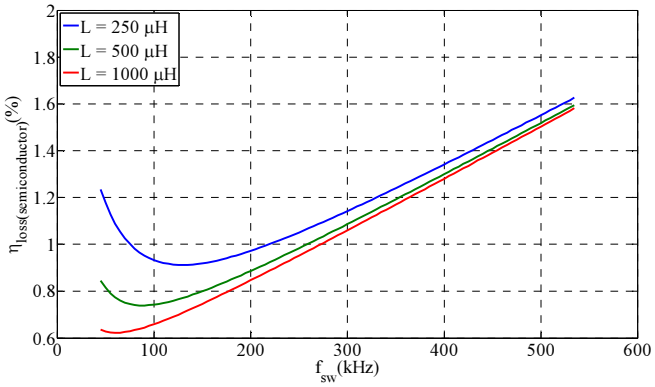

Fig. 19 Semiconductor total efficiency loss (230 mΩ superjunction MOSFET + 10A SiC diode) as a function of the converter switching frequency

If we compare the different evaluated devices, the larger MOSFET and diode with the large inductor at $45\ kHz$ would give the best performance in terms of efficiency with only 0.62% efficiency loss due to semiconductor conduction and switching loss. The necessary input filter corner frequency is situated at $32.6\ kHz$, and the calculated inductor energy storage requirement is $6.7\ mJ$. If the switching frequency is now increased up to the next local maxima in the input filter corner frequency ($@\ 70\ kHz$), the best performance is obtained from the $230m\Omega$ device with the $10A$ diode and maximum inductance value. With only 0.63% total semiconductor loss this would be the correct choice even when the efficiency is the maximum priority. This solution would increase the filter corner frequency 8% and reduce the input inductor energy storage requirement by 12% without having a negative impact on the semiconductor loss. If the $500\ \mu H$ inductor is selected at this operating frequency, the input inductor size could be reduced down to 46.7% the volume of the initial design $@\ 45\ kHz$. This selection would increase semiconductor losses by 20% and lower the input filter corner frequency by 6% respect to the initial design. If we move now towards the next maxima in the input filter corner frequency, the obvious selection is the mid-size inductor with the small MOSFET and the large diode. At this operating frequency, the input inductor energy requirement is reduced 55.5% and the input filter corner frequency is increased by 11% while the semiconductor loss is increased 27% respect to the original design. This power loss increase could be alarming, but the semiconductor power loss is still only 0.79% of the converter output power. If the design needs to be optimized for power density, the small inductor size could be chosen at a switching frequency of $350\ kHz$. This selection would give the same requirement in input filter corner frequency than the initial design with an inductor energy storage requirement reduction of 79% with a total semiconductor loss 2 times larger respect to the initial design.

V. CONCLUSIONS

This paper presents a comprehensive design/evaluation procedure for single phase PFC applications. The method is based on a mathematical model for prediction of the conducted differential mode EMI and a semiconductor dynamic characterization setup. The proposed method evaluates the input filter corner frequency requirement and the input inductor

energy storage requirement to compare different solutions in terms of power density. The obtained characterization data allows predicting the semiconductor switching loss in a precise way making possible to compare the different evaluated devices under different operating conditions. A case design is presented where two superjunction devices are analyzed together with three SiC diodes to evaluate several possible solutions regarding converter efficiency and power density. As it can be observed, limiting the converter switching frequency in the way that only the second or the third harmonic need to be attenuated is not the best solution in terms of power density. As observed in Fig. 20, as the semiconductors switching speeds increase is possible to operate beyond the 150 kHz filter corner frequency maxima achieving a high volume reduction of the input inductor size without penalizing in the input filter size and with a small penalty in terms of semiconductor loss. Solution 1 operates at $45\,kHz$ while solution 2 operates at $350\,kHz$ with more than 5 times input inductor size reduction and with a MOSFET die size 56% times the size employed in the first solution. With the same filter corner frequency the semiconductor power loss penalty is only 3.15 W for a converter output power of 500W (0.63% efficiency loss respect to solution 1). With the new introduced GaN switches this tendency will be accentuated making possible to increase the converter power densities with very small efficiency penalties.

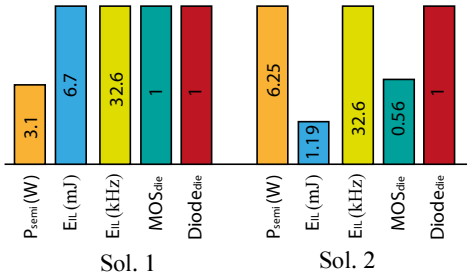

Fig. 20 Two opposite solutions in terms of efficiency vs power density. Sol. 1: 130mΩ MOSFET with the 10Adiode @ 45 kHz and Sol. 2: 230mΩ MOSFET with the 10Adiode @ 350 kHz

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