Wideband polarization splitter and rotator with large fabrication tolerance and simple fabrication process

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Silicon-on-insulator (SOI) microphotonic devices are very attractive thanks to their complementary metal oxide semiconductor (CMOS)-compatible fabrication technology, their high refractive index contrast, and compact size\(^1\). Those advantages make SOI microphotonic devices promising candidates for all-optical signal processing subsystems. However, the high refractive index contrast also introduces large polarization dependency, which becomes one of the major challenges for their practical use. In particular, if the device is to be used in a subsystem deployed over an optical fiber link, the polarization state of the optical signal at its input may change randomly over time, making standard SOI microphotonic devices no longer compatible with optical processing functionalities.

To realize polarization independence, polarization diversity (Pol-D) circuits based on polarization splitter and rotator (PSR) technologies are typically used\(^2\–4\). In this scheme, the input light contributions along the two orthogonal polarizations axes are first split by a polarization splitter\(^5\). After that, one of the two polarizations is rotated by \(90^\circ\) by a polarization rotator\(^6\). Thus, in the rest of the circuit, only one polarization needs to be processed. Many approaches have been proposed and demonstrated to realize PSRs. However, they all require a rather complex fabrication process\(^6\–11\). To simplify the fabrication process, asymmetrical directional coupler (DC)-based PSRs have been recently proposed and demonstrated\(^12\–14\). One of the main practical issues with many PSR designs is their limited fabrication tolerance, which makes them impractical for high-yield production. The best reported fabrication tolerance of \(\sim 14\) nm for a DC-based PSR was recently obtained using a tapered DC design\(^15\).

In this Letter we propose and demonstrate a PSR built on the SOI platform. In this device, an adiabatically tapered waveguide first converts the TM\(_0\) to the TE\(_1\) mode, while also preserving the TE\(_0\) mode. A \(2 \times 2\) multimode interference (MMI) coupler, which is well-known for its large fabrication tolerance\(^16\) and has been utilized for wide bandwidth polarization splitting/combining\(^17\), is introduced afterward to effectively couple the TE\(_0\) and TE\(_1\) modes at the end of the TM\(_0\)–TE\(_1\) mode converter to two distinct TE\(_0\) outputs. Simulation results show a large fabrication tolerance of \(63\) nm thanks to the use of the MMI. A low insertion loss better than \(2.5\) dB, with minimum insertion loss of only \(0.6\) dB and polarization crosstalk lower than \(-12\) dB over a wide bandwidth of \(100\) nm, is demonstrated experimentally, together with a large fabrication tolerance better than \(50\) nm.

The principle of the proposed PSR is schematically depicted in Fig. 1(a). Light is first injected into a tapered waveguide and then split into two beams by a Y-splitter. Before being injected into the \(2 \times 2\) MMI, an extra phase difference of \(\pi/2\) is introduced between the two beams. In case of TE\(_0\) input, the mode will be preserved during the adiabatic taper and split into two TE\(_0\) beams with the same phase. Thus, at the MMI input, the two beams will have a \(\pi/2\) phase difference. By properly designing the MMI, light will output from arm 1 on the TE\(_0\) mode with little crosstalk in arm 2 [Fig. 1(b)]. On the other hand, in case of TM\(_0\) input, the light is converted to the TE\(_1\) mode during the adiabatic tapering\(^14\) and split into two TE\(_0\) beams with \(\pi\) phase difference. Thus, at the MMI input, the two beams will have a \(-\pi/2\) phase difference, and light will consequently output from arm 2 on the TE\(_0\) mode.
polarization conversion, a material with a bandwidth of 98 nm are expected. Thus, an overall size deviation tolerance of 15 dB. Finally, for the MMI, in a Rayleigh range, a length tolerance can be estimated as \( \Delta L_{\text{MMI}} = \pi n_r w_{\text{eff}}/\lambda_0 \) [16], where \( \lambda_0 \) is defined as the input Gaussian beam waist, \( n_r \) is the material refractive index, and \( \lambda_0 \) is the operating wavelength. The corresponding width tolerance and operation bandwidth can be calculated as \( \Delta w_{\text{MMI}} = w_{\text{MMI}} = L_{\text{MMI}}/2 \) and \( \Delta L_{\text{MMI}} = \lambda_0 L_{\text{MMI}}/L_{\text{MMI}} \), respectively [16]. With \( \lambda_0 = 700 \) nm, \( n_r = 3.476 \), and \( \lambda_0 = 1550 \) nm, a length tolerance \( \Delta L_{\text{MMI}} \) of 860 nm, a width tolerance \( \Delta w_{\text{MMI}} \) of 63 nm, and a bandwidth \( \Delta \lambda_0 \) of 98 nm are expected. Thus, an overall size deviation tolerance of \( \Delta w_{\text{device}} = 63 \) nm is expected for the whole device with a bandwidth of 98 nm.

The device was fabricated on a SOI wafer (top silicon thickness 250 nm, buried silicon dioxide 3 \( \mu \)m) by a single step of E-beam lithography (JEOL JBX-9300FS) and inductively coupled plasma reactive ion etching (STS Advanced Silicon Etcher). Figure 4(a) shows the fabricated device with design parameters as introduced previously. The total length of the device, including the 140 \( \mu \)m long adiabatic taper-based TM\(_0\)–TE\(_1\) mode converter, is 190 \( \mu \)m. Note that the smallest feature size of the device is the inner corner of the Y-splitter, enabling our scheme to be fabricated with other methods [19]. Figure 4(b)
conversion efficiencies are obtained over a better than 50 nm device size deviation, in good agreement with the simulations.

In conclusion, we have proposed and demonstrated a PSR built on the SOI platform, which is fabricated by simple processing. A low insertion loss better than 2.5 dB with a minimum insertion loss of 0.6 dB and polarization crosstalk lower than −12 dB over a wide bandwidth of 100 nm are demonstrated together with a large fabrication tolerance better than 50 nm.

References


Fig. 4. (Color online) (a) Scanning electron microscope (SEM) picture of the fabricated device. (b) Measured coupling efficiency to the two output ports for TE0 and TM0 inputs. (c) Measured TM0–TE0 conversion efficiency for different device size deviations.

shows the measurement results. Details on the measurement setup and calibration procedure can be found in [12]. A low insertion loss (from inputs on either the TM0 or TE0 mode to output arm 1 or 2 on the TE0 mode, normalized to a straight waveguide) better than 2.5 dB with a minimum insertion loss of 0.6 dB and polarization crosstalk lower than −12 dB are obtained over a wide bandwidth of 100 nm. To improve the insertion loss, more efficient Y splitters with lower insertion loss should be used [20]. In addition, the polarization crosstalk can be improved by increasing the width of the 2 × 2 MMI so that the two output waveguides are separated sufficiently to avoid evanescent coupling between them. To further investigate the fabrication tolerance of the device, six devices with device size deviations from −20 nm to 30 nm were fabricated and characterized, as shown in Fig. 4(c). One can find that similar high