Bootstrapped Low-Voltage Analog Switches

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ABSTRACT

Novel low-voltage constant-impedance analog switch circuits are proposed. The switch element is a single MOSFET, and constant-impedance operation is obtained using simple circuits to adjust the gate and bulk voltages relative to the switched signal. Low-voltage (1-volt) operation is made feasible by employing a feedback loop. The gate oxide will not be subject to voltages exceeding the supply voltage difference.

Realistic switches have been simulated with HSPICE. The simulations show that the switch circuits operate very well, even when the supply voltage approaches the technology’s threshold voltage.

1. INTRODUCTION

Technology constraints and battery-powered operation require that low-voltage analog circuits be designed. Whereas low-voltage operation is associated with many advantages for digital circuits, it generally complicates the design of analog circuits. When the supply voltage is lowered, not only does it become increasingly difficult to maintain the same (high) level of SNDR performance, but even the functionality of the circuit may be hard to preserve.

High-performance analog circuits are usually implemented as discrete-time circuits, often as switched-capacitor (SC) circuits. The design of analog switches which conduct reliably in the rail-to-rail range is the main difficulty in the design of low-voltage SC circuits. Switched-opamp and other dedicated low-voltage SC circuit techniques that avoid the need for rail-to-rail switching have been proposed [1, 2]. Although such techniques are useful and commercially utilized, it should be understood that they represent a tradeoff with respect to speed, power consumption, and design flexibility. This paper describes simple circuits that implement the rail-to-rail switching function, thereby facilitating the implementation of general low-voltage SC circuits.

2. MOSFET-BASED ANALOG SWITCHES

A MOSFET in itself can be used as an analog switch. The drain and source terminals are the two switch terminals, and the gate and bulk terminals are used to control the conductivity of the channel between the two switch terminals. Unfortunately, the MOSFET switch’s conductivity depends not on the absolute potential of the control terminals, but on their potentials relative to the conductive channel’s potential. Despite of this property, MOSFET switches are, for simplicity, often controlled by CMOS-logic clock signals having fixed potentials in the on and off states. The conductance of such a MOSFET switch is strongly signal-dependent (Fig. 1). An NMOS and a PMOS switch can be used in parallel to form a transmission-gate switch having a region where the conductance is approximately signal-independent. However, when the supply voltage is lower than the sum of the two transistors’ threshold voltages (absolute values), this region not only vanishes, but is replaced by a region in the middle of the supply-voltage range where the switch does not conduct reliably (Fig. 2).

Figure 1: On-state conductance of the single-MOSFET switch vs. the potential of the switched signal. The switches are controlled by CMOS-logic signals.

Figure 2: On-state conductance of the transmission-gate switch.

2.1. Low-Voltage Operation

If the supply voltage is low (say, 1.2 volts) and low-threshold-voltage MOSFETs (which are subject to leakage problems) are not available, rail-to-rail switching operation requires that control signals exceeding the supply-voltage range be generated. Clock-signal doublers have been proposed [3], but in a single-well technology they can be used only for MOSFETs of one type; hence

\footnote{Occasionally, the bulk terminal is called the back-gate terminal. For single-well technologies, the bulk may be the substrate, in which case it cannot be controlled separately for each MOSFET.}

\footnote{In a P-well technology, doubled clock signals can be generated only for NMOS switches. The problem is related to the forward-biasing of PN diodes.}
the switch conductance will be strongly signal-dependent. Another disadvantage is that the gate oxide will be subject to voltages of up to twice the supply-voltage difference, which may cause hot-electron effects and possibly permanent breakdown of the gate oxide.

**3. Bootstrapped Switch**

To obtain constant-conductance operation the gate-to-channel voltage should preferably be held constant during the on state. This can be obtained using a bootstrap technique (Fig. 3). The technique is discussed in Section 11.3 in [4], but a circuit realization is unfortunately not provided.

In the off state the bootstrap capacitor is charged to the supply-voltage difference, and ideally it will act as a floating battery in the on state. The NMOS switch will be non-conducting in the off state because sw3 connects the gate terminal to the low supply potential. In the on state, the switches sw1 and sw2 connect the fully-charged bootstrap capacitor between NO's gate and source terminals. Assuming that the stray capacitance loading of Cg is small, NO's overdrive will be nearly constant and the switch's on-state conductance will be approximately (neglecting the body effect and the stray load of Cs)

\[
g_{\text{switch}} = \mu C_{\text{ox}} \frac{W}{L} (V_{\text{dd}} - V_{\text{bs}} - V_{\text{TN}})
\]

Hence, if \(V_{\text{dd}} - V_{\text{bs}} > V_{\text{TN}}\), the bootstrapped switch will conduct in the entire supply-voltage range, and its conductance will be nearly signal-independent. Clearly, the difficulty lies in the implementation of the internal switches, particularly (but not exclusively) sw1 which must also be able to conduct in the rail-to-rail range.

**3.1. Simple Implementation**

Fig. 4 shows a simple implementation of the bootstrapped switch, where sw1 is implemented as a bootstrapped NMOS switch N1. The main difference between N1 and NO is that N1's source terminal is connected to \(V_{\text{bs}}\) in the off state, whereas the switch terminals, \(V_{\text{GS}}\) and \(V_{\text{GS,b}}\) are floating.

Switches sw3 and sw5 implement trivial switching functions, hence they are implemented as simple NMOS switches N3 and N5. At first sight, the design of sw4 may also appear to be trivial, but this is not the case. Unfortunately, sw4 cannot be implemented as a simple PMOS switch controlled by CMOS logic because it would leak during \(\Phi\) when the bootstrap capacitor provides a potential that exceeds \(V_{\text{dd}}\).

As illustrated, sw2 can be implemented as a simple PMOS switch as it will only be turned on when its gate voltage exceeds \(V_{\text{dd}}\). A more serious problem of the simple implementation is that the bootstrap capacitor will not have to drive the capacitive load constituted by the well in which P2 is implemented.

**3.2. Improved Implementation**

Fig. 5 shows an improved implementation of the switch. N1b is a simple NMOS switch which should be included if the supply voltage is only slightly higher than the PMOS threshold voltage. N1b prevents switch malfunction which may occur if clock feedthrough is allowed to reduce the channel potential of P2 to a level where it does not turn on. A separate clock terminal (as shown), but it may be better to connect it to \(2V_{\text{dd}}\) which can be obtained using the level shifter and a few extra transistors (traditional voltage doubler, not shown). The biased-PMOS implementation of sw2 is a considerable drawback for the circuit because it implies that NO cannot be implemented in a separate well (using a single-well technology); consequently, NO cannot be compensated for the body effect. Unfortunately, sw2 cannot be designed as an NMOS switch because that would require that large clock signals be generated.
P2 is turned off (and \(C_2\) is precharged) by the simple PMOS switch \(P_2b\). A similar switch has been developed and published in parallel to this work [6]. The only differences are that it lacks \(N_{lb}\) (which was unnecessary because the supply voltage was fairly high, 1.5 V) and that it fails to effectively protect the gate oxide of \(P_2\).

4. BODY EFFECT COMPENSATION

At very low supply voltages, and in other critical situations, the MOSFET switch's body effect may represent an intolerable non-linearity. As discussed above, it is the PMOS implementation of \(sw_2\) which prevents the bootstrapped switch (Fig. 3) from being compensated for the body effect when implemented in a single-well technology. An alternative bootstrap topology, which is not subject to this problem, is shown in Fig. 6.

4.1. Implementation

Fig. 7 shows an implementation of the switch. Here, \(sw_4\) is implemented as a PMOS \(P_4\), which operates as a rectifier for the alternating voltage provided by the charge pump. \(sw_3\) and \(sw_5\) are implemented as the simple PMOS switches \(P_3\) and \(P_5a\). The gate oxide of \(P_5a\) is protected by the cascode device PMOS \(P_5b\).

\(sw_1\) can, for example, be implemented as a PMOS device controlled by the same gate signal as \(P_0\) (not shown). \(sw_2\) is the only switch that may be difficult to design because it is exposed to the high potential from the charge pump. If the gate oxide is robust, \(sw_2\) can be implemented as an NMOS \(N_2\) with its gate terminal connected to "Node A" in the charge pump (not used in the shown implementation). Alternatively, if the gate oxide is sensitive and the supply voltage is fairly high\(^6\), \(sw_2\) may be designed as a transmission-gate-type switch\(^7\). The shown implementation of \(sw_1\) and \(sw_2\) illustrates an option for use in the most complicated situation where the gate oxide is fragile and the supply voltage is only slightly higher than the threshold voltage.

In this case, \(sw_2\) can be an NMOS \(N_2^*\) controlled by a gate signal which is \(V_{dd}\) in the off state and \(V_{in,a}+V_{dd}\) in the on state. This signal is generated by the bootstrapped switch shown in Fig. 5, where it is available at the source terminal of \(P_2\). If this switch (Fig. 5) is implemented anyway, \(sw_1\) can be implemented simply as a bootstrapped switch \(N_1^*\) controlled by the signal provided at the drain terminal of \(P_2\).

5. SIMULATION RESULTS

The switches shown in Figs. 5 and 7 have been simulated with HSPICE using BSIM3v3 transistor models for a 0.6μm technology, in which the threshold voltages were approximately 0.8 V and \(-0.85\) V for NMOS and PMOS transistors, respectively. All transistors were minimum-length, and \(N_0\) and \(P_0\) were respectively 10 μm and 30 μm wide. Except for \(N_1, N_1^*, \) and \(N_2^*\) which were 3 μm wide, all internal NMOS transistors were 1 μm wide, and all internal PMOS transistors were 3 μm wide. All capacitors were 1 pF, except \(C_2\) which was only 0.1 pF. The switches were generally simple to design, and very little optimization was performed for these simulations.

The generation of the non-overlapping clock signals is, however, a design aspect which can make a great difference in the performance\(^8\). The inverter shown in Figs. 5 and 7 was used to drive

\(^6\)This situation is quite likely to occur because this type of switch is generally useful for circuits that sample continuous-time voltage signals. These circuits need not necessarily be subject to a supply voltages that are so low that transmission-gate switches are useless.

\(^7\)Where the NMOS's gate is connected to \(V_{dd}\) and the PMOS is controlled by a doubled clock signal (\(V_{dd}\) and \(2V_{dd}\)).

\(^8\)The use of non-overlapping clock phases is necessary to prevent the 1 pF capacitors from being partially discharged in the transition between the two states \(\Phi\) and \(\bar{\Phi}\). This is advisable even for the charge pump.
an SR latch with delayed outputs, and all internal switches were

driven by the thereby generated non-overlapping clock phases \( \Phi \)
and \( \Psi \) (each clock phase was generated both as an inverted and as
an noninverted voltage signal).

The switch’s impedance is very well-behaved; the slight drop in
impedance is caused by the corresponding droop in the gate-to-
source voltage. The switch’s operation is reliable for supply volt-
ages as low as 0.9–1.0 V, for which the switch impedance is in the
order of 10 k\( \Omega \).

If large (low-impedance) switches are designed without in-
creasing \( C_b \) proportionally, the gate-to-source voltage may have
a considerable droop. The switch, however, can still be designed
such that the impedance will be nearly signal-independent. By
connecting a small NMOS device, say N6, in parallel with P0,
and by connecting N0’s gate terminal to the gate terminal of N1∗
in Fig. 7, a bootstrapped “transmission-gate” switch with an ap-
propriate “mix” of the impedance curves in Figs. 8 and 9 can be
designed.

6. CONCLUSION

Boostraping techniques are suitable for the linearization of MOS-
FET switches. It was demonstrated that bootstrapped switches
with a reliable linear switching operation can be implemented in
a standard CMOS technology, even when the supply voltage is as
low as 1 volt. Using these switches, low-voltage SC circuits can
be implemented in any usual topology.

The best performance is obtained if the switching MOSFET is
compensated for the body effect. This is feasible also in single-
well technologies, using a new bootstrap topology (Fig. 6) where
the bootstrap capacitor is connected directly to the gate of the
switching MOSFET. The switch circuits can be designed such
that the gate oxide is not subject to voltages exceeding the supply volt-
age difference. This requires the use of several transistors, but the
total chip area required is modest.

The switch’s remarkable linearity makes it a prime candidate
for use in circuits that sample continuous-time signals (low voltage
or not). A patent is pending on the described circuits.

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