A 3rd Order Low Power SI Sigma-Delta A/D Converter for Voice-Band Applications

Jørgensen, Ivan Harald Holger; Bogason, Gudmundur

Published in:
Proc. 1997 IEEE International Symposium on Circuits and Systems

Link to article, DOI:
10.1109/ISCAS.1997.608533

Publication date:
1997

Document Version
Publisher's PDF, also known as Version of record

Link back to DTU Orbit

Citation (APA):

General rights
Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain.
- You may freely distribute the URL identifying the publication in the public portal.

If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.
A 3RD ORDER LOW POWER SI \(\Sigma\Delta\)-A/D CONVERTER FOR VOICE-BAND APPLICATIONS

Ivan H. H. Jørgensen, Dept. of Information Technology, Technical University of Denmark, 2800 Lyngby, Denmark
Tel. (+45) 4525 3912, Fax. (+45) 4588 0117, E-mail: ihhj@it.dtu.dk

Gudmundur Bogason, OTICON A/S, Strandvejen 58, 2900 Hellerup, Denmark,
Tel. (+45) 3917 7308, Fax. (+45) 3927 7900, E-mail: gb@icu.oticon.dk

ABSTRACT
This paper presents a 3rd order switched current-\(\Sigma\Delta\)-modulator. The \(\Sigma\Delta\)-modulator operates at a sampling rate of \(f_s = 600kHz\) and the signal band is \(f_s = 5.5kHz\), i.e., an oversampling factor of \(R = 54.5\) is used. Multiple input signals are used to reduce the internal signal swings which results in reduced power consumption. The shaping of the noise from the 2nd and 3rd integrator is used to allow the noise power from these integrators to be increased to further save power. The total power consumption is approximately \(2.5mW\) with a supply voltage of \(V_{DD} = 3.3V\). The maximum SNR is approximately 74.5dB.

1. INTRODUCTION
Over the last years \(\Sigma\Delta\)-modulators have gained increasing popularity as they have the potential for high accuracy data conversion with modest analog requirements. The reason for the popularity originates in the fact that the quantization noise is moved from the signal band for the popularity originates in the fact that the quantization noise is moved from the signal band for the popularity originates in the fact that the quantization noise is moved from the signal band for the popularity originates in the fact that the quantization noise is moved from the signal band. In [4] the authors showed that the cut-off frequency \(f_c\) for the NTF(z) has a very strong influence on the MSA whereas the influence on the SNR is very weak. When the ratio between \(f_c\) and \(f_s\) decreases then the MSA increases and the signal-to-quantization-noise-ratio is approximately constant over a wide range of cut-off frequencies, \(f_c\). In \(\Sigma\Delta\)-A/D modulators it is desirable to get as much signal power into the modulator as long as the quantization noise is well below the analog noise floor as the overall SNR then increases.

If a signal is forced into the \(\Sigma\Delta\)-modulator one will observe that it becomes unstable if the amplitude of the signal is greater than a certain value called the maximum stable input amplitude MSA [2]. In [4] the authors showed that the cut-off frequency \(f_c\), for the NTF(z) has a very strong influence on the MSA whereas the influence on the SNR is very weak. The maximum SNR is approximately 74.5dB.

2. SYSTEM DESIGN
In figure 1 a block diagram of the 3rd order \(\Sigma\Delta\)-modulator used in this design is shown. The signals are shown as currents as the \(\Sigma\Delta\)-modulator is to be implemented using switched current (SI) techniques.

The quantizer in figure 1 can be modeled by replacing the comparator with a amplification factor, \(K_n\), and a white noise source, \(n_q\), that represents the quantization noise [2], [3]. It is a widespread misunderstanding to assume that the gain \(K_n\) equals one because if it was so then the modulator would not be invariant to scaling of \(K_n\). In fact, it is not necessary to assume anything about the gain \(K_n\) in order to design the modulator filter, i.e., determination of the coefficients \(b_1\), \(b_2\), and \(b_3\).

The \(\Sigma\Delta\)-modulator coefficients \(b_1\), \(b_2\), and \(b_3\), are determined by designing the NTF(z), [1] and [2], as a 3rd order highpass Butterworth filter.
the output. In this design this technique was used to lower
the internal signal swings and thereby the quiescent current
in INT2 and INT3 by a factor of 2 and 4 respectively. This
results in the same SNR but reduces the power consumption
by a factor of \( \frac{1.71}{2.25} = 0.75 \).

Because the noise from INT2 and INT3 is shaped, the
noise at the output of the modulator is dominated by the
noise from the input section, i.e., INT1, DAC1 and IN1. By
increasing the MSA we increase the signal power at the
input of the modulator which allows a noisier input sec-
tion for a given SNR. We utilize this to lower the power
consumption. A very high MSA will result in a reduction
of the SNR because the modulator begins to perform poor
coding of the input signal which results in increased quan-
tization noise at the output. As a compromise we chose
MSA = 0.691 which equals to \( f_n = 0.15fs \) for a NTF(z)
designed as a 3rd order Butterworth highpass filter [4]. For
\( f_n = 0.15fs \) the following coefficients are found (see figure
1):

<table>
<thead>
<tr>
<th>( a_1 )</th>
<th>( b_2 )</th>
<th>( a_2 )</th>
<th>( b_2 )</th>
<th>( b_3 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>5.66</td>
<td>13.6</td>
<td>64.0</td>
</tr>
</tbody>
</table>

and due to the
scaling
\( k_1 = 1 \), \( IC_2 = 17.4 \) and
\( k_3 = 64.0 \).

3. IMPLEMENTATION

The SI-integrator used in this design is shown in figure 2.
The SI-integrator is a cascode type but also a folded cas-
code type was considered. However, the folded cascode SI-
integrator introduced extra noise due to the extra current
sources needed and therefore this solution would consume
more power for a given SNR and thus it was rejected.

The integrator in figure 2 has a very low input impedance
as the transistors \( M_{2,1} \) and \( M_{2,2} \) act as current convey-
ors which reduce the input impedance (compared to the
input impedance of a single transistor) by a factor of
\( LG = \frac{1}{1 + \frac{g_{m2}}{g_{m2}+g_{m2}}} \) where \( g_{m2} \) and \( g_{m2} \) are the transconductance
and output admittance for the \( M_{2,1} \)’s. The input impedance
of this circuit is therefore in the order which can be
as low as \( \frac{1}{10} \) at low frequencies. This eases the interfacing
to the circuit, in fact, the input devices IN1 and IN2 in fig-
ure 1 are just resistors that convert the input voltage to a
current. This is indicated in figure 2.

The transfer function for the integrator is:

\[
\frac{i_{out}(z)}{i_{in}(z)} = K \frac{z^{-1}}{1-z^{-1}} \tag{1}
\]

It is important that the integrator has very little loss as
any loss results in a finite DC-gain which gives rise to an
increase in the quantization noise at low frequencies. The
loss in the SI-integrator is caused by finite output resistance
and the gate-drain overlap capacitances for \( M_{2,1} \) and \( M_{2,2} \),
but the transistors \( M_{2,1} \) and \( M_{2,2} \) reduce these error with
the same gain factor \( LG \) as mentioned before. The loss in
the SI-Integrator used in this design is less than 0.1%. The
scaling factor \( K \) in figure 2 is controlled by the length and
the width of MOS-transistors.

It is well known that one of the main problems using SI-
circuits is the nonlinear settling behavior [1]. When high
signal currents compared to the quiescent current are pro-
cessed, the nonlinear settling behavior degrades the perfor-
mance of the SI-integrator drastically. Hence, it also
decreases the performance of the \( \Sigma \Delta \)-modulator. It is, how-
ever, not possible to evaluate this problem using SPICE
as the simulation time would be enormous. It was there-
fore necessary to evaluate this problem by other means. A
‘C++’-program that modeled the SI-integrator as a nonlin-
ear component was written. The program models the SI-
integrator as build from two current copiers (CCOP) (see,
[1]). A CCOP is basically a operational transconductance
amplifier (OTA) and some switches. The OTA is in the
program described as a component with a nonlinear rela-
tionship between the input voltage and the output current.
For each sample the program solves the nonlinear settling
problem using the 2nd order Runge-Kutta algorithm. The
program was verified by comparing its results with simula-
tions using PSPICE, performed on relatively simple build-
ing blocks.

Simulations performed on the entire \( \Sigma \Delta \)-modulator
showed that the internal signal swings were increased from
approximately 1.7I to 2.4I, when the integrators were made

![Figure 1. Block diagram of the 3rd order \( \Sigma \Delta \)-modulator.](image)

![Figure 2. SI-Integrator.](image)
nonlinear using a square law relationship (to model the behavior of MOS transistors) for the OTA's in the CCOP's. Furthermore, the nonlinear settling causes a DC component at the output of the modulator which causes nonharmonics in the signal band for small input amplitudes. To reduce the effect of this a quiescent current of 3$I$, i.e., $N = 3$ was chosen.

4. MEASUREMENT RESULTS

The ΣΔ-modulator is measured using a LabVIEW setup. The 1-bit output of the ΣΔ-modulator is captured using a high speed digital data acquisition board located in a PC that also runs the LabVIEW software. The LabVIEW analysis software assume that two levels of the 1-bit output from the ΣΔ-modulator is in the set $\{-1, +1\}$.

All measurements are based on FFT-analysis of 16384 output samples captured from the ΣΔ-modulator. Averaging is used to reduce the variances of the measured spectra.

All of the measurements of the ΣΔ-modulator are performed with a supply voltage of $V_{DD} = 3.3V$, and the bias current in the first integrator is $NI = 96.0\mu A$ ($I = 32.0\mu A$). The signal bandwidth is $0Hz - 5.5kHz$ and the sampling rate is $f_s = 600kHz$.

First the relationship between the 1-bit output is determined and the input voltage. This is done by applying a sinusoid with a frequency of $3kHz$ and an amplitude of $0.1V_{peak}$ to the input of the ΣΔ-modulator. Using FFT-analysis the amplitude of the sinusoid at the output of the modulator is 0.0242 RMS corresponding to $-32.3dB$.

The expected amplitude is calculated from:

$$G = \frac{V_{in, peak}}{\sqrt{2}} \frac{1}{R_{in}} \frac{1}{I} = \frac{0.1V_{peak}}{\sqrt{2} 89.1k\Omega \cdot 32.0\mu A}$$

$$= 0.0247 \text{ RMS} \sim -32.1dB$$  (2)

where $R_{in} = 89.1k\Omega$ is the resistor at the input of the modulator shown in figure 2. The results above show good agreement between the measured gain and the expected gain, they only differ with 0.2dB.

In figure 3(a) the output spectrum of the ΣΔ-modulator is shown for no input signal applied. A ΣΔ-modulator with zero input has a large tone at $\frac{f_s}{2}$. When a small DC component is present at the input of the modulator the tone at $\frac{f_s}{2}$ splits into two tones located at (1 $\pm$ DC)$\frac{f_s}{2}$ [2]. This effect is seen in figure 3(a). The small DC component at the input of the modulator also causes nonharmonic tones to appear in the signal band, as seen in 3(b). These tones are are correlated with tone at $\frac{f_s}{2}$. This effect was also observed in the simulation using the 'C++' program. If the DC component is removed then the tones in the signal band disappears.

In [1] it is shown that the noise power in SI circuit increases by a factor of two when the storage capacitance, $C_{sz}$ and $C_{zi}$ in figure 2, is halved. The chip is designed so that the storage capacitance can be halved and hence the above effect can be tested. With zero input current the noise power in the frequency range $1600Hz$ to $2800Hz$ is measured to $-93.4dB$. With the storage capacitance halved the noise power was measured to $-90.0dB$, i.e., a difference of $3.4dB$ which indicates that effect of halving the storage capacitance is as described in [1]. In both cases the noise power was estimated by averaging 32 spectra.

In figure 4 the output spectrum of the modulator is shown, with a $3kHz$-sinusoid and an amplitude of $1V_{peak}$ (6dB below MSA) applied to the input. In figure 4(a) a lot of tones are observed around $\frac{f_s}{2}$. This can be explained by the fact that the modulator will see the input sinusoid as slowly varying DC because of the high oversampling ratio. Previously it was stated that a small DC component splits the tones at $\frac{f_s}{2}$ into two tones. As the input is varying in time the tones at $\frac{f_s}{2}$ are effectively FM-modulated with the input signal. This was also verified by simulations.

In figure 4(b) the input sinusoid is clearly visible in the output spectrum. A small 2nd order harmonic is also present due to the large amplitude of the input sinusoid. No nonharmonic tones are visible at low frequencies in contrast to figure 3(b). This is partly because the modulator is busy coding the input sinusoid and partly because the order of ΣΔ-modulator is higher than 2 which makes it more chaotic and thus diffusing the tones.

In figure 5(a) the SNR as a function of the input signals is shown. The measurements are based on averages of 16 spectra for each input amplitude to lower the variances of the measured SNR. The harmonic distortion in figure 5(b) is measured the same way. The peak SNR is approximately 74.5dB. Considering the low power consumption of this ΣΔ-modulator, which is 2.5mW, this SNR is, to the knowledge of the authors, significantly higher than previously reported ΣΔ-modulator implemented using switched-current technique.

The maximum SNR is measured for a RMS value of the input amplitude of $-6.17dB$. The ΣΔ-modulator was design to have a MSA of 0.69$I$. The RMS value of a sinusoid with
an amplitude of $MSA$ is, $RMS = 20 \log\left(\frac{0.69}{\sqrt{2}}\right) = -6.23$ dB. Hence, the measured and expected $MSA$ correspond very well.

For input amplitudes exceeding $MSA$, the harmonic distortion increases significantly as shown in figure 5(b), but the modulator does not become unstable. This is seen by the fact that the modulator does not generate a sustained oscillation at the output when the input signal is removed, but enters a stable idle state. This property results from the clamping of large internal signals in the class A switched-current integrators. For high order modulators (3rd order and higher), it is of outmost importance to scale the $\Sigma\Delta$-modulator so that the internal signals are clamped, when an input signal is present with an amplitude of $MSA$. This will in most situations ensure reliable and stable operation of the modulator.

5. CONCLUSION

In this paper a 3rd order switched current-$\Sigma\Delta$-modulator is presented. Design aspects at the system level are presented together with detailed measurements. By feeding the $\Sigma\Delta$-modulator with multiple input signals and by allowing for increased noise in the integrators as they approach the comparator, the internal signal swings are kept at a minimum. This effectively results in low current consumption and hence low power consumption. At a supply voltage of $V_{DD} = 3.3V$, the power consumption of the $\Sigma\Delta$-modulator is 2.5$mW$ when it operates at a sampling frequency of $600kHz$. With this low power consumption the signal-to-noise-ratio is as high as $SNR = 74.5$dB. Due to internal clamping in the integrators and proper scaling, the stability properties of the $\Sigma\Delta$-modulator are excellent.

ACKNOWLEDGEMENTS

Ivan H. H. Jørgensen acknowledges the Ph.D. scholarship granted by the Danish Technical Research Council.

REFERENCES