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A 100 MHz Synchronized OEIC Photoreceiver in N-well, CMOS Technology

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Abstract—We analyze and demonstrate a synchronized CMOS photoreceiver for the conversion of optical inputs of pulse-light to electronic digital signals. Small-signal and photonic analysis of the proposed circuit are detailed. The photoreceiver was operated at 100 MHz with only 13.3 fJ/pulse of 830-nm input light. Its effective area is 100 x 60 µm² which makes this monolithic photoreceiver extremely important for use in data storage and optical interconnection applications.

I. INTRODUCTION

It is reported in [1] that by 2001, the integration density for silicon CMOS field-effect transistor logic is expected to be up to 13 million transistors and the projected on-chip clock rate to be 600 MHz. The enormous bandwidth that will be available for computation and switching on a silicon CMOS photoreceiver for the evolution of optoelectronic very-large-scale integrated circuits (OE-VLSI).

In this paper we report about a monolithic photoreceiver, in full CMOS technology, for conversion of optical pulses to electronic digital signals.

II. OPERATIONAL PRINCIPLE AND ANALYSIS

II.a. Photoreceiver circuit

The schematic of the synchronized photoreceiver [2] is shown in Fig. 1. The load capacitance $C_L$ is the capacitance of the external pad and package. It is estimated at 5 pF. The post-amplifier of MI-M7 is therefore buffered by two levels of complementary CMOS inverters. The input capacitance of the buffer stage is typically between 50 fF and 100 fF. The local p-n junctions available in CMOS technology are exploited to build vertical p-n-p BJT transistors [2].

Since the base of Q2 is exposed to the light, photoDarlington current $I_D$ is induced and given by $I_D = (\beta + 1)I_{ph}$, where $\beta$ is the BJT current-gain. This current $I_D$ is reflected back from the photodiode. The post-amplifier is therefore buffered by two levels of complementary CMOS inverters. The input current of the buffer stage is typically between 50 fF and 100 fF. The local p-n junctions available in CMOS technology are exploited to build vertical p-n-p BJT transistors [2].

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The output current is defined as the difference of the two drain currents $I_{rep}$ and $I_{th}$. The current-mirror comparator provides the two logical output voltages $V_{out}$: a logical high output voltage for $I_{rep}$ less than $I_{th}$, and a logical low output voltage for $I_{rep}$ higher than $I_{th}$. So the stable state of $V_{pad}$ is at 5-V, the injection of pulse of light changes the state of $V_{pad}$ to a digital pulse of 0-V.

Fig. 1. The proposed CMOS synchronized photoreceiver circuit.

This 0.7-µm 5-V n-well CMOS technology, $\beta = 22.5$ and the generated photocurrent is rearranged by reflection in this design by $I_{rep} = 177509I_{ph}$.

During measurement, the light pulse delay should take a few ns from the corresponding half-cycle, when clock is at its low state, in case to leave the maximum of time to the photocarrier diffusion current generated in the n-well/substrate photodiode.

The proposed photoreceiver has two new features in its pooled photoDarlington configuration. The first feature is that Q1 and Q2 are controlled by M8 and M9 rather than a classic Darlington structure. This pooled photoDarlington synchronizes the photoreceiver circuit. The second is the pull-up of the base voltage of the phototransistor Q2 junction to auto-reverse its base-collector when the clock is high, instead of the conventionally used phototransistor in [4].

The auto-reverse voltage modulates the n-well/substrate depletion layer [2, 5] and removes the excess charge at the base of Q2 during the first half-cycle, to just reduce the diffusion delay of the generated photocarriers to reach the junction.

II.b. Small-signal analysis

The small signal behavior of the post-amplifier M1-M7 of Fig. 1 is very important to compare the performance of the post-amplifier M1-M7 in the two following cases: (1) when it is loaded by an ideal current source; and (2) when it is loaded by the preamplifier Q1 and Q2.

The small-signal transconductances of M1-M7, and their output conductances are noted $g_{m_i}$ and $g_{ds_i}$, respectively, with $i = 1,...,7$. $C_{gs}, C_{gd},$ and $C_{gd}$ are, respectively, the gate-to-source, -to-drain and substrate-to-drain device capacitances. $g_{m_i}(q_i), g_{d_i}(q_i)$ and $g_{d_i}(q_i)$ are, respectively, the small-signal transconductances, input conductances and output conductances, and are indexed by their appropriate bipolar transistors Q1 and Q2. The use of a symbolic small-signal simulator like ISAAC [6] yields a quite complicated open-loop transfer function

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Table I. The equivalent expression of the simplified parameters of Fig. 2(b) as a function of the device transconductances $g_m$ and conductances $g_{ds}$ of M1-M7, and the capacitance coupling gate-to-source $C_{gs}$, gate-to-drain $C_{gd}$, and bulk-to-drain $C_{bd}$ of the output stage M4 and M7.

<table>
<thead>
<tr>
<th>Expression</th>
<th>( R_{out} = \frac{1}{g_{m7} + g_{ds7} + g_{ds6} + g_{ds2} + g_{ds1}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_0 = C_{gs7} )</td>
<td>( C_{out} = C_{bd7} + C_{bd4} + C_{gd7} + C_L )</td>
</tr>
<tr>
<td>( V_0 = \frac{g_{m2}}{g_{m6}} )</td>
<td>( I_0 = \frac{g_{m2}}{g_{m1} + g_{ds1}} )</td>
</tr>
<tr>
<td>( V_{in} )</td>
<td>( I_{in} )</td>
</tr>
</tbody>
</table>

\( R(s) = \frac{V_{out}}{I_{in}} \), with a second-order numerator and a third-order denominator which are too lengthy to be usefully reproduced here. However, the complete numerical small-signal analysis and curves generated by ISAAC give a good insight.

**II.b.1. Ideal analysis**

To achieve analytical relationships between the pole-zeros and the small-signal device parameters: the post-amplifier M1-M7 is presented by a simplified circuit and its small-signal model \([7]\) is shown in Fig. 2. Furthermore, some simplifications introduced in the generated expressions overcome the complexity of the full small-signal equations. The relationship between the parameters shown in Fig. 2(b) and the parameters of the circuit is revealed in Table I.

The transimpedance gain \( R(s) \) can be expressed as follows

\[
R(s) = \frac{V_{out}}{I_{in}} = -R_0 \frac{1 - s/z_1}{1 + A s + B s^2}
\]

where \( R_0, z_1, A, \) and \( B \) are given in Table II as functions of the small-signal device parameters.

![Fig. 2. (a): simplified post-amplifier circuit for small signal analysis. (b): simplified small signal model of the post-amplifier.](image)

**Table II.** Analytical expression of the transfer function characteristics of Fig. 2(b) as a function of \( g_m, g_{ds} \) of M1-M7 and \( C_{gs}, C_{gd}, C_{bd} \) of the output stage M4 and M7.

\[
R_0 = \frac{g_{m2} g_{m7}}{g_{m1} g_{m6} (g_{ds4} + g_{ds7})}
\]

\[
A = \frac{C_{gd4} + C_{bd4} + C_{bd7} + C_{gd7} + C_L + g_{m7} g_{gd7}}{g_{m6} (g_{ds4} + g_{ds7})}
\]

\[
B = C_{gd7} g_{gd7} + (C_{gd7} + C_{gd4}) (C_{bd4} + C_{bd7} + C_{bd4})
\]

The open-loop transfer function \( R(s) \) allows an easy expressions of the zero \( z_1 \) and the two poles \( p_1 \) and \( p_2 \) of the post-amplifier in the following expressions

\[
z_1 = \frac{g_{m7} C_{gd7}}{1 + A s + B s^2}
\]

\[
p_1 = -A \frac{g_{m6} (g_{ds4} + g_{ds7})}{g_{m6} (C_{gd4} + C_{bd4} + C_{bd7} + C_{gd7} + C_L) + g_{m7} g_{gd7}}
\]

\[
p_2 = -A \frac{g_{m6} (g_{gd4} + g_{bd4} + g_{bd7} + g_{gd7} + C_L) + g_{m7} g_{gd7}}{C_{gd7} C_{gd7} + (C_{gd7} + C_{gd4}) (C_{bd4} + C_{bd7} + C_{bd4} + C_L)}
\]

The zero \( z_1 \) occurs in the right half-plane due to the feed-forward path through \( C_{gd7} \). The pole \( p_1 \) is more dominant than \( p_2 \) as their expressions as the typical ratio of \( g_{ds}/C \) and \( g_{m}/C \), respectively, and \( g_m \) is always larger than \( g_{ds} \). The numerical analysis of the comparator in 0.7-\mu m 5-V n-well CMOS technology is done by ISAAC and is depicted in Fig. 3.

The transimpedance gain at low frequency \( R_0 \) is about 162 dB. The first pole of the post-amplifier with a capacitive load \( C_L = 1 \) pF is located at 1 KHz, the second pole is located at 2 MHz. The phase of the open-loop transimpedance gain of the post-amplifier amounts to 42° at the cut off frequency of 100 MHz.

![Fig. 3. ISAAC simulated phase and gain of the post-amplifier leaded by the discussed two cases: an ideal current source that is presented by the square marks; and (Q1, Q2) Darlington that is presented by the circle marks.](image)
The transimpedance gain at low frequency is increased up to 129 dB with a gain of 51 dB as shown in Fig. 3. The circuit proposed in Fig. 1 was designed and fabricated in a 0.7-μm 5-V n-well CMOS technology. The sampled switched-gate noise contributes to the noise discussed above and the clock feedthrough in [2], a switched-current circuit [9] seems to be a good candidate for the reduction of the switching noise and will replace M1 in the next version of this photoreceiver circuit in the future.

III. EXPERIMENTAL RESULTS

The photoreceiver occupies an effective area of only 100×60 μm² (the output buffer and pads are not included). During the experiments, Vbias is held at 0-V, the clock swings from 0 to 5-V, and the light input was given as 5-nS pulses of 830-nm laser diodes.

The photoreceiver's dynamic range of optical power is as wide as 40 dB at a bit-rate of 100 Kbps. The minimum detectable external optical energy level was 135 aJ (-45.7 dBm/beam) at this frequency, as shown in Fig. 5. We assume a detector responsivity of 0.5 A/W by considering that 25 % of the given 830-nm laser is reflected [10, which means that only 423 electrons generated in the diode n-well-substrate of Q2 are required for changing the output state. This corresponds to Iph = 13.6 nA minimum photocurrent generated and Iimp = 1.696 mA reflected current. The full time of the generated signal Vimp is Δt = 0.56 ns which is derived from \( i = C(dV/dt) \) calculations.

The photoreceiver performances in input-light dynamic range and maximum operating frequency are measured and found to be 11.6 MHz and 100 MHz, respectively.
The decrease in dynamic range at high frequencies is due to the accumulation of the photoelectrons in the substrate, which escape the refreshing phase when the clock is high [2]; the large absorption length of about $L_a = 10\mu m$ [11] for the given wavelength of 830-nm input laser and the total depth of the affected silicon by light $L_D = 4.6 L_n$ [5] result in a considerable sweep-out time. So the use of 460-nm blue laser diodes [12, 13] should reduce the penetration depth by one order of magnitude and decrease the photocarrier density which escape the refreshing phase when the clock is high.

We measured 13.3 fJ external pulse energy at 100 MHz, or $\frac{fJ}{\mu W}$ external light energy of 830-nm wavelength. The optical input of 1-ns pulses described previously. The output pattern shown in Fig. 6 matches perfectly the repetitive string of the optical input pulses described previously.

High operating frequency was measured for this first version of CMOS photoreceiver at 100 MHz. The optical input was given, repetitively, to the base of 42 in the order ‘000101011111’. ‘0’ means that no light was injected during the appropriate half clock period, and ‘1’ means that an internal input pulse of light was injected during the appropriate half clock period. The output $V_{pad}$ in its R Z format is shown in Fig. 6. An optical input of 1-ns pulses, 830-nm laser diode is used. These short laser pulses are able to generate photocurrent pulses of 5-ns duration [1]. Hence the photoreceiver is improved in a higher operating frequency. We measured 13.3 fJ external pulse energy at 100 MHz, or $-18.8 \text{ dBm/beam}$ external power. The output pattern shown in Fig. 6 matches perfectly the repetitive string of the optical input pulses described previously.

**REFERENCES**


