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A 100 MHz Synchronized OEIC Photoreceiver in N-well, CMOS Technology

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Abstract—We analyze and demonstrate a synchronized CMOS photoreceiver for the conversion of optical inputs of pulse-light to electronic digital signals. Small-signal and photonic analysis of the proposed circuit are detailed. The photoreceiver was operated at 100 MHz with only 13.3 fJ/pulse of 830-nm input light. Its effective area is 100 × 60 μm² which makes this monolithic photoreceiver extremely important for use in data storage and optical interconnection applications.

I. INTRODUCTION

It is reported in [1] that by 2001, the integration density for silicon CMOS field-effect transistor logic is expected to be up to 13 million transistors and the projected on-chip clock rate to be 600 MHz. The enormous bandwidth that will be available for computation and switching on a silicon CMOS scale integrated circuits (OE-VLSI).

II. OPERATIONAL PRINCIPLE AND ANALYSIS

II.a. Photoreceiver circuit

The schematic of the synchronized photoreceiver [2] is shown in Fig. 1. The load capacitance C_L is the capacitance of the external pad and package. It is estimated at 5 pF. The post-amplifier of M1-M7 is therefore buffered by two levels of complementary CMOS inverters. The input capacitance of the buffer stage is typically between 50 fF and 100 fF. The local p-n junctions available in CMOS technology are exploited to build vertical p-n-p BJT transistors [2].

Since the base of Q2 is exposed to the light, photo-Darlington current I_D is induced and given by

\[ I_D = (β+1)^2 I_{ph}, \]

where β is the BJT current-gain. This current I_D is reflected back from the photoDarlington and is mirrored and amplified by M2 in I_{amp}. The current I_{amp} will be compared with a reference bias current by M3-M7 [3]. This results in a return-to-zero (RZ) format. The gate of M7 is connected to the diode-connected M6 to replicate I_{amp} by M7 in I_{rep}. A reference current is established by M3 and M5, and it is mirrored by M4 to establish the threshold current I_{th} and the bias voltage V_{bias}.

The output current is defined as the difference of the two drain currents I_{rep} and I_{th}. The current-mirror comparator provides the two logical output voltages V_{out}: a logical high output voltage for I_{rep} higher than I_{th}, and a logical low output voltage for I_{rep} less than I_{th}. So the stable state of V_{pad} is at 5-V, the injection of pulse of light changes the state of V_{pad} to a digital pulse of 0-V.

II.b. Small-signal analysis

The small-signal behavior of the post-amplifier M1-M7 of Fig. 1 is very important to compare the performance of the post-amplifier M1-M7 in the two following cases: (1) when it is loaded by an ideal current source; and (2) when it is loaded by the preamplifier Q1 and Q2.

The small-signal transconductances of M1-M7, and their output conductances are noted g_{mi} and g_{dsi}, respectively, with i = 1,..., 7. C_{ps}, C_{sd}, and C_{sd} are, respectively, the gate-to-source, -to-drain and substrate-to-drain device capacitances. g_{m(0)}, g_{ds(0)} and g_{ds(0)} are, respectively, the small-signal transconductions, input conductances and output conductances, and are indexed by their appropriate bipolar transistors Q1 and Q2.

Table I. The equivalent expression of the simplified parameters of Fig. 2(b) as a function of the device transconductances \( g_m \) and conductances \( g_{ds} \) of M1-M7, and the capacitance coupling gate-to-source \( C_{gs} \), gate-to-drain \( C_{gd} \), and bulk-to-drain \( C_{bd} \) of the output stage M4 and M7.

\[
R_{out} = \frac{1}{g_m + g_{ds}}, \quad R_0 = \frac{1}{g_m + 2g_{ds} + g_{ds}^2} = \frac{1}{g_m}, \quad R_{in} = \frac{g_m}{g_{ds}}
\]

\[
C_0 = C_{gs}, \quad C_{out} = C_{gd} + C_{bd} + C_L
\]

\[
V_0 = \frac{8m2}{8m6}, \quad I_0 = \frac{8m2}{8m^2} = \frac{8m2}{8m6}, \quad I_{in} = \frac{8m6}{8m1 + 8d1}
\]

\[
V_{in} = \frac{1}{I_{in}}
\]

\[\mathcal{R}(s) = V_{out}/I_{in},\] with a second-order numerator and a third-order denominator which are too lengthy to be usefully reproduced here. However the complete numerical small-signal analysis and curves generated by ISAAC give a good insight.

Table II. Analytical expression of the transfer function characteristics of Fig. 2(b) as a function of \( g_m, g_{ds} \) of M1-M7 and \( C_{gs}, C_{gd}, C_{bd} \) of the output stage M4 and M7.

\[
\mathcal{R}(s) = \frac{8m2}{8m6 (8d4 + 8d7)} 
\]

\[
A = \frac{C_{gd} + C_{bd} + C_{gd4} + C_{bd4}}{C_{gd7} + C_{bd7} + C_L} + \frac{8m7}{8m6} \frac{C_{gd7}}{8d4 + 8d7}
\]

\[
B = \frac{C_{gd7} + C_{bd7} + C_{gd4} + C_{bd4} + C_L}{8m6 (8d4 + 8d7)}
\]

The open-loop transfer function \( \mathcal{R}(s) \) allows an easy expressions of the zero \( z_1 \) and the two poles \( p_1 \) and \( p_2 \) of the post-amplifier in these following expressions

\[
z_1 = \frac{8m7}{C_{gd7}}
\]

\[
p_1 = \frac{-1}{A}
\]

\[
p_2 = \frac{-8m6 (8d4 + 8d7)}{8m6 (C_{gd7} + C_{gd4} + C_{bd7} + C_{bd4} + C_L)} + \frac{8m7}{8m6} \frac{C_{gd7}}{8d4 + 8d7}
\]

The zero \( z_1 \) occurs in the right half-plane due to the feedforward path through \( C_{gd7} \). The pole \( p_1 \) is more dominant than \( p_2 \) as they are expressed as the typical ratio of \( g_{ds}/C \) and \( g_m/C \), respectively, and \( g_{ds} \) is always larger than \( g_m \). The numerical analysis of the comparator in 0.7-µm 5-V n-well CMOS technology is done by ISAAC and is depicted in Fig. 3.

The transimpedance gain at low frequency \( \mathcal{R}_0 \) is about 162 dBΩ. The first pole of the post-amplifier with a capacitive load \( C_L = 1 \) pF is located at 1 KHz, the second pole is located at 2 MHz. The phase of the open-loop transimpedance gain of the post-amplifier amounts to 42° at the cut off frequency of 100 MHz.

Fig. 2. (a): simplified post-amplifier circuit for small signal analysis. (b): simplified small signal model of the post-amplifier.

Fig. 3. ISAAC simulated phase and gain of the post-amplifier leaded by the discussed two cases: an ideal current source that is presented by the square marks; and (Q1, Q2) Darlington that is presented by the circle marks.
II.b.2. Entire analysis

The post-amplifier M1-M7 is loaded by a p-n-p Common-Collector-Common-Collector cascade (Q1, Q2) Darlington configuration by replacing \( V_{in} \) and \( I_{in} \) by \( V_P \) and \( I_P \), respectively. Since the characteristics of the circuit change due to the equivalent output impedance of the (Q1, Q2) Darlington. This output impedance can be approximated by \( 1/g_m(Q1) \), which is in parallel with \( 1/g_m(Q2) \). The approximation is done by assuming that the small-signal output resistance of the common collector configuration goes to infinity and then \( g_m(Q1) \) and \( g_m(Q2) \) are kept to zero [8].

The output stage M4 and M7 is driven from a lower equivalent resistance at the gate of M7 but does not have any effect on the performance of the circuit. Hence M7 is driven from the low resistance source of about \( 1/g_m6 \). Consequently, there is no change in the location of the poles-eros of the circuit. The voltage gain of (Q1, Q2) is close to unity by the low load impedance, \( 1/g_m1 \). Hence the post-amplifier is driven by the emitter current of Q1 which is \((\beta+1)^{-1} I_{b2}\), where \( I_{b2} \) is the input base current of Q2.

The ratio \( V_{0}/I_{0} \) expressed in table I, becomes the ratio of \( I_{0} \) by \( I_{b2} \) and is expressed by

\[
\frac{I_0}{I_{b2}} = \frac{g_m(Q2)}{g_m(Q1)} \frac{g_m(Q2)}{g_m(Q1)} \tag{5}
\]

Consequently, \( R_0 \) raises and is given by

\[
R_0 = \frac{g_m(Q2)g_m6}{g_m(Q1)g_m(Q2)} \tag{6}
\]

The numerical analysis of the comparator loaded by the (Q1, Q2) Darlington in 0.7-\( \mu \)m 5-V n-well CMOS technology is also done by ISAAC and depicted in Fig. 3. The transimpedance gain at low frequency is increased up to 178 dB. The locations of \( p_1 \) and \( p_2 \) are kept without change. At 100 MHz, the phase of the open-loop transimpedance gain of this circuit amounts to 129° with gain of 51 dB as shown in Fig. 3. Thus the performance of the proposed post-amplifier is not degraded when it is loaded by the (Q1, Q2) Darlington.

Since the gates of M8 and M9 are connected to an external large signal clock, the addition of these transistors to the previous circuit does not make any significant change as M8 and M9 contribute solely with their drain-source impedances \( r_{ds8} \) and \( r_{ds9} \), respectively. These are seen in parallel with smaller \( r_{sQ1} \) and \( r_{sQ2} \) of Q1 and Q2, respectively. Hence, the small-signal analysis performed earlier of the post-amplifier loaded by (Q1, Q2) Darlington does not change by adding M8 and M9 to the circuit. This is confirmed by ISAAC.

II.c. Noise switching circuit effects

As demonstrated in the previous description, a switching circuit (M8, M9) is needed to connect \( V_{b2} \) to a reverse voltage for refreshing after injection phase. It increases the maximum operation frequency significantly. This electrical switching circuit however causes electrical noise and large parasitic capacitance effects. The electrical noise degrades the photoreceiver performances in sensitivity and operating frequency.

Since there is no gain in the refresh circuit (M8, M9), thermal noise will play a very important role in the stability of the base signals. When a clock is applied to the base-collector capacitors \( C_{bc1} \) and \( C_{bc2} \) of Q1 and Q2, respectively, they are seen in parallel. Their top plates are charged to the base voltage and their bottom plates are connected to the collector voltage. These capacitances introduce a \( KT/C \) thermal noise which limits the bandwidth of the circuit.

The sampled switched-gate noise contributes \( \sqrt{KT/C_f} \approx 6.44 \mu V \text{rms} \) at room temperature and a noise density of 6.44 nV/\( \sqrt{Hz} \) for a bandwidth above 100 MHz, where \( C_f \) is the equivalent capacitance of the parallel connection of \( C_{bc1} \) and \( C_{bc2} \).

As a consequence to the noise discussed above and the clock feedthrough in [2], a switched-current circuit [9] seems to be a good candidate for the reduction of the switching noise and will replace M1 in the next version of this photoreceiver circuit in the future.

III. EXPERIMENTAL RESULTS

The circuit proposed in Fig. 1 was designed and fabricated in a 0.7-\( \mu \)m 5-V n-well CMOS technology. Fig. 4 shows the photograph of the synchronized photoreceiver under test. Measurement with well area \( A_{Q2} \) of 60 x 60 \( \mu \)m\(^2\) and under a dark laboratory environment result in a dark-current of about 154 nA, using an hp_4145B semiconductor parameter analyzer.

The photoreceiver occupies an effective area of only 100 x 60 \( \mu \)m\(^2\) (the output buffer and pads are not included). During the experiments, \( V_{bias} \) is held at 0-V, the clock swings from 0 to 5-V, and the light input was given as 5-ns pulses of 830-nm laser diodes.

![Photograph of the dynamic photoreceiver under test.](image)
We have established a strategy for the conception of an original monolithic CMOS photoreceiver. This strategy is based on the use of the inexpensive CMOS technology for sensing and digitizing optical input pulses. The CMOS photoreceiver is refreshed after each injection of light to avoid the accumulation of the deeply generated photoelectrons in the substrate. Our photoreceiver is designed in standard 0.7-μm 5-V n-well CMOS technology with an effective area of 100×60 μm². The maximum frequency achieved for the demonstrated photoreceiver is 100 MHz with only 13.3 fJ pulse external light energy of 830-nm wavelength.

The detailed conception of CMOS photoreceiver should play a significant role in the evolution of the state-of-the-art monolithic lightwave receiver, because the realization of a high-speed photoreceiver in CMOS technology offers the possibility to incorporate the sensor and the processing circuitry in a single IC.

REFERENCES


