Compact All-optical Parity calculator based on a single all-active Mach-Zehnder Interferometer with an all-SOA amplified feedback

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Compact All-Optical Parity Calculator Based on a Single All-Active Mach Zehnder Interferometer with All-SOA Amplified Feedback

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An all-optical signal processing circuit capable of parity calculations is demonstrated using a single all-integrated all-active SOA-based MZI, exploiting the integrated SOAs for feedback amplification.

I. Introduction

At present, all signal processing is done in the electronic domain. Two issues such as power consumption, footprint requirements, and cost of high-speed electronics will make optical solutions more attractive. For short-reach systems, and to simplify signal processing tasks may move into the optical domain [1]. Significant progress has been reported on optical signal processing circuits based on SOAs in fiber interferometers, including memory functionality through optical feedback [2-4]. Examples include all-optical parity checker based on two TOAs [2], and a UNI based on wavelength shifting, which is a time inverter [4]. In both configurations, an EDFA amplifies the output, which is fed back to the switch as a contrast source. In general, the EDFA contains many meters of fiber, it defines the latency of the circuit. This was identified as a problem in [2-4], where fiber-dispersion is traded in, in which a bit-input word was injected at times before the parity of the word could be detected at the output. This is not realistic in a real system, as well as solving the above problem, one also has to consider the time of flight of the fiber. The total delay of the system must be reduced. The only solution to this problem is integration, leaving SOA-based interferometers as prime candidates. Secondly, a feedback amplifier with minimum TOF, but still with sufficient output power to facilitate switching must be employed. The natural choice is the SOA, since it is able to integrate the switch and the feedback waveguide is desirable to further minimize the total TOF. The replacement of the EDFA with an SOA has already been demonstrated using the hybrid UNI [5], reducing the TOF of the feedback of an all-active MZI (incl. TOF through XOR gate). This paper reports on what we believe is the first demonstration of an all-optical signal processing circuit with feedback, and the first integrated all-active MZI switch with (integrated) SOAs as feedback amplifiers. The circuit has a wide range of applications, e.g., parity calculation and parity check.

2. Principals, applications, and experiments

Fig. 1 (a) shows a schematic of an XOR gate with a feedback. Depending on the TOF of the feedback, the circuit has different applications: for a total delay of 1ps (incl. TOF through XOR gate) of one-time slot the circuit is an adjacent-bit parity calculator / checker, where the 16 bit is XOR’d with the 2nd timeslot, and it can be used with the 3rd, etc. Assuming instead that the data consists of slotted packets of fixed number of bits, Np, and Dp is adjusted to match the TOF of one packet, the output will represent the accumulated parity of a specific (payload) bit. Inserting the parity-bits into the header will enable performance monitoring and lower the data rate, as well as lowering the error rate.

Fig. 1 (b) shows the implementation in terms of a hybrid all-active MZI switch with (integrated) SOAs, to be used at 1.556nm from a gain-switched DFB laser (GS-DFB 1), and is modulated with a periodic sequence IN from a pulse pattern generator. The output consists of Np bits at 10Gb/s, and launched into port #1 of the all-active MZI. The interferometer arms are 12cm long, while all access-SOAs are 400µm. GS-DFB 2 emits a 1.556nm laser, which is modulated with a gating sequence of period NE effective reducing the clock frequency of CLK to (10GHz) / 2, before it is injected into port #4 of the device. Without the feedback loop the output from port #3 represents the logic function IN AND CLK [5], which has a period of PCLK=IN(LCM(NE,Dp)) (LCM=Least Common Multiple). By connecting this result into port #2 via the feedback loop, exploiting amplification in SOA #3 and SOA #4, and synthesizing the bits to the input sequence, the output of the circuit will represent the adjacent-bit parity calculator if Np = 1 and Dp=1 (timeslots). Apart from this case because the MZI works as a 2-input XOR gate for signals launched into ports #1 and #2 [3]. Alternatively, by setting NpDp-NE-lengths (Np, the output will be the accumulated parity of a specific (payload) bit. In general, though, the output will represent the logic function OUT(n)=(IN(n) XOR (IN(n-Dp)) and CLK(n-Dp)) and CLK(n) where n is a bit counter. By studying this function it can be shown that for a total delay of NE-CLK(X) where X belongs to N and Y to Np, the period NyE of the output is given by the following provided that for Y n can be expressed as X=CMOZ (Np)GCD(LCM(NyE,Y)) (where GCD=Greatest Common Divisor). The requirements correspond to the output port #3 arriving at port #2 systematics.
the effect of the feedback will not be sampled by CLK. The length of the fiber memory loop was 20 m, and no attempt was made to reduce it, since this would require an irreversible customization of a 3-fiber-ribbon, while still not reducing D_T to near 1 timeslot. The TOF of the MZI is -38ps, which means that the TOF of the feedback loop should be -70ps or -20ps for adjacent-bit parity calculation at 10 and 20Gbit/s, respectively. Integrating would require -7Ops or -2Ops for adjacent-bit parity calculation.

To provide a waveguide with sufficiently low loss, enabling very sharp bends. Another speed limiting factor is the output power induced transit time effects [6]. However, successful operation at 20Gbit/s in counter propagation, also in a 1200 µm long SOA, has been demonstrated [7].

To visualize the output pulse-pattern on a sampling oscilloscope the period NPP of the pattern must be equal to the fiber length L. The oscilloscope can be triggered by either PPG 1 or PPG 2, which transmit trigger signals with periods of LCM(N,128) and LCM(N,256), respectively. Since the period P = 128cm(128/N) of AND CLK is independent of D, it is much easier to find a combination of N and D such that PD divides N, than to divide N by the complex expression for NPD given above. Satisfying the requirements for obtaining the general output period, and visualizing the result on the scope, implies an optimization of D/S (by means of a delay line) while changing the periods N and D of the input and gating sequences to meet the triggering requirements. This is an extremely difficult task, so to visualize the output we have chosen (NPD/N = 8,3) for QD), which fulfills the triggering requirements for PPG 2, for an output period of 20Gbit/s and AND CLK of LCM(3,24)

![Diagram](image)

**Fig. 1.** (a) Schematic of XOR gate with feedback. (b) Experimental setup used to prove FIFO concept.

We observe an open eye diagram corresponding to IN AND CLK, when the synchronization between the gating clock and the feedback input to port #2 is so poor that the clock samples completely outside the switching window generated by the feedback signal. When the synchronization is perfect, however, we expect an open eye diagram corresponding to the non-trivial function OUT(n). Between these extremes, the eye diagram will be closed due to partial synchronization. This is illustrated in Fig. 3 (a), which shows IN, the feedback at port #2 for three different synchronization spaces by 100ps, and the clock and CLK, respectively. The white set of feedback-bits in the second row corresponds to a misalignment of 100ps between CLK and the feedback at port #2. As the delay decreases towards 0, the eye will close, as the input to port #2 is misaligned with IN while the resulting distorted XOR switching window is sampled by the edge of the clock pulses. However, when the synchronization is perfect (delay = 0), the eye corresponding to OUT(n) opens up. This situation is shown in Fig. 3 (a). Decreasing the delay further, the eye will close again due to misalignment, and opens when the delay is -100ps, corresponding again to IN AND CLK (black set of bits). The measured eye diagrams in Fig. 3(b) illustrate the effect of changing the delay on the eye diagram. The time window generated by the feedback loop is shown in Fig. 3 (a). This proves that the feedback loop is active, since no change of eye diagram would have been observed otherwise. The transition of eye diagrams in Fig. 3(b), and the fact that a similar transition occurs as the current to SOA #2 is varied, are clear indications that the XOR function, and thus the feedback function, is working, and that the output does indeed represent the accumulating bit parity function. This is also verified by extensive modeling using a detailed time-domain model of a MZI introduced in [8].

![Diagram](image)

**Fig. 2.** Input sequence (upper), gating sequence (middle), and output sequence (lower), which unambiguously represents IN AND CLK.

**Fig. 2.** shows pulse traces of the input sequence (upper), the gating sequence (middle), and the output sequence (lower), which unambiguously represents IN AND CLK.

**3. Summary**

We have proposed and demonstrated an all-optical signal processing circuit with feedback, consisting of a single all-active MZI, and using the built-in SOAs as feedback amplifiers. The circuit processed data at 10Gbits/s, but it is capable of calculations/checking the parity of successive bits at bitrates >20Gbits/s, because of the low latency of the MZI combined with the promise of a very short, integrated feedback owing to the use of SOAs for amplification. The scheme can also be used in a less demanding scheme for parity checking in packet-switched networks.

4. References


**TuQ3 5:15 PM**

**Photonic Random Access Memory Using Serial-to-Parallel and Parallel-to-Serial Conversion**


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A novel photonic random access memory uses all-optical serial-to-parallel and electrical parallel-to-serial conversion, together with an optical clock-pulse generator and a silicon-based memory, and is demonstrated for 40-Gbit/s 16-bit burst optical packets.

**1. Introduction**

In future large-capacity optical packet-switched networks, many kinds of processing functions for high-speed asynchronous burst optical packets, such as label recognition, label swapping, buffering, bit-rate conversion, and 3R, may be needed. However, an increase in the optical packet bit rate will increase the difficulty in using electronic circuits. We have proposed a novel self-serial-to-parallel converter (self-SPC) [1] with a single optical clock pulse generator [2] for label recognition of a burst high-speed optical packet [3], and demonstrated 1-8bits 16-bit SPC [4] and 40-Gbits 16-bit 1x4 self-routing [5] in self-SPC, all bits of the incoming serial label are automatically converted to parallel bits using the single optical pulse generated based on the first bit of the label. This makes label recognition using CMOS electronics easy. An attractive way to solve the remaining problem is to develop a photonic random access memory (RAM) that can process high-speed burst optical packets. So far, fiber-loop-type buffer memories have been demonstrated. They can store an optical packet in the optical domain, but cannot forward the stored packet at an arbitrary time. Silicon electronic memory devices are very attractive because of their compact size, extremely large storage.