A 240W Monolithic Class-D Audio Amplifier Output Stage

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The audio amplifier market continuously demands improved performance at low cost. Apart from reliability, 3 performance criteria are of main interest: output power, idle loss and THD. Low THD should preferably be achieved open-loop, since a feedback loop cannot be easily added if the signal path is fully digital. For an integrated Class-D amplifier as shown in Fig. 19.1.1, all 3 performance criteria are influenced primarily by the timing and electrical characteristics of the gate drives, i.e., the circuits that drive the gates of the output switches. The input is a PWM audio signal, reproduced by the output stage at the V_OUT node. The external lowpass filter, L_OUT and C_OUT, reconstructs the analog audio signal on the loudspeaker terminal. The filter must be close to critically damped with a 4 to 8Ω load and provide maximum attenuation of the PWM carrier. This means that no degrees of freedom are left in its design, and L_OUT after C_OUT are considered fixed in the following. The influences of the gate drive output characteristics on each of the 3 main performance criteria are discussed below.

The V_IN voltage rating of the output LDMOS devices Q0 and Q1 (Fig. 19.1.2) sets a hard limit on the output power that can be delivered to a given load resistance. The supply voltage V_DD must be less than the device V_IN voltage rating by an amount large enough to account for the inevitable switching voltage overshoots. The size of the gate drive pull-down devices influences the same dependence of switching overshoots, and thus the achievable output power. For a rising-edge transition with a large output current I_OUT, the voltage at the output node V_OUT exceeds V_DD while the current builds up in the parasitic inductance L_DD of the power-supply decoupling network. Neglecting all parasitic capacitances other than C_DD (which is acceptable for LDMOS transistors working in the saturation region), it can be shown that the peak drain-source voltage V_DS,Q0 for Q0 can be approximated by

$$V_{DS,Q0} \approx V_{DD} + \sqrt{I_{OUT} \cdot \frac{2 \cdot V_{DSQ0} \cdot V_{GSQ0}}{R_{DSQ1}}}$$

(1)

where C_DD is the gate-drain capacitance of Q0 or Q1 (considered identical), V_GSQ0 is the gate-source voltage required by Q0 to conduct I_OUT (neglecting the fraction of I_OUT flowing into C_DD,Q0), and R_DSQ1 is the channel resistance of Q2. It is clear that the second term in (1) can be reduced by increasing R_DSQ1, i.e., by reducing the width of the gate drive pull-down device Q2. This allows the use of a higher V_IN without exceeding device ratings, which in turn increases the achievable output power. Symmetrical conditions result in the same dependence of V_DS,Q0 on the width of Q4. Another important parameter for Class-D amplifiers is idle power losses, which must be kept low, since the noise of a cooling air fan cannot be tolerated at low music volume. During idle operation, I_OUT equals the switching ripple current (see Fig. 19.1.3). For each rising-edge transition, I_OUT will charge the output node V_OUT towards V_DD right after Q0 is turned off. This charging process is referred to as autocommutation, and is almost lossless, since charge is merely moved from C_DD,Q1 to C_DD,Q0. However, if the current in C_DD,Q1 is large enough to cause a voltage drop across Q2 which exceeds the Q0 threshold voltage V_IN, Q0 will conduct part of I_OUT, and the resulting power dissipation in Q0 will increase power losses. It can easily be shown that this loss is avoided if:

$$R_{DS,Q1} < \frac{16 \cdot V_{f} \cdot L_{OUT}}{V_{DD}}$$

(2)

and similarly for R_DS,Q2 for the falling edge transition). This leads to an important design tradeoff for higher output power: Since a higher-power output stage must operate from a larger V_DD voltage, the widths of Q2 and Q4 must be increased to satisfy (2) and maintain low idle losses. However, this increases the overshoot voltages as given by (1). This effect is further accelerated by a larger I_OUT, and causes diminishing returns in terms of the output power achievable from higher voltage process nodes.

Low power losses also require avoiding any overlap between the conduction times for Q0 and Q1 during transitions. It has been shown that this sets an upper bound on the ratio R_DSQ1/R_DSQ2

(3)

and similarly R_DSQ2/R_DSQ1 [1], as indicated in Fig. 19.1.3. This is not a major constraint, since it can be achieved simply by selecting a sufficiently small width for Q3 and Q5, a change that does not affect (1) or (2). Since the present design uses N-type devices for Q3 and Q5, these transistors operate in the saturated region when turning on Q0 and Q1, and the above requirement on the channel resistances should instead be applied to the ratios of the respective drive currents. Moreover, it can be shown that this ratio bound must be obeyed not only for the zero dead time approach presented in [1], but also to avoid conduction overlap in systems with finite dead time t_D. The requirement causes the switch timing in the output stage to become asymmetrical, since Q0 and Q1 are now turned on more slowly than they are turned off. Given such an asymmetry, it can be shown that the minimum THD is obtained for a finite value of t_D, contrary to the common assumption that THD always increases with dead time (e.g., see [2]). Through careful optimization of the t_D-versus-Q2/Q3 (Q4/Q5) ratio, the open-loop THD performance shown in Fig. 19.1.4 has been obtained.

The amplifier was implemented in a 0.4µm/1.8µm P-bulk high-voltage BiCMOS process with 2 Al and 1 Cu metal layers. For each of the 2 half bridges, 3 pins are used for each of the terminals VDD, GND and OUT, and multiple bond wires connect each of these pins to the die, in order to ensure adequate current handling and reduce conduction power losses. The chip contains two half bridges, and when used in bridge tied load (BTL) configuration, the unclipped output power is 244W into 4Ω. To the best of our knowledge, this power level is unprecedented for monolithic output stages. While the output power is conventionally measured on a purely resistive load, a 4Ω loudspeaker is a complex load and requires additional current. To accommodate this need, the amplifier is designed to provide at least ±18A of output current during normal operation (see Fig. 19.1.5). Currents above this level will cause the output stage to automatically invert the PWM state, in order to limit the output current. This feature protects the device against an inadvertent short circuit at the output. During characterization, the speaker output terminals have been short circuited to ground and V_DD respectively. A total of 80,000 short circuit events have been applied over a -25 to +125°C temperature range without failure. A summary of the key performance measures is shown in Fig. 19.1.6, and a chip micrograph is shown in Fig. 19.1.7.

Acknowledgements:
The chip was designed by the Digital Audio design team at Texas Instruments, section manager Sreenath Unnikrishnan and design manager Dale J. Skelton, TI Fellow.

References:
Figure 19.1.1: Single-rail Class-D output stage (one half bridge shown).

Figure 19.1.2: Half bridge output stage detail.

Figure 19.1.3: Switching waveforms during idle operation.

Figure 19.1.4: THD+N measurement.

Figure 19.1.5: Output current capability.

Figure 19.1.6: Performance summary.

Output power

- \( V_{DD} = 50V \)
- \( 11A \) needed for
- \( 244W \) at \( 4\Omega \)

1 period of 1kHz sine wave

-\( +20A \)
-\( +10A \)
-\( 0A \)
-\( -10A \)
-\( -20A \)

-\( 8\Omega, \text{unclipped, } T_c=75°C \)
-\( 176W \) \( 8\Omega, 10\% \text{THD, } T_c=75°C \)
-\( 244W \) \( 4\Omega, \text{unclipped, } T_c=75°C \)
-\( 322W \) \( 4\Omega, 10\% \text{THD, } T_c=75°C \)

\( V_{DD} \) idle current

-\( 42mA \)

\( V_{DD} = 50V, f_s=384kHz, L_{OUT}=10\mu H, T_c=25°C \)

THD+N

-\( <0.07\% \) \( 8\Omega \)
-\( <0.10\% \) \( 4\Omega \), see Figure 19.1.4

Noise

-\( -110dB \)A Not limited by the output stage. -110dB (A-weighted) is achievable with a TI TAS5518 PWM modulator

Output current capability

\( \pm 18A \) See Figure 19.1.5
Figure 19.1.7: Die micrograph. The two half bridges form one bridge tied output.
Figure 19.1.1: Single-rail Class-D output stage (one half bridge shown).
Figure 19.1.2: Half bridge output stage detail.
Figure 19.1.3: Switching waveforms during idle operation.
Figure 19.1.4: THD+N measurement.
$11A_p$ needed for $244W @ 4\Omega$

1 period of 1kHz sine wave

Figure 19.1.5: Output current capability.
Output power $V_{DD}=50V$

<table>
<thead>
<tr>
<th></th>
<th>133W</th>
<th>8Ω, unclipped, $T_c=75°C$</th>
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<tbody>
<tr>
<td></td>
<td>176W</td>
<td>8Ω, 10% THD, $T_c=75°C$</td>
</tr>
<tr>
<td></td>
<td>244W</td>
<td>4Ω, unclipped, $T_c=75°C$</td>
</tr>
<tr>
<td></td>
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$V_{DD}$ idle current

|                | 42mA | $V_{DD}=50V$, $f_s=384kHz$, $L_{OUT}=10\mu H$, $T_c=25°C$ |

THD+N

<table>
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<tr>
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Noise

|                | -110dBA | Not limited by the output stage. -110dB (A-weighted) is achievable with a TI TAS5518 PWM modulator |

Output current capability

|                | ± 18A | See Figure 19.1.5                    |

Figure 19.1.6: Performance summary.
Figure 19.1.7: Die micrograph. The two half bridges form one bridge tied output.