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1/f Noise Characterization in CMOS Transistors in 0.13μm Technology

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Abstract

Low-frequency noise has been studied on a set of n- and p-channel CMOS transistors fabricated in a 0.13μm technology. Noise measurements have been performed on transistors with different gate lengths operating under wide bias conditions, ranging from weak to strong inversion. Noise origin has been identified for both type of devices, and the oxide trap density N_t, the Hooge parameter α_H and the Coulomb scattering parameter α_C have been extracted. The experimental results are compared with simulations using the BSIM3v3 MOS model.

1. Introduction

There is an increasing need for accurate low-noise circuits, as the technology-driven decrease in power supply voltage makes it increasingly difficult maintaining a high signal-to-noise ratio in modern analog designs. It is well known that a reduction in device size leads to an increased 1/f noise. In addition, as low-frequency noise is strongly technology dependent, novel processing steps introduced with technology downscaling lead to performance deviations which are difficult to predict [1]. To achieve an accurate prediction of the impact of 1/f noise on circuit performance, accurate noise modelling is required. Despite more than thirty years of research, a controversy still exists about the physical origin of 1/f noise in MOS transistors. Some authors attribute its origin to fluctuations in the total number of charge carriers [2], some to fluctuations in the mobility of carriers [3], and some to both [4]-[5]. The widely used BSIM3v3 MOS noise model implemented in commercially available circuit simulators is based on the latter approach [6].

In order to investigate the validity of noise models available to a circuit designer, in this work, a low frequency noise analysis is performed on n-channel and p-channel transistors biased both in weak and strong inversion, and both in linear and saturation regime. The noise measurement data are analyzed to identify the noise origin. The physical parameters N_t (oxide trap density), α_H (Hooge parameter), and α_C (Coulomb scattering parameter) have been extracted, and finally measurement data have been compared to simulations using BSIM3v3 noise model with noise parameters provided by the foundry.

2. Noise Models

Two main theories are used to describe the origin of 1/f noise in MOS transistors.

McWhorter carrier number fluctuations (∆N) theory explains the noise origin by the fluctuations of the channel free carriers due to the random trapping and detrapping of charges in the oxide traps near the Si-SiO2 interface. Theoretical formulation for the drain current power spectral density S_{f_D}, based on the ∆N theory proposed by Reimbold [7] and Van Der Ziel [8] for transistors working in weak inversion, is given by

\[ S_{f_D} = \frac{q^4 N_t}{kT W L} \gamma C_{ox} \frac{I_D^2}{f} \]

where \(N_t\) is the trap density, \(\gamma\) (10^-8 cm) is the tunnelling constant for the traps, and \(\eta\) is the weak inversion slope factor, given by \((C_{ox}+C_D+C_{it})/C_{ox}\), with \(C_{ox}, C_D\) and \(C_{it}\) being the oxide, depletion and interface trap capacitances per unit area, respectively (\(W, L, q, kT\) have their usual meaning). Experimental results in general show that the formalism (1) explains very well 1/f noise in weak inversion. In fact, the value of \(N_t\) can be extracted from noise measurements against drain current, if other parameters from (1) are known. Furthermore, this parameter is related to the BSIM noise parameter NOIA as \(N_t=NOIA/q\). For transistors working in strong inversion in the ohmic range, the ∆N-based model of \(S_{f_D}\) can be expressed by [9]

\[ S_{f_D} = \frac{q^2 kT N_t \mu_{eff}^2 W}{\gamma} \frac{V_{DS}^2}{L^3} \frac{I_D^2}{f} \]

with \(V_{DS}\) being drain-source voltage and \(\mu_{eff}\) effective mobility.

The second 1/f noise theory, Hooge mobility fluctuation (∆μ) theory [3], explains the origin of 1/f noise by the fluctuations of bulk mobility with the empirical relation for homogeneous semiconductors, given by

\[ S_{f_D} = \frac{\alpha_H I_D^2}{N} \frac{1}{f} \]

where \(\alpha_H\) is Hooge parameter, constant for a given technology and \(N\) the total number of carriers under the gate. After estimation of \(N\), it can be shown [9] that for a MOS transistor working in the linear region the following applies

\[ S_{f_D} = \alpha_H q \mu_{eff}^2 \frac{W}{L^3} (V_{GS} - V_{th}) \frac{V_{DS}^2}{f} \]
The measured 1/f noise in n-MOS transistors in strong
inversion in the ohmic region usually shows constant
$S_{TD}/I_{D}^2$ versus gate bias voltage, in agreement with (2),
which can not be predicted by the $\Delta \mu$ model, because of
the bias-independent $\alpha_{g}$; thus, the 1/f noise origin for n-
devices is attributed to the number fluctuation theory. On
the other hand, the observed dependence on the gate bias
for the same region for p-channel transistors is following the
$\Delta \mu$ theory, in line with equation (4), and can not be
explained by $\Delta N$. However, quadratic variation of $S_{TD}$ versus
drain current, following the $\Delta N$ model described by (1), is observed for both n- and p-transistors in weak
inversion, and can not be explained by the Hooge model.
This controversy, known from the experiments published in
the literature, has been observed in our experiments as well, which will be presented in the next section.

Recent modelling efforts combine the two previously
described approaches in the correlated number and mobility
fluctuations $\Delta N-\Delta \mu$ model [4]-[5], in an attempt to
come to a universal model valid for both n- and p-channel
transistors in all operation regions. This model takes into
account that the oxide/interfacial traps, apart from modulating
the number of carriers, indirectly interact with the
carrier mobility through Coulomb scattering. By this
approach, the normalized drain current noise spectral density
takes the form presented by Gibbudo [5]

$$
\frac{S_{TD}}{I_{D}^2} = [1 + \alpha_{e} \mu_{eff} C_{ox} \frac{I_{D}}{g_m}] \frac{g_m}{I_{D}} \frac{S_{V_{fb}}}{(g_m)^2} \frac{S_{V_{fb}}}{V_{fb}}
$$

(5)

where $\alpha_{e}$ is scattering parameter and $S_{V_{fb}}$ is the flatband
voltage spectral density given by

$$
S_{V_{fb}} = \frac{q^2 kT N_t}{\gamma W/L C_{ox}^2 \delta f}
$$

(6)

Since for weak

$$
g_m \approx \frac{q}{kT \eta}
$$

(7)

and by neglecting the scattering term in (5), it can be noticed that

$$
\frac{S_{TD}}{I_{D}^2} = \left(\frac{g_m}{I_{D}}\right)^2 \frac{S_{V_{fb}}}{g_m}
$$

(8)

equals equation (1). Similarly, by plugging in the formulas
for $\mu_{eff}$ and $L_{g}$ in the linear region in (5), it can be shown that the input-referred noise voltage density takes the form

$$
S_{V_{g}} = \left[1 + \alpha_{s} \mu_{0} C_{ox} (V_{GS} - V_{th})\right] \frac{S_{V_{fb}}}{g_m}
$$

(9)

where $\mu_{0}$ is the low-field mobility and $V_{GS}$ the gate-
source voltage.

The $\Delta N-\Delta \mu$ model described shows a satisfactory fit-
ting to the experimental data for both p- and n-channel
devices. However, critical discussions on its exactness exist
[10]. A form of the unified model noise expression (5)-(9)
is implemented in the BSIM3v3 circuit simulator model
[6].

3. Experimental Study

3.1. Measurement Set-Up

The devices studied are fabricated in a 0.13μm CMOS
technology with oxide thickness 2.4nm, n+/p+ poly gate,
Figure 1: Normalized drain current noise $S_{ID}/I_D^2$ and $(g_m/I_D)^2$ ratio (f) versus drain current for $V_{DS}=50$mV for NMOS with various transistor lengths. L=0.26(□), 0.5 (×), 1 (●) and 2 (+) μm.

Figure 2: Normalized drain current $S_{ID}/I_D^2$ noise and $(g_m/I_D)^2$ ratio (×) versus drain current for $V_{DS}=50$mV for various PMOS transistor lengths. L=0.26(□), 0.5 (×) and 1 (●) μm.

Figure 3: Input referred noise $S_{Vg}$ versus gate overdrive voltage for $V_{DS}=50$mV for various NMOS transistor lengths. Simulation (f), L=0.26(□), 0.5 (×), 1 (●) and 2 (+) μm.

Figure 4: Input referred noise $S_{Vg}$ versus gate overdrive voltage for $V_{DS}=50$mV for various PMOS transistor lengths. Simulation (×), L=0.26(□), 0.5 (×) and 1 (●) μm.

dage for n-transistors, and in Fig. 4 for p-transistors ($V_{DS}$ is 50mV). From these figures, the noise origin observed in Fig. 1 and 2 can be confirmed by the fact that the input noise does not depend on $V_{GS}$ for n-channel transistors, while it is proportional to $V_{GS}-V_{th}$ for p-channel transistors as predicted by (2) and (4), respectively. In our experiments, the same origin has been confirmed by the plot of $S_{ID}$ versus $V_{GS}$, not shown here. The occasionally observed $S_{ID}$ dependence on $V_{GS}$ for high overdrive voltages [12], due to the drain and source series resistances can not be observed for the relatively low bias voltages in Fig. 3. The solid lines in Fig. 3 and 4 are the results obtained by BSIM3v3 simulations. It can be seen that the simulator model predicts very well the noise of p-transistors, while discrepancies exist for the n-channel in linear region. The model predicts dependence on the gate bias similar to p-channel bias dependence. This might be due to the fact that for correct modelling when the ΔN model dominates, similarly to $\alpha_H$, the NOIB parameter should be proportional to $(V_{GS} - V_{th})^{-1}$. Besides that, it can be seen in Fig. 3 that the model provides different value of the flatband voltage, compared to the measured one. The mean value of $\alpha_H$ for p-transistors with different dimensions is about $4.5 \cdot 10^{-4}$. This value is obtained from the measurement data by using a formula similar to (4) with $S_{ID}$ expressed as a function of $I_D$, $V_{GS}$ [9] that does not require the measurement of mobility attenuation factor $\theta$. The values of $\alpha_H$ for p-channel transistors, extracted using (9), have values $7.5 \cdot 10^{-4} - 9.5 \cdot 10^{-4}$ (V/C). The values extracted are similar to the values reported for the same technology node [13].

$S_{ID}$ versus drain current for $V_{DS}=0.45$V for various dimensions of p- and n-transistors is shown in Fig. 5 and 6, along with the simulated data. As expected, the drain current spectral density shows a quadratic dependence on the drain current in weak inversion for $V_{DS}=450$mV as well as for $V_{DS}=50$mV. As for the transistors working in linear region, measurements for p-channel transistors match very well simulations, while for n-transistors discrepancies are observed. The slope of the curve of $S_{ID}$ versus
drain current is the same for measured and simulated data in Fig. 5 while the measured values are somehow greater than simulated.

![Figure 5: Drain noise spectral density S_{1f} versus drain current for V_{DS}=450mV for various NMOS transistor lengths. Simulation (-), L=0.26(□), 0.5(×) and 2 (+) µm.](image)

![Figure 6: Drain noise spectral density S_{1f} versus drain current for V_{DS}=450mV for various PMOS transistor lengths. Simulation (-), L=0.26(□), 0.5(×) and 1 (●) µm.](image)

4. Conclusion

In this work, low frequency noise has been investigated on MOS transistors from 0.13µm technology. It has been observed that the noise in n-transistors originates from the number fluctuation theory, while the noise in p-MOS is due to the number fluctuations with correlated mobility fluctuations. Values of the physical parameters extracted match well the values for similar technologies. The simulation result show very good match with the measured data for p-transistors, while some discrepancies for n-transistors are observed.

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6. References


