De-embedding and Modelling of pnp SiGe HBTs

Hadziabdic, Dzenan; Jiang, Chenhui; Johansen, Tom Keinicke; Fischer, G.G.; Heinemann, B.; Krozer, Viktor

Published in:
Proceedings of the 2nd European Microwave Integrated Circuits Conference

Link to article, DOI:
10.1109/EMICC.2007.4412682

Publication date:
2007

Document Version
Publisher's PDF, also known as Version of record

Link back to DTU Orbit

Citation (APA):
De-embedding and Modelling of pnp SiGe HBTs
D. Hadziabdic\textsuperscript{1}, C. Jiang\textsuperscript{1}, T. K. Johansen\textsuperscript{1}, G.G. Fischer\textsuperscript{2}, and B. Heinemann\textsuperscript{2}, V. Krozer\textsuperscript{1}

\textsuperscript{1}ElectroScience, Oersted-DTU, Technical University of Denmark
Oersteds Plads 348, 2800 Kgs. Lyngby, Denmark
dh@oersted.dtu.dk

\textsuperscript{2}IHP
Im Technologiepark 25, D-15236 Frankfurt (Oder), Germany
gerhard.fischer@ihp-microelectronics.com

Abstract—In this work we present a direct parameter extraction procedure for SiGe pnp heterojunction bipolar transistor (HBT) large-signal and small-signal models. Test structure parasitics are removed from the measured small-signal parameters using an open-short de-embedding technique, improved to account for the distributed nature of the interconnect lines. Good agreement is achieved between the small-signal model of the HBT and the measurements. Parameters for the large-signal VBIC model are extracted based on multi-bias small-signal model extraction, leading to consistency between measured and modeled $f_T$.

I. INTRODUCTION

A complementary BiCMOS (CBiCMOS) technology is a promising approach to achieve low voltage supply, low power consumption and high speed simultaneously in millimetre-wave applications. The main challenge to develop such a process is to integrate high performance pnp transistors in a BiCMOS technology. IHP’s 0.25 $\mu$m SiGe:C CBiCMOS process offers a successful combination of npp HBTs with $f_T/f_{\text{max}}$ of 170/170GHz and pnp HBTs with $f_T/f_{\text{max}}$ of 90/120GHz (drawn emitter area: 0.22 $\times$ 0.84 mm$^2$) [1].

Successful circuit design using this technology requires accurate circuit models for both transistor types. Modelling of npp SiGe HBT devices has been a wide area of research [3]-[5]. In this paper, we focus on the modelling of the pnp HBTs.

An accurate de-embedding of the test structure parasitics is firstly implemented to improve HBT model accuracy. Hereafter, the de-embedded measurement results are applied for a direct parameter extraction of the small-signal equivalent circuit parameters. The model is verified by comparison of the simulated and measured results up to 49 GHz. The small-signal model is utilized for parameter extraction for the large-signal VBIC95 model. The VBIC95 model [6] includes several advantages compared to the SPICE Gummel-Poon model: improved Early-effect modelling, quasi saturation, substrate and oxide parasitics, avalanche-multiplication and self-heating behaviour – all of which are important for accurate modelling of modern SiGe HBTs.

Finally, the VBIC model is experimentally verified against the measurements.

II. DE-EMBEDDING OF THE TEST STRUCTURE

A three-step de-embedding method reported in [2] is employed to remove the contribution of the test structure parasitics. This method is further developed here to account for the distribution of the interconnect lines of the test structure. The equivalent circuit for the test structure including the transistor is shown in Fig. 1. Elements $Y_{\text{line}}$, and $Y_{\text{pad}}$, model the distributed coupling of the interconnect lines and the pads to the ground. Coupling between the pads through the substrate is negligible due to the presence of the ground shield. $Y_{\text{ps}}$ is therefore assumed to be the only transmission element in the open structure. Two loading admittances of the two respective pads together with the corresponding interconnect lines are represented as the elements of the admittance matrix $Y_{\text{line}}$ as

$$Y_{\text{line}} = \begin{bmatrix} Y_{\text{open}11} + Y_{\text{open}21} & 0 \\ 0 & Y_{\text{open}22} + Y_{\text{open}12} \end{bmatrix}$$  \hspace{1cm} (1)

where $Y_{\text{open}}$ are measured admittance matrix elements of the open standard. An empirical factor $n$ is introduced to divide the $Y_{\text{line}}$ into $Y_{\text{pad}}$ and $Y_{\text{line}}$ admittance matrices as

$$Y_{\text{pad}} = Y_{\text{line}} \cdot n; \quad Y_{\text{inn}} = Y_{\text{line}} \cdot (1 - n) ,$$  \hspace{1cm} (2)

where contribution of series impedances $Z_{\text{ps}}$ and $Z_{\text{pc}}$ to $Y_{\text{line}}$ at low frequencies is assumed to be negligible. Series impedance elements, $Z_{\text{ps}}$, $Z_{\text{pc}}$, and $Z_{\text{pe}}$, are extracted as

$$Z_{\text{p}} = (Y_{\text{short}} - Y_{\text{pad}})^{-1}$$  \hspace{1cm} (3)

$$Z_{\text{pc}} = Z_{\text{p12}}$$  \hspace{1cm} (4)

$$Z_{\text{ps}} = (Z_{\text{p11}} - Z_{\text{p21}})/n_{\text{shift}}$$  \hspace{1cm} (5)

$$Z_{\text{pe}} = (Z_{\text{p22}} - Z_{\text{p12}})/n_{\text{shift}}$$  \hspace{1cm} (6)

where $Y_{\text{short}}$ is the admittance matrix of the short standard measurement, and $n_{\text{shift}}$ is introduced to correct a de-embedding error, as will be explained later.

Fig. 1 Equivalent circuit model for the HBT test structure
The factor \( n \) in (2) is found from the frequency dependence of the inductive part of \( Z_{in} \) and \( Z_{pc} \), which both can be modelled as a series-connected inductor and resistor. As shown in Fig. 2, \( L_{pc} \) is nearly frequency independent when \( n=0.65 \), meaning that only ~65% of \( Y_{line} \) admittance is due to the physical pad. Reduced frequency dependence is correspondingly observed in the extracted small-signal equivalent circuit element values of the HBT discussed.

![Fig. 2 Extracted inductances of the interconnect line on the collector side](image)

**III. EXTRACTION OF THE SMALL-SIGNAL EQUIVALENT CIRCUIT PARAMETERS**

The small-signal equivalent circuit for the pnp SiGe HBT is shown in Fig. 3 [3]. The bias dependent intrinsic part describes the active device, while the extrinsic part represents the device parasitics.

![Fig. 3 Small-signal equivalent circuit of a SiGe HBT biased in forward active mode operation](image)

**A. Oxide Capacitances**

The total base-emitter and base-collector capacitances, \( C_{in} \) and \( C_{fb} \), have been extracted from the Y-parameters of an HBT biased in the cut-off mode operation [3]. They are modelled in VBIC as sums of the fixed oxide capacitances and bias dependent junction capacitances,

\[
C_{in} = C_{bec} + \frac{C_{je} + C_{jeb}}{1 - \frac{V_{be}}{P_e}}; \quad C_{fb} = C_{bec} + \frac{C_{je} + C_{jeb}}{1 - \frac{V_{be}}{P_e} \cdot \tau_{nshif}} \quad (7)
\]

respectively, where \( C_{je} \) and \( C_{jeb} \) are zero-bias depletion capacitances, \( P_e \) and \( P_{eb} \) are built-in potentials and \( M_e \) and \( M_{eb} \) are grading terms of the two respective junctions. \( C_{bec} \) is the extrinsic base-collector zero-bias depletion capacitance. The parameters are extracted by fitting the two curves, \( (C_{je}+C_{jeb}) \) vs. \( (1-V_{be}/P_e) \) and \( (C_{je}+C_{jeb}) \) vs. \( (1-V_{be}/P_e) \) respectively, to straight lines in double logarithmic plots [4].

**B. Fixed Access Resistances and Inductances**

HBTs in saturation can be represented by a simple T-network of resistors corresponding to access resistances \( R_{bx} \), \( R_{cx} \), and \( R_e \) in Fig. 3. These resistors are found from the de-embedded \( Z \)-parameters at these bias conditions after removal of the fixed oxide capacitances as

\[
R_{bx} = \Re\{Z_{11} - Z_{12}\} \quad (8)
\]

\[
R_e = \Re\{Z_{12}\} \quad (9)
\]

\[
R_{cx} = \Re\{Z_{22} - Z_{12}\} \quad (10)
\]

The values of these resistors in deep saturation \((I_b=3mA)\) are not varying with frequency, as depicted from Fig. 4(a), over a large frequency range. The fixed resistances are found from extrapolation of the values in (8) at large base currents as shown in Fig. 4(b).

![Fig. 4 (a) Extracted values of equations (8)-(10) at \( I_b=3mA \) and \( I_e=1.5mA \). (b) Determination of \( R_{bx} \), \( R_{cx} \), and \( R_e \) from extrapolation of the \( Z \)-parameters](image)

Total access inductances of base and collector can be extracted as in (8)-(10) by using the imaginary part of the impedances. Negative collector inductance and relatively large base inductance are derived using this procedure. This indicates that the probes in the measurement setup could have been slightly shifted towards the collector side compared to the probe location in the short standard measurements. Adding 4 \( pF \) to the collector inductance and subtracting the same from the base inductance would balance both inductances. This error is compensated by the factor \( n_{shif}=1.06 \) in (5) and (6), since the compensating inductance corresponds to ~6% of the inductance of the access lines. After the compensation, the two access inductances have become negligibly small, 1.5 \( pF \), and have therefore been omitted from the equivalent circuit.
C. Substrate Parasitics

After the oxide capacitances and the fixed resistances in base and collector have been removed, the elements of the parasitic substrate transistor can be extracted through the Y-parameters of HBTs in cut-off mode operation [3]. Neglecting the $R_s$ in Fig. 3, the substrate resistance $R_s$ and the collector-substrate capacitance $C_{cs}$ have been extracted as

$$ R_s = \Re \left( \frac{1}{Y_{22} + Y_{12}} \right) ; \quad \omega C_{cs} = -\Im \left( \frac{1}{Y_{22} + Y_{12}} \right) \quad (11) $$

The extracted $C_{cs}$ is fitted to the usual depletion capacitance expression, excluding the oxide capacitance term and using the corresponding VBIC parameters, $M_s$, $P_t$ and $C_{jeb}$.

D. Hybrid-π Equivalent Circuit Modelling

The intrinsic HBT shown in Fig. 3 exhibits the well-known hybrid-π topology. The elements are extracted analytically from Y-parameters after removing the extrinsic part of the HBT except $C_{bcx}$ using the method reported in [5]. Some extracted elements vs. frequency are shown in Fig. 5.

The intrinsic HBT shown in Fig. 3 exhibits the well-known hybrid-π topology. The elements are extracted analytically from Y-parameters after removing the extrinsic part of the HBT except $C_{bcx}$ using the method reported in [5]. Some extracted elements vs. frequency are shown in Fig. 5.

![Fig. 5 Frequency dependence of the extracted elements for the hybrid-π circuit at four bias points](image)

The parameters of HBTs in cut-off mode operation [3]. Neglecting the $R_s$ in Fig. 3, the substrate resistance $R_s$ and the collector-substrate capacitance $C_{cs}$ have been extracted as

$$ R_s = \Re \left( \frac{1}{Y_{22} + Y_{12}} \right) ; \quad \omega C_{cs} = -\Im \left( \frac{1}{Y_{22} + Y_{12}} \right) \quad (11) $$

The extracted $C_{cs}$ is fitted to the usual depletion capacitance expression, excluding the oxide capacitance term and using the corresponding VBIC parameters, $M_s$, $P_t$ and $C_{jeb}$.

The intrinsic HBT shown in Fig. 3 exhibits the well-known hybrid-π topology. The elements are extracted analytically from Y-parameters after removing the extrinsic part of the HBT except $C_{bcx}$ using the method reported in [5]. Some extracted elements vs. frequency are shown in Fig. 5.

Comparison between the measured and the small-signal modelled S-parameters is shown in Fig. 6. Excellent agreement under various bias conditions is achieved in a wide frequency range. Simulated curves in Fig. 6 are based on extracted element values listed in Table 1.

![Fig. 6 Measured (o) and modelled (-) s-parameters in frequency range 0-49 GHz for the two parallel-connected HBTs biased in forward active region.](image)

| Table 1 |
| Fixed elements |
| $C_{bcx}$ [fF] | $R_{bi}$ [Ω] | $R_{na}$ [Ω] | $R_{be}$ [Ω] | $R_s$ [Ω] | $R_c$ [Ω] |
| 2.4 | 1.75 | 29 | 14.6 | 36 | 500 |

![Fig. 7 Extracted intrinsic base resistance versus collector current at $V_{ce}=1.5$ V.](image)

From the average slope of the $\omega \tau$ plot in the Fig. 5 it appears that the extracted excess phase delay $\tau$ falls with increasing collector current. The reason is that the base-collector reverse voltage and hence the collector depleton width, which contribute to the total transit time, decrease. Since the excess phase delay in the VBIC model is
independent on the bias, an average value of $0.4\,\text{ps}$ is used for the excess phase delay parameter $T_d$. Such a low value for the excess phase delay has only little impact on the small-signal behaviour well below the cut-off frequency $f_T$.

Quasi-saturation-parameters, $R_{ci}$, $\Gamma$, $V_0$ and $H_{eff}$, are found by fitting the collector current $I_c$ versus emitter-collector voltage $V_{ac}$ curves, as shown in Fig. 8. The resulting value of $R_{ci}$ was $95\,\Omega$.

Subsequently, the forward transit time parameter $T_F$, which describes the hole transport through the base region and the collector depletion region, is estimated by extrapolation of the plot of the measured forward transit time vs. inverse collector current as illustrated in Fig. 9. The $(R_{cx}+R_{ci})/C_{bc}$ term accounts for a contribution from the parasitic collector resistance.

Finally, the parameters $X_{rf}$, $V_{rf}$, $I_{tf}$ and $Q_{tf}$, which determine the transit time bias dependence, are determined from the $f_T - I_C$ curves shown in Fig. 10. Behaviour of the collector-base heterojunction was not captured by the VBIC with a high accuracy. Using an $R_{ci}=200\,\Omega$ in the parameter extraction would have yielded a remarkably better fit of the output characteristics in the quasi-saturation region as well as of the $f_T - I_C$ curve at $V_{ac}=0.5\,\text{V}$. This resistance is however much larger than expected from the layer properties of the structure.

V. CONCLUSIONS

This work focuses on modelling of high performance SiGe pnp HBT devices. Parasitics of the test structure are de-embedded taking into account distributed impedance of the interconnect lines. A de-embedding error resulting from the probe positioning inaccuracies is corrected. The elements of the small-signal equivalent circuit of the HBT are analytically extracted leading to an excellent agreement between the model and the measurements. The small-signal model has also shown to be beneficial for extraction of the VBIC model parameters. It was not possible to accurately model the transistor action in quasi-saturation, while simultaneously keeping the physical meaning of the VBIC parameters.

REFERENCES