Nanoscale patterning of electronic devices at the amorphous LaAlO3/SrTiO3 oxide interface using an electron sensitive polymer mask

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Nanoscale patterning of electronic devices at the amorphous LaAlO$_3$/SrTiO$_3$ oxide interface using an electron sensitive polymer mask


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A simple approach is presented for designing complex oxide mesoscopic electronic devices based on the conducting interfaces of room temperature grown LaAlO$_3$/SrTiO$_3$ heterostructures. The technique is based entirely on methods known from conventional semiconductor processing technology, and we demonstrate a lateral resolution of $\sim$100 nm. We study the low temperature transport properties of nanoscale wires and demonstrate the feasibility of the technique for defining in-plane gates allowing local control of the electrostatic environment in mesoscopic devices. © 2018 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/). https://doi.org/10.1063/1.5026362

Since the discovery of a two-dimensional conducting electron system (2DES) at the interface between TiO$_2$ terminated strontium titanate (STO) and lanthanum aluminate (LAO), the efforts towards exploring, understanding, and utilizing the electronic properties of oxide interfaces have attracted significant attention from all branches of physics and materials science. One example is the drive towards the integration of oxide interfaces in mesoscopic devices to complement the semiconductor heterostructures and bottom-up grown nanostructures which have been the material platform for two decades of research in quantum transport. The oxide electron systems share the properties of low dimensionality and electrostatic gateability with the conventional semiconductor systems but in addition display a wide range of phenomena such as gate-tunable superconductivity, ferroelectricity, magnetism, and spin-orbit coupling caused by strong electron-electron and electron-lattice interactions in regimes not accessible in semiconductors. However, the oxide 2DES is highly sensitive to the quality of the epitaxial interfaces and subsequent surface processing, and a range of specialized fabrication techniques have therefore been developed for realizing patterned oxide devices while protecting interfaces and limiting post processing. Such techniques range from patterned growth of the oxide top-layer by hard-mask techniques, ion irradiation, thickness variations of the top layer, or the creation of conducting nanostructures using scanning probe lithography. Such approaches are more involved than conventional semiconductor processing and often include wet etching which is difficult to control leading to limited reproducibility and resolution.

Most studies so far have considered crystalline STO-based heterostructures where the top-films are deposited at temperatures above $\sim$600 °C. Room temperature (RT) deposition such as for the amorphous LAO/STO ($\alpha$-LAO/STO) system also leads to conducting interfaces where electrons predominately originate from oxygen vacancies and usually exhibit reduced mobilities compared to crystalline LAO/STO. The key properties of gate-tunability and gate-tunable superconductivity, however, remain intact, and moreover, the highest transition temperature reported for the STO-based 2DES was achieved in the $\alpha$-LAO/STO system. Also, recently, studies were performed on the transport properties of negative-U quantum dot devices which were fabricated from $\alpha$-LAO/STO heterostructures. Thus, the $\alpha$-LAO/STO system provides an interesting system for mesoscopic oxide devices, and here, we demonstrate that the reduced deposition temperature allows patterning of the interface conductivity by a conventional electron-beam or optical lithography with only minor adjustments. We explore the limitations of the technique in terms of lateral resolution and the performance of nanoscale devices at low temperatures.

Our fabrication procedure is schematically illustrated in Fig. 1(a). The starting point is a (001) STO single crystal with a TiO$_2$ terminated surface achieved by first sonicating in ethanol and acetone at room temperature (RT) for 300 s, then for 20 min in deionized (DI) water at 70 °C, and 20 min in aqua regia (3:1:16 HCl:HNO$_3$:H$_2$O) at 70 °C. Finally, following a brief 30 s cleaning in DI water, the substrates are annealed for 60 min at 1000 °C in a tube furnace under oxygen flow and cooled to RT with a ramp rate of 100 °C/h. Substrates for e-beam(optical) lithography are then spin-coated with 2% polymethyl methacrylate (PMMA) diluted in anisole(AZ1505 photo resist) and heated for 1 min at 185 °C(115 °C) on a hot plate. Additionally, the e-beam substrates are spin-coated with a layer of SX-AR-PC 5000 e-space, which is heated for 60 s at 115 °C, to reduce distortion during exposure. PMMA(AZ1505) was exposed using standard parameters and the patterns developed in 1:3 Methyl-Isobutyl-Ketone and Isopropanol(MF-321 developer). Before growing the top-layer, the substrates were carefully cleaned in an oxygen plasma for 120 s (calibrated to remove 8 nm of PMMA) and cleaned in Milli-Q (MQ) water for 120 s at RT. Lift-off patterning of $\alpha$-LAO combined with subsequent high

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temperature annealing and deposition has previously been used for defining insulating structures in crystalline LAO/STO devices. For defining conducting structures, it is however, crucial that the exposed surface does not contain any resist residues and previous attempts excluding the last cleaning steps have been found to lead to insulating samples. We have tested the patterning technique for both e-beam lithography and optical lithography yielding similar results; in the following, we present the results obtained using the former technique. The final PMMA resist profile is shown in Fig. 1(e), and a representative AFM image of the surface terraces in the exposed channel is shown in Fig. 1(f) after the cleaning procedure. No discernible differences to the as-treated surface are observed. A top layer of 12 nm a-LAO was grown by room temperature Pulsed-Laser-Deposition (PLD). To investigate the properties of the 2DES induced at the exposed interfaces and the spatial resolution of the lithographical patterning, standard Hall-bars were defined as well as structures allowing 4-terminal measurements of leakage currents between parallel wires with varying separations and of the conductance of wires of varying widths. Hall-bar samples were fabricated with a width of \( W = 30 \) \( \mu \)m and a length of \( L = 500 \) \( \mu \)m, and Fig. 2(a) shows a representative sample after the growth of the top layer. Measurements were performed in a dilution refrigerator with a \( \sim 20 \) mK base temperature, and standard lock-in techniques were used to measure the longitudinal \( V_x \) and transverse \( V_y \) voltage drops as indicated in the figure. The samples were mounted in a sample carrier using conductive silver epoxy, and the overall carrier density was modulated by biasing the conducting back-plane of the sample (\( V_{BG} \)). No leakage was measured between neighboring Hall-bars on the samples. As seen in Fig. 2(b), the sheet resistance \( R_S = (W/L)V_x/I \) decreases upon cooling as typically observed for metallic oxide interfaces. The dependence of \( R_x \) and \( R_y \) on a perpendicular magnetic field \( B \) at 20 mK is shown in Fig. 2(c). The positive magneto-resistance in \( R_x \) is observed in all samples and has also been reported previously for oxide interfaces and has been attributed to contributions from more than one carrier type. The finite value for \( R_y \) at \( B = 0 \) is attributed to a contribution from the longitudinal voltage drop due to an off-set of the voltage probes or a non-isotropic current path in the sample. Fitting \( R_x \) and the high-field value of \( R_y \) to the two-band model as shown in the figure, we find a higher density \( n_1 = 4.75 \times 10^{13} \) cm\(^{-2}\) of low mobility \( \mu_1 = 125 \) cm\(^2\)/V s and a lower density \( n_2 = 7.5 \times 10^{12} \) cm\(^{-2}\) of high mobility carriers.
Our patterns were performed after previous measurements and after substrates exhibit superconductivity. Also, even in unpatterned growths, we find significant growth-to-growth variations when substrates exhibit superconductivity. This could be a consequence of the patterning technique and measured under the same conditions at the same time using the same batches of substrates without substrate leakage induced by the processing. In all, the results of Fig. 2 show that devices patterned on a large scale using the PMMA as a direct mask have the same properties as those made using alternative patterning approaches.

The spatial resolution of the patterning technique is crucial for fabrication of nanoscale devices. The pattern in the PMMA resist can routinely be defined with a resolution below 50 nm. The conducting interface is, however, not created until the deposition of the LAO top film in the exposed regions, and depending on the ability of the plasma cleaning step described above and of the plasma of the PLD to enter nanoscale patterns in the ~100 nm thick mask layer [Fig. 1(b)], the resulting conducting areas may be smaller than the resist openings. On the other hand, since the interface conductivity is presumably a result of oxygen vacancies created when depositing the top-layer, and that the oxygen diffusion length may be significant, this could lead to conducting regions extending beyond the resist openings. This could be the consequence of under-cut in the exposed resist profile due to exposure by electrons back-scattered from the substrate which is often the case. Thus, in the case where either of these mechanisms are significant, the actual resolution would not be set by the resolution of the lithography. To investigate this, two types of devices were fabricated allowing 4-terminal measurements of (1) the leakage currents between sets of parallel wires with varying separations, \( s = 5,2,1,0.5, 0.25 \mu m \), between the resist openings [Fig. 3(a)] and (2) the conductance of wires defined with varying widths, \( W = 5,2,1,0.5, 0.25 \mu m \) [Fig. 3(c)].

Considering first the leakage between separated structures, none of the devices showed leakage at low bias and the three largest wire separations show negligible leak currents up to a bias voltage of \( |V_{bias}| = 10 \) V at room temperature. For the wires separated by 250 nm and 500 nm, however, a leak current is observed for an applied bias of \( |V_{bias}| \sim 4.5 V \) for the 250 nm wire and at \( |V_{bias}| \sim 9 V \) for 500 nm. Note that after the devices leak, the currents in Fig. 3(b) are set by a 100 M\( \Omega \) series resistor included for protection. At low temperatures, the leakage threshold decreased to \( |V_{bias}| \sim 150 mV \) for the smallest separations probably due to the temperature dependent dielectric properties of STO (see below). For all devices, the observed leakage was reversible, suggesting the origin to be a tunneling effect between the parallel wires rather than the electronic discharge or physical rearrangement of atoms in the sample. From AFM inspection of the resist profiles, the edges of the openings have a roughness of about 25 nm, and since the measured leakage will be dominated by the points of smallest separation, the absence of leakage at low bias shows that the conducting region extends at most 100 nm beyond the resist openings and presumably much less.

Figure 3(d) shows the RT resistance of the wire devices as a function of the width. To reduce the effects of inhomogeneities, each device consists of 5 identical wires in parallel. Each wire is 100 \( \mu m \) long and has two 45 \( \mu m \) long sections that are kept at a width of 5 \( \mu m \) joined together by a central narrow section of length \( L \) and varying width \( W \).
of the 2DES and summarize, the results in Fig. 3 show that within an uncertainty of 
structure or nearby regions of the 2DES itself can be utilized 
layer, either metallic gates can be used as a part of the mask 
process onto the sample safer than the growth of the top-
system by an oxide. Alternatively, to avoid possible damage 
tively coupled metallic top electrodes isolated from the electron 
contacts (QPCs). Local gates are usually defined by capaci-
defined by the lithography), the conducting regions in the 
interface reproduce the lithographically defined openings in 
the resist openings even for the most narrow wires. To sum-
marize, the results in Fig. 3 show that within an uncertainty of 
about 25 nm (given by the roughness of the resist openings 
defined by the lithography), the conducting regions in the 
interface reproduce the lithographically defined openings in 
the resist mask.

Local electrostatic control is an important element in most 
mesoscopic devices such as quantum dots and quantum point 
contacts (QPCs). Local gates are usually defined by capaci-
tively coupled metallic top electrodes isolated from the electron 
system by an oxide. Alternatively, to avoid possible damage 
due to processing on the samples after the growth of the top-
layer, either metallic gates can be used as a part of the mask 
structure or nearby regions of the 2DES itself can be utilized 
for gating. Figure 4 demonstrates the latter approach using 

![AFM image of the device consisting of central channels and in-place side-gates. Channel width, side-gate width, and spacing between the gate and the channel were designed to be 500 nm.](https://example.com/afm_image.png)

**FIG. 4.** (a) AFM image of the device consisting of central channels and in-plane side-gates. Channel width, side-gate width, and spacing between the gate and the channel were designed to be 500 nm. (b) 2D plot displaying the effect of each gate on the conductance of the channel within the maximum range of no leak from the side gates. The two side-gates show comparable individual effects on the 2DES with the ability combined to modulate the conductance from 1 to 2 e²/h. (c) Gate cut-outs corresponding to the dashed lines in (b). The two side-gates modulate the conductance almost identically when operated separately with a much larger effect when operated symmetrically. (d) Back-gate dependence on the conductance. The reduction in gate-efficiency with lower voltage can be explained by the E-field dependence of the dielectric constant in STO.

In conclusion, we have presented a patterning approach 
for the fabrication of mesoscopic devices from STO-based 
heterostructures with room temperature grown top-layers. The technique utilizes only conventional polymer resists sen-
tive to either electron or optical exposure and allows for 
patterning with a resolution of at least 100 nm without affect-
ing the quality of the 2DES. Finally, we demonstrated devices 
implementing local electrostatic gate-control of the carrier density in narrow constrictions. Various aspects of the patterning approach were demonstrated using room tem-
perature grown amorphous LAO as the top-layer; however, 
alternative STO-based conducting room temperature grown interfaces have been reported, and we expect that the techniques reported in this study may be directly applied to 
such systems as well. The results present a simple way to 
bridge the gap between oxide-based quantum device fabrication 
and state-of-the-art semiconductor processing.

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