System-level synthesis of multi-ASIP platforms using an uncertainty model

In this paper we propose a system-level synthesis for MPSoCs that integrates multiple Application Specific Instruction Set Processors (ASIPs). Each ASIP is customized for a specific set of tasks. The system-level synthesis is responsible for assigning the tasks to the ASIPs, exploring different platform alternatives. We can allocate tasks to the different ASIPs and determine if the applications are schedulable only knowing the worst-case execution time (WCET) of each task. We can estimate the WCET only after establishing the micro-architecture of the ASIP. At the same time, an ASIP micro-architecture can be derived only knowing the assignment of tasks to ASIP. To address this circular dependency, we propose an Uncertainty Model for the WCETs, which captures the performance of tasks running on a range of possible ASIP implementations. We propose a novel stochastic schedulability analysis to evaluate each multi-ASIP platform. We use an Evolutionary Algorithm-based approach to explore the design space of macro-architecture possibilities and we evaluate it using real case studies.

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