Memory architecture for efficient utilization of SDRAM: a case study of the computation/memory access trade-off

This paper discusses the trade-off between calculations and memory accesses in a 3D graphics tile renderer for visualization of data from medical scanners. The performance requirement of this application is a frame rate of 25 frames per second when rendering 3D models with 2 million triangles, i.e. 50 million triangles per second, sustained (not peak). At present, a software implementation is capable of 3-4 frames per second for a 1 million triangle model. By using direct evaluation of certain interpolation parameters instead of forward differencing, writing back parameters to SDRAM is avoided. In software, forward differencing is usually better, but in this hardware implementation, the trade-off has made it possible to develop a very regular memory architecture with a buffering system, which can reach 95% bandwidth utilization using off-the-shelf SDRAM. This is achieved by changing the algorithm to use a memory access strategy with write-only and read-only phases, and a buffering system, which uses round-robin bank write-access combined with burst read-access.

General information
State: Published
Organisations: Department of Information Technology
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Pages: 51-55
Publication date: 2000

Host publication information
Title of host publication: Proceedings of the Eighth International Workshop on Hardware/Software Codesign
Place of publication: New York
Electronic versions:
Gleerup.pdf

Bibliographical note
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Source: orbit
Source-ID: 175390
Research output: Research - peer-review › Article in proceedings – Annual report year: 2000