Linearisation of RF Power Amplifiers - DTU Orbit (18/01/2019)

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This thesis deals with linearisation techniques of RF power amplifiers (PA), PA design techniques and integration of the necessary building blocks in a CMOS technology. The opening chapters introduces the theory of transmitter architectures, RF-signal representation and the principles of digital modulation. Furthermore different types of power amplifiers, models and measures of non-linearities are presented. A chapter is also devoted to different types of linearisation systems. The work carried out and described in this thesis can be divided into a more theoretical and system oriented treatment of linearisation systems with focus on polar modulation feedback, and a chip oriented part focusing on integrating of separate building blocks of the system on a chip. The system oriented part of this thesis deals with analog feedback linearisation systems. The Polar modulation feedback system is compared with the more traditional Cartesian modulation feedback system in terms of loop settlement and dependencies between the feedback signals. A method to calculate the distortion functions of the linearisation system (AM/AM and AM/PM) based on the distortion functions of the power amplifier is presented. Also the polar loop architecture and its suitability to modern digital transmitters is discussed. A proposal of an architecture that is suitable for digital transmitters, which means that it has an interface to the digital back-end, defined by low-pass signals in polar form, is presented. Simulation guidelines that utilize properties of the polar loop are presented. Analysis of the envelope feedback loop shows some fundamental limitations of the loop gain and the loop bandwidth due to the varying PA gain. Based on these observation a set of design guidelines for an envelope feedback loop is given. The guidelines consider trade-off between output power and necessary filter bandwidth to guarantee a certain distortion. An analysis of the dynamics of the polar loop shows that the nonlinear behaviour of the PA only degrades the stability and the precision of the envelope feedback loop. An extension to the proposed architecture is presented which improves the precision of the envelope feedback system without sacrificing the stability of the loop. The chip oriented part of this thesis deals with building blocks for polar loop linearisation including the PA itself. A description on experiments on a RF phase shifter and an amplitude detection circuit is given. The purpose is to explore the limitation on commercial available parts and to recognize the challenges in polar loop linearisation. The design of a fabricated CMOS PA is presented. The design is carried out in a standard digital Epi-CMOS which allows integration of circuitry such as the linearisation circuit. The amplifier has the highest output power compared to other published class B power in the same process. The design phase including the on-chip inductor and the lateral flux capacitors is described. The other test chips designed are envelope detectors. Three different detectors were designed. Two non-linear detectors and one linear. The two former AM-detectors have been measured. Based on these measurements the achievable spectral leakage and error vector magnitude were predicted.

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