The switching performances of the integrated high voltage power MOSFETs that have prevailing interconnection matrices are being heavily influenced by the parasitic capacitive coupling of on-chip metal wires. The mechanism of the side-by-side coupling is generally known, however, the layer-to-layer coupling and the comparison of the layout impacts have not been well established. This paper presents modeling of parasitic mutual coupling to analyze the parasitic capacitance directly coupled between two on-chip metal wires. The accurate 3D field solver analysis for the comparable dimensions shows that the layer-to-layer coupling can contribute higher impacts than the well-known side-by-side coupling. Four layout structures are then proposed and implemented in a 0.18 µm partial SOI process for 100 V integrated power MOSFETs with a die area 2.31 mm². The post-layout comparison using an industrial 2D extraction tool shows that the side-by-side coupling dominated structure can perform better than the layer-to-layer coupling dominated structure, in terms of on-resistance times input or output capacitance, by 9.2% and 4.9%, respectively.