Investigation of Transformer Winding Architectures for High Voltage (2.5 kV) Capacitor Charging and Discharging Applications

Transformer parasitics such as leakage inductance and self-capacitance are rarely calculated in advance during the design phase, because of the complexity and huge analytical error margins caused by practical winding implementation issues. Thus, choosing one transformer architecture over another for a given design is usually based on experience, or a trial and error approach. This paper presents analytical expressions for calculating leakage inductance, self-capacitance and ac resistance in transformer winding architectures (TWAs), ranging from the common non-interleaved primary/secondary winding architecture, to an interleaved, sectionalized, and bank winded architecture. The calculated results are evaluated experimentally, and through finite element (FEM) simulations, for a RM8 transformer with a turns ratio of 10. The four TWAs such as, noninterleaved and non-sectioned, non-interleaved and sectioned, interleaved and non-sectioned, and interleaved and sectioned, for an EF25 transformer with a turns ratio of 20, are investigated and practically implemented. The best TWA for a RM8 transformer in a high-voltage (HV) bidirectional flyback converter, used to drive an electro active polymer based incremental actuator, is identified based on the losses caused by the transformer parasitics. For an EF25 transformer, the best TWA is chosen according to whether electromagnetic interference (EMI) due to the transformer interwinding capacitance, is a major problem or not.

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