High-level synthesis of asynchronous circuits from control data flow graph representations - DTU Orbit (09/01/2019)

High-level synthesis of asynchronous circuits from control data flow graph representations. / Nielsen, Sune Fallgaard; Sparsø, Jens; Madsen, Jan; Hammerstoft, Jens-Peder; Hansen, Jacob Skou. Second ACiD-WG Workshop (of the european commission's fifth framework programme), Munich, Germany 28-29 January, 2002.

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