Hierarchical DSE for multi-ASIP platforms

This work proposes a hierarchical Design Space Exploration (DSE) for the design of multi-processor platforms targeted to specific applications with strict timing and area constraints. In particular, it considers platforms integrating multiple Application Specific Instruction Set Processors (ASIPs) and each ASIP is automatically synthesized and tuned for a specific set of tasks. The definition of the platform (number of processors and their interconnection) and of the micro-architecture of each single ASIP are tightly coupled. Tasks can be allocated to the different ASIPs only knowing their performance and therefore the ASIP micro-architecture. At the same time an ASIP can be derived only knowing the functionality that it has to implement, i.e. the tasks that are assigned. We break this circular dependency with an iterative hierarchical DSE, applied at platform and micro-architecture level. We evaluate different platforms and micro-architecture alternatives to find a multi-ASIP platform targeted to the input application and able to meet the design constraints. We evaluate our design flow using a MJPEG encoder application.