Hardware-efficient Implementation of Half-Band IIR Filter for Interpolation and Decimation - DTU Orbit (23/06/2019)

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This brief deals with a simple heuristic method for the hardware optimization of a half-band infinite-impulse response (IIR) filter. The optimization method that is proposed here is intended for a quick design selection at the system level, without the need for computationally intensive calculations and simulations.

The aim is to arrive at a design with low hardware complexity that is measured in terms of the number of adders. In the approach that is presented here, the filter specification is treated with some flexibility at the topmost system level. The half-band filter is implemented as a parallel connection of two all-pass filter cells. The filter is designed by first fixing the most sensitive filter coefficient to a convenient value that can be quantized by using only a few adders. Subsequently, the overdesign margin is used to coarsely quantize the remaining filter coefficients and thereby minimize hardware demands. The complexity of the resulting IIR filter is evaluated by counting all the adders in the filter, i.e., the adders for both the filter coefficients and the filter cells. The result of the method is compared with state-of-the-art works where the filter is designed by using the fixed filter specification and advanced algorithms to minimize the hardware that is used to implement filter coefficients.

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