Digital Signal Processing for a Sliceable Transceiver for Optical Access Networks

Methods to upgrade the network infrastructure to cope with current traffic demands has attracted increasing research efforts. A promising alternative is signal slicing. Signal slicing aims at re-using low bandwidth equipment to satisfy high bandwidth traffic demands. This technique has been used also for implementing full signal path symmetry in real-time oscilloscopes to provide performance and signal fidelity (i.e. lower noise and jitter). In this paper the key digital signal processing (DSP) subsystems required to achieve signal slicing are surveyed. It also presents, for the first time, a comprehensive DSP power consumption analysis for both WDM and TDM systems at 1 Gbps and 10 Gbps, discussing latency penalties for each approach. For 1 Gbps WDM system 278 pJ per information bit for 4 slices is reported at 105 ns latency penalties, whereas 3898.4 pJ per information bit at 183.5 µs latency penalty is reported for 10 Gbps. Power savings of the order of hundreds of Watts can be obtained when using signal slicing as an alternative to 10 Gbps implemented access networks.