Behavioral Synthesis of Asynchronous Circuits Using Syntax Directed Translation as Backend - DTU Orbit (22/12/2018)

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The current state-of-the art in high-level synthesis of asynchronous circuits is syntax directed translation, which performs a one-to-one mapping of a HDL-description into a corresponding circuit. This paper presents a method for behavioral synthesis of asynchronous circuits which builds on top of syntax directed translation, and which allows the designer to perform automatic design space exploration guided by area or speed constraints. The paper presents an asynchronous implementation template consisting of a data-path and a control unit and its implementation using the asynchronous hardware description language Balsa [1]. This "conventional" template architecture allows us to adapt traditional synchronous synthesis techniques for resource sharing, scheduling, binding etc, to the domain of asynchronous circuits. A prototype tool has been implemented on top of the Balsa framework, and the method is illustrated through the implementation of a set of example circuits. The main contributions of the paper are: the fundamental idea, the template architecture and its implementation using asynchronous handshake components, and the implementation of a prototype tool.

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