A Probabilistic Approach for the System-Level Design of Multi-ASIP Platforms

Application Specific Instruction-set Processors (ASIPs) offer a good trade-off between performance and flexibility when compared to general purpose processors or ASICs. Additionally, multiple ASIPs can be included in a single platform and they allow the generation of customized heterogeneous MPSoC with a relatively short time-to-market. While there are several commercial tools for the design of a single ASIP, there is still a lack of automation in the design of multi-ASIP platforms.

In this thesis we consider multi-ASIP platforms for real-time applications. Each ASIP is designed to run a specific group of tasks that we identify as a task cluster. With real-time applications, to decide how the tasks should be clustered, we perform a schedulability analysis of the system to verify if the deadlines of the applications can be met. However, to run a schedulability analysis, we need to know the WCET of each task that is available only after an ASIP is designed. Therefore, there is a circular dependency between the definition of the task clusters and the impossibility of defining them without knowing the WCET of the tasks as the ASIPs have not been defined yet.

Many approaches available in the literature break this circular dependency considering pre-defined task clusters or considering a small set of micro-architecture configurations for each ASIP. We propose an alternative approach that uses a probabilistic model to consider the design space of all possible micro-architecture configurations. We introduce a system-level Design Space Exploration (DSE) for the very early phases of the design that automatizes part of the multi-ASIP design flow. Our DSE is responsible for assigning the tasks to the different ASIPs exploring different platform alternatives. We perform a schedulability analysis for each solution to determine which one has the highest chances of meeting the deadlines of the applications and that should be considered in the next stages of the multi-ASIP design flow.

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