Twelve-bit 20-GHz reduced size pipeline accumulator in 0.25 µm SiGe:C technology for direct digital synthesiser applications

This article presents a 20 GHz, 12-bit pipeline accumulator with a reduced number of registers, suitable for direct digital synthesizer (DDS) applications. The accumulator is implemented in the IHP SG25H1 (0.25µm) SiGe:C technology featuring heterojunction bipolar transistors (HBT) with Ft/Fmax of 180/220 GHz respectively. The accumulator architecture omits the pre-skewing registers of the pipeline, thereby lowering both power consumption and circuit complexity. Some limitations to this design are discussed and the necessary equations for determining the phase jump encountered each time the control word (synthesized frequency) is changed are presented. For many applications employing signal processing after detection, this phase shift can then be corrected for. Compared to a full pipeline architecture, the implemented 12-bit accumulator reduces the number of registers by 55% and the power by approximately 32%, while obtaining the highest clock frequency for SiGe:C accumulators intended for DDS applications.

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