A Controller for Dynamic Partial Reconfiguration in FPGA-Based Real-Time Systems

In real-time systems, the use of hardware accelerators can lead to a worst-case execution-time speed-up, to a simplification of its analysis, and to a reduction of its pessimism. When using FPGA technology, dynamic partial reconfiguration (DPR) can be used to minimize the area, by only loading those accelerators that are needed at any given point in time. The DPR controllers provided by the FPGA vendors satisfy a wide range of requirements and rely on software to manage the reconfiguration. This approach may lead to slow reconfiguration and unpredictable timing. This paper presents an open-source DPR controller specially developed for hard real-time systems and prototyped in connection with the open-source multi-core platform for real-time applications T-CREST. The controller enables a processor to perform reconfiguration in a time-predictable manner and supports different operating modes. The paper also presents a software tool for bitstream conversion, compression, and for reconfiguration time analysis. The DPR controller is evaluated in terms of hardware cost, operating frequency, speed, and bitstream compression ratio vs. reconfiguration time trade-off. A simple application example is also presented with the scope of showing the reconfiguration features of the controller.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Pezzarossa, L. (Intern), Schoeberl, M. (Intern), Sparsø, J. (Intern)
Pages: 92-100
Publication date: 2017

Host publication information
Title of host publication: 2017 IEEE 20th International Symposium on Real-Time Distributed Computing
Publisher: IEEE
ISSN: 2375-5261
Main Research Area: Technical/natural sciences
Conference: 2017 IEEE 20th International Symposium on Real-Time Distributed Computing, Toronto, Canada, 16/05/2017 - 16/05/2017
Logic circuits, Logic and switching circuits, Field programmable gate arrays, Real-time systems, Dynamic partial reconfiguration, FPGA-based real-time systems, Open-source DPR controller, Open-source multicore platform, Software
A resource-efficient network interface supporting low latency reconfiguration of virtual circuits in time-division multiplexing networks-on-chip

This paper presents a resource-efficient time-division multiplexing network interface of a network-on-chip intended for use in a multicore platform for hard real-time systems. The network-on-chip provides virtual circuits to move data between core-local on-chip memories. In such a platform, a change of the application’s operating mode may require reconfiguration of virtual circuits that are setup by the network-on-chip. A unique feature of our network interface is the instantaneous reconfiguration between different time-division multiplexing schedules, containing sets of virtual circuits, without affecting virtual circuits that persist across the reconfiguration. The results show that the worst-case latency from triggering a reconfiguration until the new schedule is executing, is in the range of 300 clock cycles. Experiments show that new schedules can be transmitted from a single master to all slave nodes for a 16-core platform in between 500 and 3500 clock cycles. The results also show that the hardware cost for an FPGA implementation of our architecture is considerably smaller than other network-on-chips with similar re-configuration functionalities, and that the worst-case time for a reconfiguration is smaller than that seen in functionally equivalent architectures.
Can Real-Time Systems Benefit from Dynamic Partial Reconfiguration?

In real-time systems, a solution where hardware accelerators are used to implement computationally intensive tasks can be easier to analyze, in terms of worst-case execution time (WCET), than a pure software solution. However, when using FPGAs, the amount and the complexity of the hardware accelerators are limited by the resources available. Dynamic partial reconfiguration (DPR) of FPGAs can be used to overcome this limitation by replacing the accelerators that are only required for limited amounts of time with new ones. This paper investigates the potential benefits of using DPR to implement hardware accelerators in real-time systems and presents an experimental analysis of the trade-offs between hardware utilization and WCET increase due to the reconfiguration time overhead of DPR. We also investigate the trade-off between the use of multiple specialized accelerators combined with DPR instead of the use of a more general accelerator. The results show that, for computationally intensive tasks, the use of DPR can lead to a more efficient use of the FPGA, while maintaining comparable computational performance.

General information

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark
Authors: Pezzarossa, L. (Intern), Kristensen, A. T. (Ekstern), Schoeberl, M. (Intern), Sparsø, J. (Intern)
Number of pages: 6
Publication date: 2017

Host publication information

Title of host publication: Proceedings of the IEEE NorCAS 2017
Publisher: IEEE
ISBN (Print): 978-1-5386-2844-7
Main Research Area: Technical/natural sciences
Conference: Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC), Linköping, Sweden, 23/10/2017 - 23/10/2017
Electronic versions:
Can_Real_Pezzarossa_CR.pdf
DOIs:
10.1109/NORCHIP.2017.8124984
Source: PublicationPreSubmission
Source-ID: 140261751
Publication: Research - peer-review › Article in proceedings – Annual report year: 2017

High-level synthesis for reduction of WCET in real-time systems

The increasing design complexity of systems-on-chip (SoCs) requires designers to work at higher levels of abstraction. High-level synthesis (HLS) is one approach towards this. It allows designers to synthesize hardware directly from code written in a high-level programming language and to more quickly explore alternative implementations by re-running the synthesis with different optimization parameters and pragmas. HLS is particularly interesting for FPGA circuits, where different hardware implementations can easily be loaded into the target device. Another perspective on HLS is performance. Compared to executing the high-level language code on a processor, HLS can be used to create hardware
that accelerates critical parts of the code. When discussing performance in the context or real-time systems, it is the worst-case execution time (WCET) of a task that matters. WCET obviously benefits from hardware acceleration, but it may also benefit from a tighter bound on the WCET. This paper explores the use of and integration of accelerators generated using HLS into a time-predictable processor intended for real-time systems. The high-level design tool, Vivado HLS, is used to generate hardware accelerators from benchmark code, and the system using the generated hardware accelerators is evaluated against the WCET of the original code. The design evaluation is carried out using the Patmos processor from the open-source T-CREST platform and implemented on a Xilinx Artix 7 FPGA. The WCET speed-up achieved is between a factor of 5 and 70.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark
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Number of pages: 6
Pages: 1-6
Publication date: 2017

Host publication information
Title of host publication: Proceedings of the 2017 IEEE Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC)
Publisher: IEEE
ISBN (Print): 978-1-5386-2845-4
ISBN (Electronic): 978-1-5386-2844-7
Main Research Area: Technical/natural sciences
Conference: Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC), Linköping, Sweden, 23/10/2017 - 23/10/2017
Electronic versions:
08124945.pdf
DOIs:
10.1109/NORCHIP.2017.8124945
Source: FindIt
Source-ID: 2393856967
Publication: Research - peer-review › Article in proceedings – Annual report year: 2017

Timing organization of a real-time multicore processor
Real-time systems need a time-predictable computing platform. Computation, communication, and access to shared resources needs to be time-predictable. We use time division multiplexing to statically schedule all computation and communication resources, such as access to main memory or message passing over a network-on-chip. We use time-driven communication over an asynchronous network-on-chip to enable time division multiplexing even in a globally asynchronous, locally synchronous multicore architecture. Using time division multiplexing at all levels of the architecture yields in a time-predictable multicore processor where we can statically analyze the worst-case execution time of tasks.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Schoeberl, M. (Intern), Sparse, J. (Intern)
Pages: 89-92
Publication date: 2017

Host publication information
Title of host publication: 2017 New Generation of CAS
Publisher: IEEE
ISBN (Print): 9781509064472
Main Research Area: Technical/natural sciences
Conference: 2017 New Generation of CAS, Genova, Italy, 06/09/2017 - 06/09/2017
DOIs:
10.1109/NGCAS.2017.73
Source: FindIt
Source-ID: 2391811503
Publication: Research - peer-review › Article in proceedings – Annual report year: 2017
An Area-Efficient TDM NoC Supporting Reconfiguration for Mode Changes

This paper presents an area-efficient time-division-multiplexing (TDM) network-on-chip (NoC) intended for use in a multicore platform for hard real-time systems. In such a platform, a mode change at the application level requires the tear-down and set-up of some virtual circuits without affecting the virtual circuits that persist across the mode change. Our NoC supports such reconfiguration in a very efficient way, using the same resources that are used for transmission of regular data. We evaluate the presented NoC in terms of worst-case reconfiguration time, hardware cost, and maximum operating frequency. The results show that the hardware cost for an FPGA implementation of our architecture is a factor of 2.2 to 3.9 times smaller than other NoCs with reconfiguration functionalities, and that the worst-case time for a reconfiguration is shorter or comparable to those NoCs.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Sørensen, R. B. (Intern), Pezzarossa, L. (Intern), Sparsø, J. (Intern)
Number of pages: 4
Publication date: 2016

Host publication information
Title of host publication: Proceedings of the 10th IEEE/ACM International Symposium on Networks-on-Chip (NOCS 2016)
Publisher: IEEE
ISBN (Print): 978-1-4673-9030-9
BFI conference series: Networks-on-Chips (5000385)
Main Research Area: Technical/natural sciences
DOIs: 10.1109/NOCS.2016.7579324
Source: PublicationPreSubmission
Source-ID: 124656146
Publication: Research - peer-review › Article in proceedings – Annual report year: 2016

Argo: A Real-Time Network-on-Chip Architecture With an Efficient GALS Implementation

In this paper, we present an area-efficient, globally asynchronous, locally synchronous network-on-chip (NoC) architecture for a hard real-time multiprocessor platform. The NoC implements message-passing communication between processor cores. It uses statically scheduled time-division multiplexing (TDM) to control the communication over a structure of routers, links, and network interfaces (NIs) to offer real-time guarantees. The area-efficient design is a result of two contributions: 1) asynchronous routers combined with TDM scheduling and 2) a novel NI microarchitecture. Together they result in a design in which data are transferred in a pipelined fashion, from the local memory of the sending core to the local memory of the receiving core, without any dynamic arbitration, buffering, and clock synchronization. The routers use two-phase bundled-data handshake latches based on the Mousetrap latch controller and are extended with a clock gating mechanism to reduce the energy consumption. The NIs integrate the direct memory access functionality and the TDM schedule, and use dual-ported local memories to avoid buffering, flow-control, and synchronization. To verify the design, we have implemented a 4 x 4 bitorus NoC in 65-nm CMOS technology and we present results on area, speed, and energy consumption for the router, NI, NoC, and postlayout.

General information
State: Published
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Pages: 479-492
Publication date: 2016
Main Research Area: Technical/natural sciences

Publication information
Journal: IEEE Transactions on Very Large Scale Integration (VLSI) Systems
Volume: 24
Issue number: 2
ISSN (Print): 1063-8210
Ratings:
BFI (2018): BFI-level 2
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 2
Avionics Applications on a Time-Predictable Chip-Multiprocessor

Avionics applications need to be certified for the highest criticality standard. This certification includes schedulability analysis and worst-case execution time (WCET) analysis. WCET analysis is only possible when the software is written to be WCET analyzable and when the platform is time-predictable. In this paper we present prototype avionics applications that have been ported to the time-predictable T-CREST platform. The applications are WCET analyzable, and T-CREST is supported by the aiT WCET analyzer. This combination allows us to provide WCET bounds of avionic tasks, even when executing on a multicore processor.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, GMV
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Pages: 777-785
Publication date: 2016
Clock domain crossing modules for OCP-style read/write interfaces

The open core protocol (OCP) is an openly licensed, configurable, and scalable interface protocol for on-chip subsystem communications. The protocol defines read and write transactions from a master towards a slave across a point-to-point connection and the protocol assumes a single common clock.

This paper presents the design of two OCP clock domain crossing interface modules, that can be used to construct systems with multiple clock domains. One module (called OCPio) supports a single word read-write interface and the other module (called OCPburst) supports a four word burst read-write interface.

The modules has been developed for the T-CREST multi-core platform \[8, 9, 13\] but they can easily be adopted and used in other designs implementing variants of the OCP interface standard. The OCPio module is used to connect a Patmos processor to a message passing network-on-chip and the OCPburst is used to connect the Processor and its cache controllers to a shared on-chip memory.

While the problem of synchronizing a simple streaming interface is well described in the literature and often solved using bi-synchronous FIFOs we found surprisingly little published material addressing synchronization of bus-style read-write transaction interfaces. An OCP interface typically has control signals related to both the master issuing a read or write request and the slave producing a response. If all these control signals are passed across the clock domain boundary and synchronized it may add significant latency to the duration of a transaction. Our interface designs avoid this and synchronize only a single signal transition in each direction during a read or a write transaction. The designs are available as open source, and the modules have been tested in a complete multi-core platform implemented on an FPGA board.

Reconfiguration in FPGA-Based Multi-Core Platforms for Hard Real-Time Applications

In general-purpose computing multi-core platforms, hardware accelerators and reconfiguration are means to improve performance; i.e., the average-case execution time of a software application. In hard real-time systems, such average-case speed-up is not in itself relevant - it is the worst-case execution-time of tasks of an application that determines the systems ability to respond in time. To support this focus, the platform must provide service guarantees for both communication and computation resources. In addition, many hard real-time applications have multiple modes of operation, and each mode has specific requirements. An interesting perspective on reconfigurable computing is to exploit run-time reconfiguration to support mode changes. In this paper we explore approaches to reconfiguration of
communication and computation resources in the T-CREST hard real-time multi-core platform. The reconfiguration of communication resources is supported by extending the message-passing network-on-chip with capabilities for setting up, tearing down, and modifying the bandwidth of virtual circuits. The reconfiguration of computation resources, such as hardware accelerators, is performed using the dynamic partial reconfiguration capabilities found in modern FPGAs.

State-based Communication on Time-predictable Multicore Processors
Some real-time systems use a form of task-to-task communication called state-based or sample-based communication that does not impose any flow control among the communicating tasks. The concept is similar to a shared variable, where a reader may read the same value multiple times or may not read a given value at all. This paper explores time-predictable implementations of state-based communication in network-on-chip based multicore platforms through five algorithms. With the presented analysis of the implemented algorithms, the communicating tasks of one core can be scheduled independently of tasks on other cores. Assuming a specific time-predictable multicore processor, we evaluate how the read and write primitives of the five algorithms contribute to the worst-case execution time of the communicating tasks. Each of the five algorithms has specific capabilities that make them suitable for different scenarios.

Time-Predictable Communication on a Time-Division Multiplexing Network-on-Chip Multicore
This thesis presents time-predictable inter-core communication on a multicore platform with a time-division multiplexing (TDM) network-on-chip (NoC) for hard real-time systems. The thesis is structured as a collection of papers that contribute within the areas of: reconfigurable TDM NoCs, static TDM scheduling, and time-predictable inter-core communication.

More specifically, the work presented in this thesis investigates the interaction between hardware and software involved in time-predictable inter-core communication on the multicore platform. The thesis presents: a new generation of the Argo NoC network interface (NI) that supports instantaneous reconfiguration, a TDM traffic scheduler that generates virtual...
circuit (VC) configurations for the Argo NoC, and software functions for two types of intercore communication.

The new generation of the Argo NoC adds the capability of instantaneously reconfiguring VCs and it addresses the identified shortcomings of the previous generation. The VCs provide the guaranteed bandwidth and latency required to implement time-predictable inter-core communication on top of the Argo NoC. This new Argo generation is, in terms of hardware, less than half the size of NoCs that provide similar functionalities and it offers a higher degree of flexibility to the application programmer.

The developed TDM scheduler supports a generic TDM NoC and custom parameterizable communication patterns. These communication patterns allow the application programmer to generate schedules that provide a set of VCs that efficiently uses the hardware resources. The TDM scheduler also shows better results, in terms of TDM period, compared to previous state-of-the-art TDM schedulers. Furthermore, we provide a description of how a communication pattern can be optimized in terms of shortening the TDM period.

The thesis identifies two types of inter-core communication that are commonly used in real-time systems: message passing and state-based communication. We implement message passing as a circular buffer with the data transfer through the NoC. The worst-case execution time (WCET) of the send and receive functions of our implementation is not dependent on the message size. We also implement five algorithms for state-based communication and analyze them in terms of the WCET and worst-case communication delay. The five algorithms each have scenarios where they are better than the others.

This thesis shows in detail how time-predictable inter-core communication can be implemented in an efficient way, from the low-level hardware to the high-level software functions.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Sørensen, R. B. (Intern), Sparsø, J. (Intern), Schoeberl, M. (Intern)
Number of pages: 143
Publication date: 2016

Publication information
Place of publication: Kgs. Lyngby
Publisher: Technical University of Denmark (DTU)
Original language: English
Series: DTU Compute PHD-2016
Number: 423
ISSN: 0909-3192
Main Research Area: Technical/natural sciences
Electronic versions:
phd423_Sorensen_RB.pdf

Relations
Projects:
Time-Predictable Communication on a Time-Division Multiplexing Network-on-Chip Multicore
Publication: Research › Ph.D. thesis – Annual report year: 2016

Time-predictable Stack Caching
Embedded systems are computing systems for controlling and interacting with physical environments. Embedded systems with special timing constraints where the system needs to meet deadlines are referred to as real-time systems. In hard real-time systems, missing a deadline causes the system to fail completely. Thus, in systems with hard deadlines the worst-case execution time (WCET) of the real-time software running on them needs to be bounded.

Modern architectures use features such as pipelining and caches for improving the average performance. These features, however, make the WCET analysis more complicated and less imprecise. Time-predictable computer architectures provide solutions to this problem. As accesses to the data in caches are one source of timing unpredictability, devising methods for improving the timepredictability of caches are important. Stack data, with statically analyzable addresses, provides an opportunity to predict and tighten the WCET of accesses to data in caches.

In this thesis, we introduce the time-predictable stack cache design and implementation within a time-predictable processor. We introduce several optimizations to our design for tightening the WCET while keeping the timepredictability of the design intact. Moreover, we provide a solution for reducing the cost of context switching in a system using the stack cache. In design of these caches, we use custom hardware and compiler support for delivering time-predictable stack data accesses. Furthermore, for systems where compiler support or hardware changes are not practical, we propose and explore two different alternatives based on only software and only hardware support.
An Asynchronous Time-Division-Multiplexed Network-on-Chip for Real-Time Systems

Multi-processor architectures using networks-on-chip (NOCs) for communication are becoming the standard approach in the development of embedded systems and general purpose platforms. Typically, multi-processor platforms follow a globally asynchronous locally synchronous (GALS) timing organization. This thesis focuses on the design of Argo, a NOC targeted at hard real-time multi-processor platforms with a GALS timing organization.

To support real-time communication, NOCs establish end-to-end connections and provide latency and throughput guarantees for these connections. Argo uses time division multiplexing (TDM) in combination with a static schedule to implement virtual end-to-end circuits. TDM is a straightforward way to provide guarantees and to share the resources efficiently, and it has an efficient hardware implementation. Argo supports a GALS system organization, and additionally it explores more flexible timing within its structure, to address signal distribution issues, using a network of synchronous routers.

NOCs consist of a switching structure of routers connected by links, with network interfaces (NIs) that connect the processors to the switching structure. Argo uses a novel NI design that supports time-predictability, and asynchronous routers that form a time-elastic network. The NI design integrates the DMA functionality and the TDM schedule, and uses dual-ported local memories. The routers combine the router functionality and asynchronous elastic behavior. They also use a gating mechanism to reduce the energy consumption. The combination of the NI design and the router design supports the formation of end-to-end paths in the NOC, from the local memory of a sending core to the local memory of a receiving core. These end-to-end paths do not require any dynamic arbitration, buffering, flow control, or clock synchronization, in the routers or the NIs.

This thesis explores the implementation of the individual components of Argo, as well as several complete instances of the Argo NOC. The implementations target both FPGA technology and 65 nm CMOS technology. It is shown that (i) the NI design is scalable and four to five times smaller than previously published NIs for similar NOCs, (ii) the router design is power efficient and two to three times smaller than equivalent router designs, and (iii) the overall Argo NOC is around four times smaller than other TDM NOCs. Argo is an important part of the T-CREST plattform and used in a number of configurations.

The flexible timing organization of Argo combines asynchronous routers with mesochronous NIs, which are connected to individually clocked cores, supporting a GALS system organization. The mesochronous NIs operate at the same frequency, possibly with some skew, while the network of asynchronous routers absorbs this skew within certain limits. The elasticity of the asynchronous network is explored, answering the question of how much skew the Argo NOC can absorb. A qualitative analysis studies the parameters affecting the elasticity and its limits. A quantitative analysis models the Argo behavior using timed-graph models and worstcase timing separation of events analysis to evaluate the elasticity of Argo. The results show that the skew absorbed by the network of routers can be two or more cycles, depending on the frequency applied at its endpoints, the NIs.

Overall this thesis presents the design and implementation of Argo, and the analysis of its elastic behavior. It shows that Argo provides hard real-time guarantees in a straightforward way, it has an efficient implementation and it is time-elastic.
Interfacing Hardware Accelerators to a Time-Division Multiplexing Network-on-Chip

This paper addresses the integration of stateless hardware accelerators into time-predictable multi-core platforms based on time-division multiplexing networks-on-chip. Stateless hardware accelerators, like floating-point units, are typically attached as co-processors to individual processors in the platform. Our design takes a different approach and connects the hardware accelerators to the network-on-chip in the same way as processor cores. Each processor that uses a hardware accelerator is assigned a virtual channel for sending instructions to the hardware accelerator and a virtual channel for receiving results. This allows a stateless and possibly pipelined hardware accelerator to be shared in an interleaved fashion without any form of reservation, and this opens for interesting area-performance trade-offs. The design is developed with a focus on time-predictability, areaefficiency, and FPGA implementation. The design evaluation is carried out using the open source T-CREST multi-core platform implemented on an Altera Cyclone IV FPGA. The size of the proposed design, including a floating-point accelerator, is about two-thirds of a processor.

Message Passing on a Time-predictable Multicore Processor

Real-time systems need time-predictable computing platforms. For a multicore processor to be time-predictable, communication between processor cores needs to be time-predictable as well. This paper presents a time-predictable message-passing library for such a platform. We show how to build up abstraction layers from a simple, time-division multiplexed hardware push channel. We develop these time-predictable abstractions and implement them in software. To prove the time-predictability of these functions we analyze their worst-case execution time (WCET) with the aiT WCET analysis tool. We combine these WCET numbers with the calculation of the network latency of a message and then provide a statically computed end-to-end latency for this core-to-core message.
Models of Communication for Multicore Processors

To efficiently use multicore processors we need to ensure that almost all data communication stays on chip, i.e., the bits moved between tasks executing on different processor cores do not leave the chip. Different forms of on-chip communication are supported by different hardware mechanisms, e.g., shared caches with cache coherency protocols, core-to-core networks-on-chip, and shared scratchpad memories. In this paper we explore the different hardware mechanisms for on-chip communication and how they support or favor different models of communication. Furthermore, we discuss the usability of the different models of communication for real-time systems.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Schoeberl, M. (Intern), Sørensen, R. B. (Intern), Sparsø, J. (Intern)
Pages: 44-51
Publication date: 2015

T-CREST: Time-predictable multi-core architecture for embedded systems

Real-time systems need time-predictable platforms to allow static analysis of the worst-case execution time (WCET). Standard multi-core processors are optimized for the average case and are hardly analyzable. Within the T-CREST project we propose novel solutions for time-predictable multi-core architectures that are optimized for the WCET instead of the average-case execution time. The resulting time-predictable resources (processors, interconnect, memory arbiter, and memory controller) and tools (compiler, WCET analysis) are designed to ease WCET analysis and to optimize WCET performance. Compared to other processors the WCET performance is outstanding. The T-CREST platform is evaluated with two industrial use cases. An application from the avionic domain demonstrates that tasks executing on different cores do not interfere with respect to their WCET. A signal processing application from the railway domain shows that the WCET can be reduced for computation-intensive tasks when distributing the tasks on several cores and using the network-on-chip for communication. With three cores the WCET is improved by a factor of 1.8 and with 15 cores by a factor of 5.7. The T-CREST project is the result of a collaborative research and development project executed by eight partners from academia and industry. The European Commission funded T-CREST.

General information
State: Published
Pages: 449-471
Publication date: 2015
Main Research Area: Technical/natural sciences
The Argo NOC: Combining TDM and GALS

Argo is a network-on-chip developed for use in a multi-core platform designed specifically for hard real-time applications and it supports message passing across virtual end-to-end channels. Argo implements these channels using time-division-
multiplexing (TDM) of the resources in the NOC following a static schedule. This requires some form of global synchrony across the platform. At the same time it is generally accepted that a large chip should employ some form of globally-asynchronous locally-synchronous (GALS) organization. By using asynchronous routers and by rethinking the microarchitecture of the network interfaces we have managed to combine TDM and GALS and obtain a very hardware-efficient implementation of the NOC. The paper gives a brief overview of the Argo NOC and focuses on two important issues: how to safely bring the NOC out of reset and timing analysis of the network of asynchronous routers.

### General information

**State:** Published  
**Organisations:** Embedded Systems Engineering, Department of Applied Mathematics and Computer Science  
**Authors:** Kasapaki, E. (Intern), Sparsø, J. (Intern)  
**Number of pages:** 4  
**Publication date:** 2015

### Host publication information

**Title of host publication:** Proceedings of the 22nd European Conference on Circuit Theory and Design (ECCTD 2015)  
**Publisher:** IEEE  
**ISBN (Print):** 978-1-4799-9877-7  
**BFI conference series:** European Conference on Circuit Theory and Design (5010330)  
**Main Research Area:** Technical/natural sciences  
**Conference:** 22nd European conference on circuit theory and design, Trondheim, Norway, 24/08/2015 - 24/08/2015  
**DOIs:** 10.1109/ECCTD.2015.7300101  
**Source:** FindIt  
**Source-ID:** 276537292  
**Publication:** Research - peer-review › Article in proceedings – Annual report year: 2015

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A Loosely Synchronizing Asynchronous Router for TDM-Scheduled NOCs

This paper presents an asynchronous router design for use in time-division-multiplexed (TDM) networks-on-chip. Unlike existing synchronous, mesochronous and asynchronous router designs with similar functionality, the router is able to silently skip over cycles/TDM-slots where no traffic is scheduled and hence avoid all switching activity in the idle links and router ports. In this way switching activity is reduced to the minimum possible amount. The fact that this relaxed synchronization is sufficient to implement TDM scheduling represents a contribution at the conceptual level. The idea can only be implemented using asynchronous circuit techniques. To this end, the paper explores the use of “click-element” templates. Click-element templates use only flipflops and conventional gates, and this greatly simplifies the design process when using conventional EDA tools and standard cell libraries. Few papers, if any, have explored this.

### General information

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**Pages:** 151-158  
**Publication date:** 2014

### Host publication information

**Title of host publication:** Proceedings of the 8th IEEE/ACM International Symposium on Networks-on-Chip (NOCS) 2014  
**Publisher:** IEEE  
**ISBN (Print):** 978-1-4799-5347-9  
**BFI conference series:** Networks-on-Chips (5000385)  
**Main Research Area:** Technical/natural sciences  
**DOIs:** 10.1109/NOCS.2014.7008774  
**Source:** PublicationPreSubmission  
**Source-ID:** 101067503  
**Publication:** Research - peer-review › Article in proceedings – Annual report year: 2014

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A Metaheuristic Scheduler for Time Division Multiplexed Network-on-Chip

This report presents a metaheuristic scheduler for inter-processor communication in multi-core platforms using time division multiplexed (TDM) networks on chip (NOC). Input to the scheduler is a specification of the target multi-core
platform and a specification of the application. Compared to previous works, the scheduler handles a broader and more
general class of platforms.

Another contribution, which has significant practical implications, is the minimization of the TDM schedule period by over-
provisioning bandwidth to connections with the smallest bandwidth requirements. Our results show that this is possible
with only negligible impact on the schedule period.

We evaluate the scheduler with seven different applications from the MCSL NOC benchmark suite. We observe that the
metaheuristics perform better than the greedy solution. In the special case of all-to-all communication with equal
bandwidths on all communication channels, we obtain schedules with a shorter period than reported in previous work.

A Metaheuristic Scheduler for Time Division Multiplexed Network-on-Chip
This paper presents a metaheuristic scheduler for inter-processor communication in multi-processor platforms using time
division multiplexed (TDM) networks on chip (NOC). Compared to previous works, the scheduler handles a broader and
more general class of platforms.

Another contribution, which has significant practical implications, is the minimization of the TDM schedule period by over-
provisioning bandwidth to connections with the smallest bandwidth requirements. Our results show that this is possible
with only negligible impact on the schedule period. We evaluate the scheduler with seven different applications from the
MCSL NOC benchmark suite. In the special case of all-to-all communication with equal bandwidths on all communication
channels, we obtain schedules with a shorter period than reported in previous work.
Argo: A Time-Elastic Time-Division-Multiplexed NOC using Asynchronous Routers
In this paper we explore the use of asynchronous routers in a time-division-multiplexed (TDM) network-on-chip (NOC), Argo, that is being developed for a multi-processor platform for hard real-time systems. TDM inherently requires a common time reference, and existing TDM-based NOC designs are either synchronous or mesochronous. We use asynchronous routers to achieve a simpler, smaller, and more robust, self-timed design. Our design exploits the fact that pipelined asynchronous circuits also behave as ripple FIFOs. Thus, it avoids the need for explicit synchronization FIFOs between the routers. Argo has interesting elastic timing properties that allow it to tolerate skew between the network interfaces (NIs).

The paper presents Argo NOC-architecture and provides a quantitative analysis of its ability of absorb skew between the NIs. Using a signal transition graph model and realistic component delays derived from a 65nm CMOS implementation, a worstcase analysis shows that a typical design can tolerate a skew of 1-5 cycles (depending on FIFO depths and NI clock frequency). Simulation results of a 2 x 2 NOC confirm this.

A Time-predictable Memory Network-on-Chip
To derive safe bounds on worst-case execution times (WCETs), all components of a computer system need to be time-predictable: the processor pipeline, the caches, the memory controller, and memory arbitration on a multicore processor. This paper presents a solution for time-predictable memory arbitration and access for chip-multiprocessors. The memory network-on-chip is organized as a tree with time-division multiplexing (TDM) of accesses to the shared memory. The TDM based arbitration completely decouples processor cores and allows WCET analysis of the memory accesses on individual cores without considering the tasks on the other cores. Furthermore, we perform local, distributed arbitration according to the global TDM schedule. This solution avoids a central arbiter and scales to a large number of processors.
Open Core Protocol (OCP) Clock Domain Crossing Interfaces

The open core protocol (OCP) is an openly licensed configurable and scalable interface protocol for on-chip subsystem communications. The protocol defines read and write transactions from a master towards a slave across a point-to-point connection and the protocol assumes a single common clock. This paper presents the design of two OCP clock domain crossing interface modules that can be used to construct systems with multiple clock domains. An OCP interface typically has control signals related to both the master issuing a read or write request and the slave producing a response. If all these control signals are passed across the clock-domain boundary and synchronized it may add significant latency to the duration of a transaction. Our interface designs avoid this and synchronize only a single signal transition in each direction during a read or a write transaction.

While the problem of synchronizing a simple streaming interface is well described in the literature and often solved using bi-synchronous FIFOs we found surprisingly little published material addressing synchronization of bus-style read-write transaction interfaces.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark
Authors: Herlev, M. (Ekstern), Poulsen, C. K. (Ekstern), Sparsø, J. (Intern)
Number of pages: 6
Publication date: 2014

Host publication information
Title of host publication: Proceedings of the 32th IEEE Norchip Conference 2014
Publisher: IEEE
Editors: Nurmi, J., Daniel, O., Liljeberg, P., Rahkonen, T., Nielsen, I. R.
ISBN (Print): 978-1-4799-6890-9
BFI conference series: NORCHIP (5010927)
Main Research Area: Technical/natural sciences
DOIs: 10.1109/NORCHIP.2014.7004739
Source: PublicationPreSubmission
Source-ID: 101067555
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

Synthesis and Layout of an Asynchronous Network-on-Chip using Standard EDA Tools
Asynchronous circuit design is well understood but design tools supporting asynchronous design are largely lacking, and designers are limited to using conventional EDA-tools. These tools have a built-in synchronous mind-set and this complicates their use for asynchronous implementation. One example is the key role that clock signals play in specifying time-constraints for the synthesis. In this paper explain how we handled the synthesis and layout of an asynchronous network-on-chip for a multi-core platform. Focus is on the design process while the actual NOC-design and its performance are presented elsewhere.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Müller, C. (Intern), Kasapaki, E. (Intern), Sørensen, R. B. (Intern), Sparsø, J. (Intern)
Number of pages: 6
A 65-nm CMOS Area Optimized De-synchronization Flow for sub-VT Designs

This paper proposes a process independent post layout de-synchronization flow implemented in tool command language working on designs operating in the sub-VT regime. The overhead due to the self-timed operation is combated by introducing full-custom delay elements and latches for a standard 65-nm CMOS process. The flow offers the possibility to adjust granularity based on user requirements. Case studies with different reference designs manifested an average reduction of area and power overhead from 105% to 9% and 174% to 58% in comparison to a full standard cell de-synchronization approach.

An area-efficient network interface for a TDM-based Network-on-Chip

Network interfaces (NIs) are used in multi-core systems where they connect processors, memories, and other IP-cores to a packet switched Network-on-Chip (NOC). The functionality of a NI is to bridge between the read/write transaction interfaces used by the cores and the packet-streaming interface used by the routers and links in the NOC. The paper addresses the design of a NI for a NOC that uses time division multiplexing (TDM). By keeping the essence of TDM in mind, we have developed a new area-efficient NI micro-architecture. The new design completely eliminates the need for FIFO buffers and credit based flow control - resources which are reported to account for 50–85% of the area in existing NI designs. The paper discusses the design considerations, presents the new NI micro-architecture, and reports area figures for a range of implementations.
Router Designs for an Asynchronous Time-Division-Multiplexed Network-on-Chip

In this paper we explore the design of an asynchronous router for a time-division-multiplexed (TDM) network-on-chip (NOC) that is being developed for a multi-processor platform for hard real-time systems. TDM inherently requires a common time reference, and existing TDM-based NOC designs are either synchronous or mesochronous, but both approaches have their limitations: a globally synchronous NOC is no longer feasible in today's sub micron technologies and a mesochronous NOC requires special FIFO-based synchronizers in all input ports of all routers in order to accommodate for clock phase differences. This adds hardware complexity and increases area and power consumption. We propose to use asynchronous routers in order to achieve a simpler, more robust and globally-asynchronous NOC, and this represents an unexplored point in the design space. The paper presents a range of alternative router designs. All routers have been synthesized for a 65nm CMOS technology, and the paper reports post-layout figures for area, speed and energy and compares the asynchronous designs with an existing mesochronous clocked router. The results show that an asynchronous router is 2 times smaller, marginally slower and with roughly the same energy consumption, while offering a robust solution to the clock distribution problem. The paper further explores "clock-gating" of the individual pipeline stages in the asynchronous routers, and shows that this can lead to significant power savings.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Eindhoven University of Technology
Authors: Kasapaki, E. (Intern), Sparsø, J. (Intern), Sørensen, R. B. (Intern), Goossens, K. (Ekstern)
Pages: 319-326
Publication date: 2013

A Light-Weight Statically Scheduled Network-on-Chip

This paper investigates how a light-weight, statically scheduled network-on-chip (NoC) for real-time systems can be designed and implemented. The NoC provides communication channels between all cores with equal bandwidth and latency. The design is FPGA-friendly and consumes a minimum of resources. We implemented a 64 core 16-bit multiprocessor connected with the proposed NoC in a low-cost FPGA.

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Embedded Systems Engineering, Computer Science and Engineering
Authors: Sørensen, R. B. (Intern), Schoeberl, M. (Intern), Sparsø, J. (Intern)
Number of pages: 6
Publication date: 2012
A Statically Scheduled Time-Division-Multiplexed Network-on-Chip for Real-Time Systems

This paper explores the design of a circuit-switched network-on-chip (NoC) based on time-division-multiplexing (TDM) for use in hard real-time systems. Previous work has primarily considered application-specific systems. The work presented here targets general-purpose hardware platforms. We consider a system with IP-cores, where the TDM-NoC must provide directed virtual circuits - all with the same bandwidth - between all nodes. This may not be a frequent scenario, but a general platform should provide this capability, and it is an interesting point in the design space to study. The paper presents an FPGA-friendly hardware design, which is simple, fast, and consumes minimal resources. Furthermore, an algorithm to find minimum-period schedules for all-to-all virtual circuits on top of typical physical NoC topologies like 2D-mesh, torus, bidirectional torus, tree, and fat-tree is presented. The static schedule makes the NoC time-predictable and enables worst-case execution time analysis of communicating real-time tasks.

Design of Networks-on-Chip for Real-Time Multi-Processor Systems-on-Chip

This paper addresses the design of networks-on-chips for use in multi-processor systems-on-chips - the hardware platforms used in embedded systems. These platforms typically have to guarantee real-time properties, and as the network is a shared resource, it has to provide service guarantees (bandwidth and/or latency) to different communication flows. The paper reviews some past work in this field and the lessons learned, and the paper discusses ongoing research conducted as part of the project "Time-predictable Multi-Core Architecture for Embedded Systems" (T-CREST), supported by the European Commissions seventh framework programme. The aim of this project is to develop a general-purpose multi-core platform for real-time systems as well as tools supporting its use (compiler, simulator, and worst-case execution time analysis tool).
IR-Drop Reduction in Sub-VT Circuits by De-synchronization

This paper proposes IR-drop reduction of sub-VT circuits by de-synchronization. The de-synchronization concept is briefly demonstrated and analyzed by a case study. Extensive IR-drop analysis of various technology options of a 65nm CMOS family demonstrate how the noise margins are reduced due to switching noise on the supply rails. It is shown that a desynchronized implementation reduces severe voltage drops on the supply rails by approximately 50%, compared to a clocked design.

Analytical derivation of traffic patterns in cache-coherent shared-memory systems

This paper presents an analytical method to derive the worst-case traffic pattern caused by a task graph mapped to a cache-coherent shared-memory system. Our analysis allows designers to rapidly evaluate the impact of different mappings of tasks to IP cores on the traffic pattern. The accuracy varies with the application's data sharing pattern, and is around 65% in the average case and 1% in the best case when considering the traffic pattern as a whole. For individual connections, our method produces tight worst-case bandwidths.
CDIO Projects in DTU's B.Eng. in IT Study Program

Since the fall 2008 all B.Eng. study programs at the Technical University of Denmark have been based on the CDIO concept. The adoption of the CDIO standards and principles resulted in new or significantly revised study programs. As part of this effort design-build projects have been introduced on each of the first 4 semesters, and each semester-project spans several courses. The aim of this paper is to describe the four CDIO semester projects in the B.Eng. in IT study, and – along with similar papers describing the other six B.Eng. programs – to provide documentation to accompany an exposition with stands providing additional information and with students demonstrating their projects. The paper is narrowly focused on the IT-study program. At the time of writing this paper the students enrolled in 2008 have completed all four semesters in the new CDIO-based study plan, and the students enrolled in 2009 are currently in the process of finishing the 4th semester. Consequently, the paper is reporting on curriculum development which has been implemented,
and for which experiences have gained.

**General information**

State: Published

Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling, Algorithms and Logic, Software Engineering, Language-Based Technology


Publication date: 2011

**Host publication information**

Title of host publication: Proceedings of the 7th International CDIO Conference, Technical University of Denmark, Copenhagen, June 20 - 23, 2011

Place of publication: Lyngby

Publisher: Technical University of Denmark (DTU)

Main Research Area: Technical/natural sciences

Conference: 7th International CDIO Conference, Copenhagen, Denmark, 20/06/2011 - 20/06/2011

Electronic versions:

FB15Ad01.pdf

DOIs:

10.4122/1.1000054694

Links:

http://www.cdio2011.dtu.dk/

Source: orbit

Source-ID: 279914

Publication: Research - peer-review › Article in proceedings – Annual report year: 2011

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**Energy-minimum sub-threshold self-timed circuits using current-sensing completion detection**

This study addresses the design of self-timed energy-minimum circuits, operating in the sub-VT domain and a generic implementation template using bundled-data circuitry and current sensing completion detection (CSCD). Furthermore, a fully decoupled latch controller was developed, which integrates with the current-sensing circuitry. Different configurations that utilise the proposed latch controller are highlighted. A contemporary synchronous electronic design automation tools-based design flow, which transforms a synchronous design into a corresponding self-timed circuit, is outlined. Different use cases of the CSCD system are examined. The design flow and the current-sensing technique are validated by the implementation of a self-timed version of a wavelet-based event detector for cardiac pacemaker applications in a standard 65 nm CMOS process. The chip was fabricated and verified to operate down to 250 mV. Spice simulations indicate a gain of 52.58% in throughput because of asynchronous operation. By trading the throughput improvement, energy dissipation is reduced by 16.8% at the energy-minimum supply voltage.

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**General information**

State: Published

Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling, Lund University

Authors: Akgun, O. C. (Ekstern), Rodrigues, J. N. (Ekstern), Sparsø, J. (Intern)

Pages: 342-353

Publication date: 2011

Main Research Area: Technical/natural sciences

**Publication information**

Journal: I E T Computers and Digital Techniques

Volume: 5

Issue number: 4

ISSN (Print): 1751-8601

Ratings:

BFI (2018): BFI-level 1

Web of Science (2018): Indexed yes

BFI (2017): BFI-level 1

Web of Science (2017): Indexed Yes

BFI (2016): BFI-level 1

Scopus rating (2016): SJR 0.21 SNIP 0.722 CiteScore 1.06

BFI (2015): BFI-level 1

Scopus rating (2015): SJR 0.229 SNIP 0.515 CiteScore 0.82

BFI (2014): BFI-level 1
The ReNoC Reconfigurable Network-on-Chip: Architecture, Configuration Algorithms, and Evaluation

This article presents a reconfigurable network-on-chip architecture called ReNoC, which is intended for use in general-purpose multiprocessor system-on-chip platforms, and which enables application-specific logical NoC topologies to be configured, thus providing both efficiency and flexibility. The article presents three novel algorithms that synthesize an application-specific NoC topology, map it onto the physical ReNoC architecture, and create deadlock-free, application-specific routing algorithms. We apply our algorithms to a mixture of real and synthetic applications and target three different physical architectures. Compared to a conventional NoC, ReNoC reduces power consumption by up to 58% on average.

General information

State: Published
Organisations: Biomedical Engineering, Department of Electrical Engineering, Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Stuart, M. B. (Intern), Stensgaard, M. B. (Intern), Sparsø, J. (Intern)
Pages: 45:1-45:26
Publication date: 2011
Main Research Area: Technical/natural sciences

Publication information

Journal: A C M Transactions on Embedded Computing Systems
Volume: 10
Issue number: 4
ISSN (Print): 1539-9087
Support for Programming Models in Network-on-Chip-based Many-core Systems
This thesis addresses aspects of support for programming models in Network-on-Chip-based many-core architectures. The main focus is to consider architectural support for a plethora of programming models in a single system. The thesis has three main parts. The first part considers parallelization and scalability in an image processing application with the aim of providing insight into parallel programming issues. The second part proposes and presents the tile-based Clupea many-core architecture, which has the objective of providing configurable support for programming models to allow different programming models to be supported by a single architecture. The architecture features a specialized network interface processor which allows extensive configurability of the memory system. Based on this architecture, a detailed implementation of the cache coherent shared memory programming model is presented. The third part considers modeling and evaluation of the Clupea architecture configured for support for cache coherent shared memory. An analytical model and the MC sim simulator, which provides detailed cycle-accurate simulation of many-core architectures, have been developed for the evaluation of the Clupea architecture. The evaluation shows that configurability causes a moderate increase of the application execution time. Considering the improved flexibility, this impact is considered acceptable as the architecture can potentially exploit application-specific optimizations and offers a valuable platform for comparing programming models.

General information
State: Published
Modelling, Synthesis, and Configuration of Networks-on-Chips

This thesis presents three contributions in two different areas of network-on-chip and system-on-chip research: Application modelling and identifying and solving different optimization problems related to two specific network-on-chip architectures. The contribution related to application modelling is an analytical method for deriving the worst-case traffic pattern caused by an application and the cache-coherence protocol in a cache-coherent shared-memory system. The contributions related to network-on-chip optimization problems consist of two parts: The development and evaluation of six heuristics for solving the network synthesis problem in the MANGO network-on-chip, and the identification and formalization of the ReNoC configuration problem together with three heuristics for solving it.

Minimum-Energy Sub-Threshold Self-Timed Circuits: Design Methodology and a Case Study

This paper addresses the design of self-timed energy-minimum circuits, operating in the sub-VT domain. The paper presents a generic implementation template using bundled-data circuitry and current sensing completion detection. To support this, a fully-decoupled latch controller has been developed, which integrates the current sensing circuitry. The paper outlines a corresponding design flow, which is based on contemporary synchronous EDA tools, and which transforms a synchronous design into a corresponding self-timed circuit. The design flow and the current-sensing technique is validated by the implementation of an asynchronous version of a wavelet based event detector for cardiac pacemaker applications in a standard 65nm CMOS process. The chip has been fabricated and the area overhead due to power domain separation and completion detection circuitry is 13.6 %. The improvement in throughput due to asynchronous operation is 52.58 %. By trading the throughput improvement, energy dissipation is reduced by 16.8% at the energy-minimum supply voltage.
A Behavioral Synthesis Frontend to the Haste/TiDE Design Flow

This paper presents a complete design tool which performs automatic behavioral synthesis of asynchronous circuits (resource sharing, scheduling and binding). The tool targets a traditional control-datapath-style template architecture. Within the limitations set by this template architecture it is possible to optimize for area (which is our main focus) or for speed. This is done by simply using different cost functions. Input to the tool is a behavioral description in the Haste language, and output from the tool is a Haste program describing the synthesized implementation consisting of a datapath and a controller. The tool may be seen as an add-on to the Haste/TiDE tool flow, and it can be used to automatically optimize parts of a design and to quickly explore alternative optimizations. The paper outlines the design flow, explains key elements of the design tool, and presents a number of benchmark results.
Analytical Derivation of Traffic Patterns in Shared Memory Architectures from Task Graphs

Task Graphs is a commonly used application model in research in computer-aided design tools for design space exploration of embedded systems, including system synthesis, scheduling and application mapping. These design tools need an estimate of the actual communication in the target system caused by the application modelled by the task graph. In this paper, we present a method for analytically deriving the worst-case traffic pattern when a task graph is mapped to a multiprocessor system-on-chip with a shared memory architecture. We describe the additionally needed information besides the dependencies in the task graph in order to derive the traffic pattern. Finally, we construct a simulator that we use to find the actual traffic pattern in a system and compare this to the derived pattern. Results show that our worst-case derivation overestimates the bandwidth by 9% for systems with small caches and between 32% and 52% for systems with large caches.

Behavioral Synthesis of Asynchronous Circuits Using Syntax Directed Translation as Backend

The current state-of-the art in high-level synthesis of asynchronous circuits is syntax directed translation, which performs a one-to-one mapping of a HDL-description into a corresponding circuit. This paper presents a method for behavioral synthesis of asynchronous circuits which builds on top of syntax directed translation, and which allows the designer to perform automatic design space exploration guided by area or speed constraints. The paper presents an asynchronous implementation template consisting of a data-path and a control unit and its implementation using the asynchronous hardware description language Balsa [1]. This "conventional" template architecture allows us to adapt traditional synchronous synthesis techniques for resource sharing, scheduling, binding etc, to the domain of asynchronous circuits. A prototype tool has been implemented on top of the Balsa framework, and the method is illustrated through the implementation of a set of example circuits. The main contributions of the paper are: the fundamental idea, the template architecture and its implementation using asynchronous handshake components, and the implementation of a prototype tool.
COMPARISON AND CLASSIFICATION OF DESIGN BUILD PROJECTS IN DIFFERENT ENGINEERING BACHELOR PROGRAMS

General information
State: Published
Organisations: Section for Building Design, Department of Civil Engineering, Computer Aided Process Engineering Center, Department of Chemical and Biochemical Engineering, Department of Electrical Engineering, Department of Mechanical Engineering, Department of Informatics and Mathematical Modeling
Authors: Vigild, M. E. (Intern), Willumsen, L. E. (Intern), Borchersen, E. (Intern), Clement, K. (Intern), Bjerregaard Jensen, L. (Intern), Kjærgaard, C. (Intern), Kliit, P. (Intern), Sparsø, J. (Intern)
Pages: 1-7
Publication date: 2009

Host publication information
Title of host publication: COMPARISON AND CLASSIFICATION OF DESIGN BUILD PROJECTS IN DIFFERENT ENGINEERING BACHELOR PROGRAMS
Place of publication: Singapore
Publisher: Proceedings of the 5th International CDIO Conference, Singapore Polytechnic, Singapore, June 7 - 10, 2009
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 255337
Publication: Research - peer-review › Article in proceedings – Annual report year: 2009

Current Trends in High-Level Synthesis of Asynchronous Circuits
This paper is a survey paper presenting what the author sees as two major and promising trends in the current research in CAD-tools and design-methods for asynchronous circuits. One branch of research builds on top of existing asynchronous CAD-tools that perform syntax directed translation, e.g., the Haste/TiDE tool from Handshake Solutions or the Balsa tool from the University of Manchester. The aims are to add high-level synthesis capabilities to these tools and to extend the tools such that a wider range of (higher speed) micro-architectures can be generated. Another branch of research takes a conventional synchronous circuit as the starting point, and then adds some form of handshake-based flow-control. One approach keeps the global clock and implements discrete-time asynchronous operation. Another approach substitutes the clocked registers by asynchronous handshake-registers, thus creating truly continuous time asynchronous circuits that operate without a clock. The perspective here is that the substitution/conversion is done as the final step in an otherwise conventional synchronous design flow.

General information
State: Published
Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling
Authors: Sparsø, J. (Intern)
Pages: 347-350
Publication date: 2009

Host publication information
Title of host publication: 16th IEEE International Conference on Electronics Circuits and Systems (ICECS)
Publisher: IEEE
ISBN (Print): 978-1-4244-5091-6
Main Research Area: Technical/natural sciences
Electronic versions:
Sparsø.pdf
DOIs:
10.1109/ICECS.2009.5411011

Bibliographical note
Copyright 2009 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.
Source: orbit
Source-ID: 255585
Publication: Research - peer-review › Article in proceedings – Annual report year: 2009
Performance Analysis of a Hardware/Software-based Cache Coherence Protocol in Shared Memory MPSoCs

General information
State: Published
Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling
Authors: Rasmussen, M. S. (Intern), Karlsson, S. (Intern), Sparsø, J. (Intern)
Publication date: 2009

Host publication information
Title of host publication: Workshop on Programming Models for Emerging Architectures
Main Research Area: Technical/natural sciences
Conference: Workshop on Programming Models for Emerging Architectures, 01/01/2009
Source: orbit
Source-ID: 252061
Publication: Research - peer-review › Article in proceedings – Annual report year: 2009

Synthesis of Topology Configurations and Deadlock Free Routing Algorithms for ReNoC-based Systems-on-Chip

General information
State: Published
Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling
Authors: Stuart, M. B. (Intern), Stensgaard, M. B. (Intern), Sparsø, J. (Intern)
Publication date: 2009

Host publication information
Title of host publication: International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 252060
Publication: Research - peer-review › Article in proceedings – Annual report year: 2009

A Reactive and Cycle-True IP Emulator for MPSoC Exploration

The design of MultiProcessor Systems-on-Chip (MPSoC) emphasizes intellectual-property (IP)-based communication-centric approaches. Therefore, for the optimization of the MPSoC interconnect, the designer must develop traffic models that realistically capture the application behavior as executing on the IP core. In this paper, we introduce a Reactive IP Emulator (RIPE) that enables an effective emulation of the IP-core behavior in multiple environments, including bit and cycle-true simulation. The RIPE is built as a multithreaded abstract instruction-set processor, and it can generate reactive traffic patterns. We compare the RIPE models with cycle-true functional simulation of complex application behavior (tasksynchronization, multitasking, and input/output operations). Our results demonstrate high-accuracy and significant speedups. Furthermore, via a case study, we show the potential use of the RIPE in a design-space-exploration context.

A Reactive and Cycle-True IP Emulator for MPSoC Exploration

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling, System-on-Chip Hardware, Embedded Systems Engineering
Authors: Mahadevan, S. (Intern), Angiolini, F. (Ekstern), Sparsø, J. (Intern), Benini, L. (Ekstern), Madsen, J. (Intern)
Pages: 109-122
Publication date: 2008
Main Research Area: Technical/natural sciences

Publication information
Volume: 27
Issue number: 1
ISSN (Print): 0278-0070
Ratings:
BFI (2018): BFI-level 1
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 1
Web of Science (2017): Indexed yes
BFI (2016): BFI-level 1
Scopus rating (2016): CiteScore 2.72 SJR 0.486 SNIP 1.816
Web of Science (2016): Indexed yes
BFI (2015): BFI-level 1
Scopus rating (2015): SJR 0.619 SNIP 1.658 CiteScore 2.41
BFI (2014): BFI-level 1
Scopus rating (2014): SJR 0.598 SNIP 1.915 CiteScore 2.18
BFI (2013): BFI-level 1
Scopus rating (2013): SJR 0.665 SNIP 1.853 CiteScore 2.27
ISI indexed (2013): ISI indexed yes
Web of Science (2013): Indexed yes
BFI (2012): BFI-level 1
Scopus rating (2012): SJR 0.65 SNIP 1.513 CiteScore 1.88
ISI indexed (2012): ISI indexed yes
BFI (2011): BFI-level 2
Scopus rating (2011): SJR 0.784 SNIP 1.595 CiteScore 2.08
ISI indexed (2011): ISI indexed yes
BFI (2010): BFI-level 2
Scopus rating (2010): SJR 0.775 SNIP 1.441
BFI (2009): BFI-level 1
Scopus rating (2009): SJR 0.878 SNIP 1.693
BFI (2008): BFI-level 2
Scopus rating (2008): SJR 0.889 SNIP 1.614
Web of Science (2008): Indexed yes
Scopus rating (2007): SJR 0.861 SNIP 1.765
Scopus rating (2006): SJR 0.847 SNIP 1.968
Web of Science (2006): Indexed yes
Scopus rating (2005): SJR 1.096 SNIP 2.096
Scopus rating (2004): SJR 0.86 SNIP 1.868
Scopus rating (2003): SJR 1.695 SNIP 2.002
Scopus rating (2002): SJR 1.56 SNIP 2.094
Scopus rating (2001): SJR 1.139 SNIP 1.559
Scopus rating (2000): SJR 0.331 SNIP 1.859
Scopus rating (1999): SJR 0.263 SNIP 1.375
Original language: English
Network traffic reproduction, Traffic profiling and trace parsing, Simulation, Traffic generator, Bus traffic modelling, Traffic shaping, Systems-on-chip, Cycle-true traffic generator, Reactive application models, Multi Processor Systems-on-Chip (MPSoC), Simple instruction set architecture, Macromodelling, Multi-processing, Network-on-chip
Electronic versions:
Mahadevan.pdf
DOIs:
10.1109/TCAD.2007.906990

Bibliographical note
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Source: orbit
Source-ID: 208476
Publication: Research - peer-review › Journal article – Annual report year: 2008

E-learning support for student's understanding of electronics
To enhance active learning and understanding of analogue and digital electronics the use of e-learning techniques will be investigated. In a redesigned course combining introductory analogue and digital electronics, students will be motivated to prepare for lectures and exercises by providing access to interactive simulations. Some exercises will furthermore be carried out first as simulations of electrical circuits and then with physical components, i.e. as design-build exercises. A number of didactic problems in learning electricity and electronics are discussed.
Network Traffic Generator Model for Fast Network-on-Chip Simulation

For Systems-on-Chip (SoCs) development, a predominant part of the design time is the simulation time. Performance evaluation and design space exploration of such systems in bit- and cycle-true fashion is becoming prohibitive. We propose a traffic generation (TG) model that provides a fast and effective Network-on-Chip (NoC) development and debugging environment. By capturing the type and the timestamp of communication events at the boundary of an IP core in a reference environment, the TG can subsequently emulate the core's communication behavior in different environments. Access patterns and resource contention in a system are dependent on the interconnect architecture, and our TG is designed to capture the resulting reactivity. The regenerated traffic, which represents a realistic workload, can thus be used to undertake faster architectural exploration of interconnection alternatives, effectively decoupling simulation of IP cores and of interconnect fabrics. The results with the TG on an AMBA interconnect show a simulation time speedup above a factor of 2 over a complete system simulation, with close to 100% accuracy.

ReNoC: A Network-on-Chip Architecture with Reconfigurable Topology

This paper presents a Network-on-Chip (NoC) architecture that enables the network topology to be reconfigured. The architecture thus enables a generalized System-on-Chip (SoC) platform in which the topology can be customized for the application that is currently running on the chip, including long links and direct links between IP-blocks. The configurability is inserted as a layer between routers and links, and the architecture can therefore be used in combination with existing NoC routers, making it a general architecture. The topology is configured using energy-efficient topology switches based on physical circuit switching as found in FPGAs. The paper presents the ReNoC (Reconfigurable NoC) architecture and evaluates its potential. The evaluation design shows a 56% decrease in power consumption compared to a static 2D mesh topology.
A Scalable, Timing-Safe, Network-on-Chip Architecture with an Integrated Clock Distribution Method

Growing system sizes together with increasing performance variability are making globally synchronous operation hard to realize. Mesochronous clocking constitutes a possible solution to the problems faced. The most fundamental of problems faced when communicating between mesochronously clocked regions concerns the possibility of data corruption caused by metastability. This paper presents an integrated communication and mesochronous clocking strategy, which avoids timing related errors while maintaining a globally synchronous system perspective. The architecture is scalable as timing integrity is based purely on local observations. It is demonstrated with a 90 nm CMOS standard cell network-on-chip design which implements completely timing-safe, global communication in a modular system.

Asynchronous design of Networks-on-Chip

The Network-on-chip concept has evolved as a solution to a broad range of problems related to the design of complex systems-on-chip (SoC) with tens or hundreds of (heterogeneous) IP-cores. The paper introduces the NoC concept, identifies a range of possible timing organizations (globally-synchronous, mesochronous, globally-asynchronous locally-synchronous and fully asynchronous), discusses the circuitry needed to implement these timing methodologies, and provides some implementation details for a couple of asynchronous NoCs designed at the Technical University of Denmark (DTU). The paper is written to support an invited talk at the NORCHIP’2007 conference.

General information

State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Bjerregaard, T. (Intern), Stensgaard, M. B. (Intern), Sparsø, J. (Intern)
Pages: 1-6
Publication date: 2007
A Traffic injection methodology with support for system-level synchronization

This paper compares simulated annealing and tabu search for generating custom topologies for applications with periodic behaviour executing on a network-on-chip. The approach differs from previous work by starting from a fixed mapping of IP-cores to routers and performing design space exploration around an initial topology. The tabu search has been modified from its normally encountered form to allow easier escaping from local minima. A number of synthetic benchmarks are used for tuning the parameters of both heuristics and for testing the quality of the solutions each heuristic produces. An analytical model is used to determine communication latencies in the network-on-chip.

Custom Topology Generation for Network-on-Chip

This paper compares simulated annealing and tabu search for generating custom topologies for applications with periodic behaviour executing on a network-on-chip. The approach differs from previous work by starting from a fixed mapping of IP-cores to routers and performing design space exploration around an initial topology. The tabu search has been modified from its normally encountered form to allow easier escaping from local minima. A number of synthetic benchmarks are used for tuning the parameters of both heuristics and for testing the quality of the solutions each heuristic produces. An analytical model is used to determine communication latencies in the network-on-chip.
Towards CDIO-based B.Eng. studies at the Technical University of Denmark

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling, Solid Mechanics, Department of Mechanical Engineering, LearningLab DTU, Technical Information Center of Denmark, The Danish Polymer Centre, Department of Chemical and Biochemical Engineering
Authors: Sparsø, J. (Intern), Klit, P. (Intern), May, M. (Intern), Mohr, G. (Intern), Vigild, M. E. (Intern)
Publication date: 2007

Host publication information
Title of host publication: Proceedings of the 3rd International CDIO Conference
Main Research Area: Technical/natural sciences
Links: http://www2.imm.dtu.dk/pubdb/views/publication_details.php?id=5460
Source: orbit
Source-ID: 203167
Publication: Research - peer-review › Article in proceedings – Annual report year: 2007

Simulation-based Modeling Frameworks for Networked Multi-processor System-on-Chip
This thesis deals with modeling aspects of multi-processor system-on-chip (MpSoC) design affected by the on-chip interconnect, also called the Network-on-Chip (NoC), at various levels of abstraction. To begin with, we undertook a comprehensive survey of research and design practices of networked MpSoC. The survey presents the challenges of modeling and performance analysis of the hardware and the software components used in such devices. These challenges are further exasperated in a mixed abstraction workspace, which is typical of complex MpSoC design environment. We provide two simulation-based frameworks: namely ARTS and RIPE, that allows to model hardware (computation time, power consumption, network latency, caching effect, etc.) and software (application partition and mapping, operating system scheduling, interrupt handling, etc.) aspects from system-level to cycle-true abstraction. Thereby, we can realistically model the application executing on the architecture. This includes e.g. accurate modeling of synchronization, cache refills, context switching effects, so on, which are critically dependent on the architecture and the performance of the NoC. The foundation of the ARTS model is abstract tasks, while the foundation of the RIPE model is cycle-count. For ARTS, using different case-studies with over one hundred tasks (five applications) from the mobile multimedia domain, we show the potential of the framework under real-time constraints. For RIPE, first using six applications we derive the requirements to model the application and the architecture properties independent of the NoC, and then use these applications to successfully validate the approach against a reference cycle-true system. The presence of a standard socket at the intellectual property (IP) and the NoC interface in both the ARTS and the RIPE frameworks allows easy incorporation of IP cores from either frameworks, into a new instance of the design. This could pave the way for seamless design evaluation from system-level to cycle-true abstraction in future component-based MpSoC design practice.

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling, System-on-Chip Hardware, Embedded Systems Engineering
Authors: Mahadevan, S. (Intern), Sparsø, J. (Intern), Madsen, J. (Intern)
Publication date: Apr 2006

Publication information
Original language: English
Series: IMM-PHD-2006-157
Main Research Area: Technical/natural sciences
The MANGO clockless network-on-chip: Concepts and Implementation

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, System-on-Chip Hardware
Authors: Bjerregaard, T. (Intern), Sparsø, J. (Intern)
Publication date: Feb 2006

Publication information
Original language: English
Series: IMM-PHD-2005-153
Main Research Area: Technical/natural sciences
Electronic versions:
imm4548.pdf
Source: orbit
Source-ID: 191706
Publication: Research › Ph.D. thesis – Annual report year: 2006

A simple clockless Network-on-Chip for a commercial audio DSP chip

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Stensgaard, M. B. (Intern), Bjerregaard, T. (Intern), Sparsø, J. (Intern), Pedersen, J. H. (Ekstern)
Publication date: 2006

Host publication information
Title of host publication: Euromicro Conference on Digital System Design: Architectures, Methods and Tools
Publisher: IEEE
ISBN (Print): 0-7695-2609-8
Main Research Area: Technical/natural sciences
application, asynchronous, System-on-Chip, on-chip network, Network-on-Chip, clockless
Electronic versions:
Stensgaard.pdf
DOIs:
10.1109/DSD.2006.17

Bibliographical note
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Source: orbit
Source-ID: 191577
Publication: Research - peer-review › Article in proceedings – Annual report year: 2006

Implementation of Guaranteed Services in the MANGO Clockless Network-on-Chip

Shared, segmented, on-chip interconnection networks, known as networks-on-chip (NoC), may become the preferred way of interconnecting intellectual property (IP) cores in future giga-scale system-on-chip (SoC) designs. A NoC can provide the required communication bandwidth while accommodating the effects of scaling microchip technologies. Equally important, a NoC facilitates a truly modular and scalable design flow. The MANGO (message-passing asynchronous network-on-chip providing guaranteed services over open core protocol (OCP) interfaces) NoC is presented, and how its key characteristics (clockless implementation, standard socket access points, and guaranteed communication services) make MANGO suitable for a modular SoC design flow is explained. Among the advantages of using clockless circuit techniques are inherent global timing closure, low forward latency in pipelines, and zero dynamic idle power consumption. Time division multiplexing, generally used to provide bandwidth guarantees in clocked NoCs, however, is not possible in a clockless environment. MANGO provides an alternative, high-performance solution to providing hard, connection-oriented
service guarantees, using clockless circuit techniques. In-depth circuit details are presented, and the 0.13 /spl mu/m
standard cell implementation of a 5/spl times/5 routing node, for use in a mesh type NoC, is described.

Packetizing OCP Transactions in the MANGO Network-on-Chip
The scaling of CMOS technology causes a widening gap between the performance of on-chip communication and
computation. This calls for a communication-centric design flow. The MANGO network-on-chip architecture enables
globally asynchronous locally synchronous (GALS) system-on-chip design, while facilitating IP reuse by standard socket
access points. Two types of services are available: connection-less best-effort routing and connection-oriented guaranteed
service (GS) routing. This paper presents the core-centric programming model for establishing and using GS connections
in MANGO. We show how OCP transactions are packetized and transmitted across the shared network, and illustrate how
this affects the end-to-end performance. A high predictability of the latency of communication on shared links is shown in a
MANGO-based demonstrator system.
A Network Traffic Generator Model for Fast Network-on-Chip Simulation

For Systems-on-Chip (SoCs) development, a predominant part of the design time is the simulation time. Performance evaluation and design space exploration of such systems in bit- and cycle-true fashion is becoming prohibitive. We propose a traffic generation (TG) model that provides a fast and effective Network-on-Chip (NoC) development and debugging environment. By capturing the type and the timestamp of communication events at the boundary of an IP core in a reference environment, the TG can subsequently emulate the core's communication behavior in different environments. Access patterns and resource contention in a system are dependent on the interconnect architecture, and our TG is designed to capture the resulting reactivity. The regenerated traffic, which represents a realistic workload, can thus be used to undertake faster architectural exploration of interconnection alternatives, effectively decoupling...
simulation of IP cores and of interconnect fabrics. The results with the TG on an AMBA interconnect show a simulation
time speedup above a factor of 2 over a complete system simulation, with close to 100% accuracy.

**General information**
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Mahadevan, S. (Intern), Angiolini, F. (Ekstern), Storgaard, M. (Ekstern), Olsen, R. (Ekstern), Sparsø, J. (Intern),
Madsen, J. (Intern)
Pages: 780-785
Publication date: 2005

**Host publication information**
Title of host publication: Design, Automation and Test in Europe
ISBN (Print): 0-7695-2288-2
Main Research Area: Technical/natural sciences
Conference: 2005 Design, Automation and Test in Europe Conference and Exposition, Munich, Germany, 07/03/2005 - 07/03/2005
Electronic versions:
Angiolini.pdf
DOIs:
10.1109/DATE.2005.22

**Bibliographical note**
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Source: orbit
Source-ID: 185716
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

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**An OCP Compliant Network Adapter for GALS-based SoC Design Using the MANGO Network-on-Chip**
The demand for IP reuse and system level scalability in System-on-Chip (SoC) designs is growing. Network-on-chip (NoC)
constitutes a viable solution space to emerging SoC design challenges. In this paper we describe an OCP compliant
network adapter (NA) architecture for the MANGO NoC. The NA decouples communication and computation, providing
memory-mapped OCP transactions based on primitive message-passing services of the network. Also, it facilitates GALS-
type systems, by adapting to the clockless network. This helps leverage a modular SoC design flow. We evaluate
performance and cost of 0.13 um CMOS standard cell instantiations of the architecture.

**General information**
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Bjerregaard, T. (Intern), Mahadevan, S. (Intern), Olsen, R. G. (Ekstern), Sparsø, J. (Intern)
Pages: 171-174
Publication date: 2005

**Host publication information**
Title of host publication: Proceedings of the International Symposium on System-on-Chip (SoC'05)
Publisher: IEEE
ISBN (Print): 0-7803-9294-9
Main Research Area: Technical/natural sciences
Conference: Proceedings of the International Symposium on System-on-Chip (SoC'05), 01/01/2005
standard socket, asynchronous, ocp, clockless, Network-on-chip
Electronic versions:
imm4165.pdf
DOIs:
10.1109/ISSOC.2005.1595670

**Bibliographical note**
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Source: orbit
Source-ID: 185667
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005
A Router Architecture for Connection-Oriented Service Guarantees in the MANGO Clockless Network-on-Chip

On-chip networks for future system-on-chip designs need simple, high performance implementations. In order to promote system-level integrity, guaranteed services (GS) need to be provided. We propose a network-on-chip (NoC) router architecture to support this, and demonstrate with a CMOS standard cell design. Our implementation is based on clockless circuit techniques, and thus inherently supports a modular, GALS-oriented design flow. Our router exploits virtual channels to provide connection-oriented GS, as well as connection-less best-effort (BE) routing. The architecture is highly flexible, in that support for different types of BE routing and GS arbitration can be easily plugged into the router.

A Scheduling Discipline for Latency and Bandwidth Guarantees in Asynchronous Network-on-Chip

Guaranteed services (GS) are important in that they provide predictability in the complex dynamics of shared communication structures. This paper discusses the implementation of GS in asynchronous Network-on-Chip. We present a novel scheduling discipline called Asynchronous Latency Guarantee (ALG) scheduling, which provides latency and bandwidth guarantees in accessing a shared media, e.g. a physical link shared between a number of virtual channels. ALG overcomes the drawbacks of existing scheduling disciplines, in particular the coupling between latency and bandwidth guarantees. A 0.12 µm CMOS standard cell implementation of an ALG link has been simulated. The operation speed of the design was 702 MD/s.
Behavioral synthesis of asynchronous circuits

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling, System-on-Chip Hardware, Embedded Systems Engineering
Authors: Nielsen, S. F. (Intern), Sparsø, J. (Intern), Madsen, J. (Intern)
Publication date: 2005

Publication information
Original language: English
Series: IMM-PHD-2005-144
Main Research Area: Technical/natural sciences
Electronic versions:
imm3866.ps
imm3866.pdf
Links:
http://www2.imm.dtu.dk/pubdb/p.php?3866
Source: orbit
Source-ID: 185930
Publication: Research › Ph.D. thesis – Annual report year: 2005

Modular SoC-Design using the MANGO clockless NoC (Invited talk)

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Bjerregaard, T. (Intern), Sparsø, J. (Intern), Mahadevan, S. (Intern), Madsen, J. (Intern)
Publication date: 2005

Host publication information
Title of host publication: International Conference on Parallel Computing (PARCO'05)
Place of publication: PARCO
Publisher: PARCO
Main Research Area: Technical/natural sciences
Conference: International Conference on Parallel Computing (PARCO'05), 01/01/2005
Links:
http://www2.imm.dtu.dk/pubdb/p.php?3919
Source: orbit
Source-ID: 185785
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

Realistically Rendering SoC Traffic Patterns with Interrupt Awareness

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Angiolini, F. (Ekstern), Mahadevan, S. (Ekstern), Madsen, J. (Intern), Benini, L. (Ekstern), Sparsø, J. (Intern)
Publication date: 2005
A Channel Library for Asynchronous Circuit Design Supporting Mixed-Mode Modelling

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Bjerregaard, T. (Intern), Mahadevan, S. (Intern), Sparsø, J. (Intern)
Pages: 301-310
Publication date: 2004

Host publication information
Title of host publication: PATMOS 2004, 14th Intl. Workshop on Power and Timing Modeling, Optimization and Simulation
Publisher: Springer
Main Research Area: Technical/natural sciences
Links:
Source: orbit
Source-ID: 154595
Publication: Research - peer-review › Article in proceedings – Annual report year: 2004

A Low-Power Heterogeneous Multiprocessor Architecture for Audio Signal Processing

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Paker, O. (Intern), Sparsø, J. (Intern), Isager, M. (Ekstern), Haandbæk, N. (Ekstern), Nielsen, L. S. (Ekstern)
Pages: 95-110
Publication date: 2004

Publication information
Volume: 37
Issue number: 1
Original language: English
Links:
Source: orbit
Source-ID: 154564
Publication: Research - peer-review › Journal article – Annual report year: 2004

Future Networks-on-Chip; will they be Synchronous or Asynchronous? (Invited talk)

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Sparsø, J. (Intern)
Publication date: 2004

Host publication information
Title of host publication: SSoCC ’04 (Swedish System on Chip Conference, Båstad)
Main Research Area: Technical/natural sciences
Links:
Source: orbit
Towards behavioral synthesis of asynchronous circuits - an implementation template targeting syntax directed compilation

This paper presents a method for behavioral synthesis of asynchronous circuits. Our approach aims at providing a synthesis flow which is very similar to what is found in existing synchronous design tools. We adapt the synchronous behavioral synthesis abstraction into the asynchronous handshake domain by introducing a computation model, which resembles the synchronous datapath and control architecture, but which is completely asynchronous. The datapath and control architecture is then expressed in the Balsa-language, and using syntax directed compilation a corresponding handshake circuit implementation is produced. The paper also reports area, speed and power figures for a couple of benchmark circuits, which have been synthesized to layout.

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Nielsen, S. F. (Intern), Sparsø, J. (Intern), Madsen, J. (Intern), Selvaraj, H. (ed.) (Ekstern)
Publication date: 2004

Host publication information
Title of host publication: EUROMICRO Symposium on Digital System Design
Publisher: IEEE
ISBN (Print): 0-7695-2203-3
Main Research Area: Technical/natural sciences
Conference: Euromicro Symposium on Digital System Design, 01/01/2004
Electronic versions:
Nielsen.pdf
DOIs:
10.1109/DSD.2004.1333290

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Source: orbit
Source-ID: 154641
Publication: Research - peer-review › Article in proceedings – Annual report year: 2004

Virtual Channel Designs for Guaranteeing Bandwith in Asynchronous Network-on-chip

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Bjerregaard, T. (Intern), Sparsø, J. (Intern)
Pages: 269-272
Publication date: 2004

Host publication information
Title of host publication: 22nd Norchip Conference
Publisher: IEEE
Main Research Area: Technical/natural sciences
Links:
Source: orbit
Source-ID: 154596
Publication: Research - peer-review › Article in proceedings – Annual report year: 2004

Compact beamforming in medical ultrasound scanners
This Ph.D. project was carried out at the Center for Fast Ultrasound Imaging, Technical University of Denmark, under the supervision of Prof. Jørgen Arendt Jensen, Assoc. Prof. Jens Sparsø and Prof. Erik Bruun. The goal was to investigate methods for efficient beamforming, which make it possible to fit a large number of channels on a single integrated circuit. The use of oversampled analog-to-digital (A/D) converters with the corresponding beamforming was identified as a particularly promising approach, since it provides both inexpensive and compact A/D conversion and allows for much more compact implementation of the beamformer compared to the case where conventional A/D conversion is used. The compact and economic beamforming is a key aspect in the progress of medical ultrasound imaging. Currently, 64 or 128
channels are widely used in scanners, top-of-the-range scanners have 256 channels, and even more channels are necessary for 3-dimensional (3D) diagnostic imaging. On the other hand, there is a demand for inexpensive portable devices for use outside hospitals, in field conditions, where power consumption and compactness are important factors. The thesis starts with an introduction into medical ultrasound, its basic principles, system evolution and its place among medical imaging techniques. Then, ultrasound acoustics is introduced, as a necessary base for understanding the concepts of acoustic focusing and beamforming, which follow. The necessary focusing information for high-quality imaging is large, and compressing it leads to better compactness of the beamformers. The existing methods for compressing and recursive generation of focusing data, along with original work in the area, are presented in Chapter 4. The principles and the performance limitations of the oversampled delta-sigma converters are given in Chapter 5, followed by an overview of the present architectures of oversampled beamformers. Then, a new architecture is introduced, which has the potential of achieving the highest image quality that an oversampling beamformer can provide. That architecture has been implemented using VHDL, and estimates for its performance have been obtained. The results indicate that a 32-channel beamformer reaches the target operation frequency of 140 MHz, thereby providing diagnostic image with dynamic range of 60 dB for an excitation central frequency of 3 MHz. That image quality is comparable to that of the very good scanners currently on the market. The performance results have been achieved with the use of a simple oversampled converter of second order. The use of a higher order oversampled converter will allow higher pulse frequency to be used while the high dynamic range in the end image is preserved. The logic resource utilization of a Xilinx FPGA device XCV2000E-7 is less than 45 % when a 32-channel beamformer is implemented. The maximum number of channels that can fit in that FPGA device is 57, due to the fact that too many of the available gates take part in the routing when the channel number is increased.

Low power digital signal processing
This thesis introduces a novel approach to programmable and low power platform design for audio signal processing, in particular hearing aids. The proposed programmable platform is a heterogeneous multiprocessor architecture consisting of small and simple instruction set processors called mini-cores as well as standard DSP/CPU-cores that communicate using message passing. The work has been based on a study of the algorithm suite covering the application domain. The observation of dominant tasks for certain algorithms (FIR, IIR, correlation, etc.) that require custom computational units and special data addressing capabilities lead to the design of low power mini-cores. The algorithm suite also consisted of less demanding and/or irregular algorithms (LMS, compression) that required subsample rate signal processing justifying the use of a DSP/CPU-core. The thesis also contributes to the recent trend in the development of intellectual property based design methodologies. The actual mini-core designs are parameterized in word-size, memory-size, etc. and can be instantiated according to the needs of the application at hand. They are intended as low power programmable building blocks for a standard cell synthesis based design flow leading to a system-on-chip. Two mini-cores targeting FIR and IIR type of algorithms have been designed to evaluate the concept. Results obtained from the design of a prototype chip demonstrate a power consumption that is only 1.5 - 1.6 times larger than commercial hardwired ASICs and more than 621 times lower than current state of the art low-power DSP processors. An orthogonal but practical contribution of this thesis is the test bench implementation. A PCI-based FPGA board has been used to equip a standard desktop PC with tester facilities. The test bench proved to be a viable alternative to conventional expensive test equipment. Finally, the work presented in this thesis has been published at several IEEE workshops and conferences, and in the Journal of VLSI Signal Processing.

Low power digital signal processing
This thesis introduces a novel approach to programmable and low power platform design for audio signal processing, in particular hearing aids. The proposed programmable platform is a heterogeneous multiprocessor architecture consisting of small and simple instruction set processors called mini-cores as well as standard DSP/CPU-cores that communicate using message passing. The work has been based on a study of the algorithm suite covering the application domain. The observation of dominant tasks for certain algorithms (FIR, IIR, correlation, etc.) that require custom computational units and special data addressing capabilities lead to the design of low power mini-cores. The algorithm suite also consisted of less demanding and/or irregular algorithms (LMS, compression) that required subsample rate signal processing justifying the use of a DSP/CPU-core. The thesis also contributes to the recent trend in the development of intellectual property based design methodologies. The actual mini-core designs are parameterized in word-size, memory-size, etc. and can be instantiated according to the needs of the application at hand. They are intended as low power programmable building blocks for a standard cell synthesis based design flow leading to a system-on-chip. Two mini-cores targeting FIR and IIR type of algorithms have been designed to evaluate the concept. Results obtained from the design of a prototype chip demonstrate a power consumption that is only 1.5 - 1.6 times larger than commercial hardwired ASICs and more than 621 times lower than current state of the art low-power DSP processors. An orthogonal but practical contribution of this thesis is the test bench implementation. A PCI-based FPGA board has been used to equip a standard desktop PC with tester facilities. The test bench proved to be a viable alternative to conventional expensive test equipment. Finally, the work presented in this thesis has been published at several IEEE workshops and conferences, and in the Journal of VLSI Signal Processing.
The Synputer - A Novel MIMD Processor Targeting High Performance Low Power DSP Applications

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Streltsov, N. (Ekstern), Sparsø, J. (Intern), Bokov, S. (Ekstern), Kleberg, S. (Ekstern)
Publication date: 2003

Host publication information
Title of host publication: International Signal Processing Conference
Publisher: Global Technology Conferences (www.gt-conferences.com)
Main Research Area: Technical/natural sciences

Using SystemC to Model Asynchronous Communication at Different Levels of Abstraction

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Mahadevan, S. (Intern), Bjerregaard, T. (Intern), Sparsø, J. (Intern), Madsen, J. (Intern)
Publication date: 2003

Host publication information
Title of host publication: Third ACiD-WG Workshop, Heraklion, Crete, Greece
Main Research Area: Technical/natural sciences

A heterogeneous multi-core platform for low power signal processing in systems-on-chip
This paper presents a low-power and programmable DSP architecture - a heterogeneous multiprocessor platform consisting of standard CPU/DSP cores, and a set of simple instruction set processors called mini-cores each optimized for a particular class of algorithm (FIR, IIR, LMS, etc.). Communication is based on message passing. The mini-cores are designed as parameterized soft macros intended for a synthesis based design flow. A 520,000 transistor 0.25µm CMOS prototype chip containing 6 mini-cores has been fabricated and tested. Its power consumption is only 50% higher than a hardwired ASIC and more than 6-21 times lower than a general purpose CPU/DSP core while executing non-trivial industrial applications.

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Embedded Systems Engineering, Department of Information Technology
Authors: Paker, O. (Intern), Sparsø, J. (Intern), Haandbæk, N. (Ekstern), Isager, M. (Ekstern), Nielsen, L. S. (Intern)
Publication date: 2002

Host publication information
Publisher: IEEE Press
ISBN (Print): 88-900847-9-0
A Heterogeneous Multi-Core Platform for Low Power Signal Processing

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Embedded Systems Engineering
Authors: Paker, O. (Intern), Sparsø, J. (Intern)
Publication date: 2002

Host publication information
Title of host publication: Proceedings of the IEEE Workshop "Heterogeneous reconfigurable Systems on Chip"
Publisher: RWTH Aachen
Editor: Blume, H.
Main Research Area: Technical/natural sciences
Conference: IEEE Workshop "Heterogeneous reconfigurable Systems on Chip", 01/01/2002
Source: orbit
Source-ID: 58214
Publication: Research - peer-review › Article in proceedings – Annual report year: 2002

Embedded tutorial 1: Future Directions in Clocking Multi-GHz Systems

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Oklobdzija, V. G. (Ekstern), Sparsø, J. (Intern)
Publication date: 2002

Host publication information
ISLPED '02.
Publisher: IEEE Computer Society Press
Main Research Area: Technical/natural sciences
Links:
Source: orbit
Source-ID: 58259
Publication: Research - peer-review › Article in proceedings – Annual report year: 2002

High-level synthesis of asynchronous circuits from control data flow graph representations

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Nielsen, S. F. (Intern), Sparsø, J. (Intern), Madsen, J. (Intern), Hammerstoft, J. (Ekstern), Hansen, J. S. (Ekstern)
Publication date: 2002

Host publication information
Title of host publication: Second ACiD-WG Workshop (of the european commission's fifth framework programme), Munich, Germany 28-29 January
Main Research Area: Technical/natural sciences
Links:
http://www.scism.sbu.ac.uk/ccsv/ACiD-WG/Workshop2FP5/Programme/
A heterogeneous multiprocessor architecture for low-power audio signal processing applications

This paper describes a low-power programmable DSP architecture that targets audio signal processing. The architecture can be characterized as a heterogeneous multiprocessor consisting of small and simple instruction set processors called mini-cores that communicate using message passing. The processors are tailored for different classes of filtering algorithms (FIR, IIR, N-LMS etc.), and in a typical system the communication among processors occurs at the sampling rate only. The processors are parameterized in word-size, memory-size, etc. and can be instantiated according to the needs of the application at hand using a normal synthesis based ASIC design flow. To give an impression of the size of a processor we mention that one of the FIR processors in a prototype design has 16 instructions, a 32 word×16 bit program memory, a 64 word×16 bit data memory and a 25 word×16 bit coefficient memory. Early results obtained from the design of a prototype chip containing filter processors for a hearing aid application, indicate a power consumption that is an order of magnitude better than current state of the art low-power audio DSPs implemented using full-custom techniques. This is due to: (1) the small size of the processors and (2) a smaller instruction count for a given task.

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering, Department of Information Technology, Oticon A/S
Authors: Paker, O. (Intern), Sparsø, J. (Intern), Haandbæk, N. (Ekstern), Isager, M. (Ekstern), Nielsen, L. S. (Intern)
Pages: 47-53
Publication date: 2001

Host publication information
Title of host publication: Proceedings on IEEE Computer Society Workshop
ISBN (Print): 0-7695-1056-6
Main Research Area: Technical/natural sciences
Conference: IEEE Computer Society Workshop, Orlando, FL, 01/01/2001

Electronic versions:
parker.pdf
DOIs:
10.1109/IWV.2001.923139

Bibliographical note
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Source: orbit
Source-ID: 58246
Publication: Research › Article in proceedings – Annual report year: 2002

Analysis of low-power SoC interconnection networks

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Nielsen, S. F. (Intern), Sparsø, J. (Intern)
Pages: 77-86
Publication date: 2001

Host publication information
Title of host publication: IEEE 19th Norchip Conference
Main Research Area: Technical/natural sciences
Links:

Source: orbit
Source-ID: 259241
Publication: Research - peer-review › Article in proceedings – Annual report year: 2001

Asynchronous circuit design - A tutorial
Principles of Asynchronous Circuit Design - A Systems Perspective

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Sparse, J. (Intern), Furber, S. (ed.) (Ekstern)
Number of pages: 360
Publication date: 2001

Publication information
Publisher: Kluwer
ISBN (Print): 0-7923-7613-7
Original language: English
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 57923
Publication: Research - peer-review › Book – Annual report year: 2001

Channel Abstraction and Statement Level Concurrency in VHDL++

General information
State: Published
Organisations: Department of Information Technology, Department of Informatics and Mathematical Modeling
Authors: Pletscher-Frankild, S. (Intern), Sparsø, J. (Intern)
Publication date: 2000

Host publication information
Title of host publication: 4th Asynchronous Circuit Design Workshop ACID 2000
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 176523
Publication: Research - peer-review › Article in proceedings – Annual report year: 2000

Asynchronous Design using plain VHDL in a standard CAD-tool framework

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Pedersen, M. (Ekstern), Sparsø, J. (Intern)
Number of pages: 3
Publication date: 1999
Designing Asynchronous Circuits for Low Power: An IFIR Filter (Invited Paper)

This paper addresses the design of asynchronous circuits for low power through an example: a filter bank for a digital hearing aid. The asynchronous design re-implements an existing synchronous circuit which is used in a commercial product. For comparison, both designs have been fabricated in the same 0.7 μm CMOS technology. When processing typical data (less than 50 dB sound pressure), the asynchronous control and data-path logic, an improved RAM design, and by a mechanism that adapts the number range to the actual need (exploiting the fact that typical audio signals are characterized by numerically small samples). Apart from the improved RAM design, these measures are only viable in an asynchronous design. The principles and techniques explained in this paper are of a general nature, and they apply to the design of asynchronous low-power digital signal-processing circuits in a broader perspective. In fact, this understanding is one of the contributions of the paper. Finally, the paper can be read as an example-driven introduction to asynchronous low-power design.

General information
State: Published
Organisations: Department of Information Technology, Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Nielsen, L. S. (Intern), Sparsø, J. (Intern)
Pages: 268-281
Publication date: 1999
Main Research Area: Technical/natural sciences

Publication information
Journal: Proceedings of the IEEE
Volume: 87
Issue number: 2
ISSN (Print): 0018-9219
Ratings:
BFI (2018): BFI-level 2
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 2
Web of Science (2017): Indexed Yes
BFI (2016): BFI-level 2
Scopus rating (2016): SJR 1.343 SNIP 3.847 CiteScore 7.68
Web of Science (2016): Indexed yes
BFI (2015): BFI-level 2
Scopus rating (2015): SJR 1.436 SNIP 4.503 CiteScore 6.93
BFI (2014): BFI-level 2
Scopus rating (2014): SJR 1.439 SNIP 5.067 CiteScore 6.26
BFI (2013): BFI-level 2
Scopus rating (2013): SJR 1.792 SNIP 5.959 CiteScore 7.59
ISI indexed (2013): ISI indexed yes
Web of Science (2013): Indexed yes
BFI (2012): BFI-level 2
Scopus rating (2012): SJR 2.66 SNIP 6.76 CiteScore 9.37
ISI indexed (2012): ISI indexed yes
BFI (2011): BFI-level 2
Scopus rating (2011): SJR 1.93 SNIP 5.417 CiteScore 7.83
ISI indexed (2011): ISI indexed yes
BFI (2010): BFI-level 2
Scopus rating (2010): SJR 2.123 SNIP 5.428
High Speed Frame Synchronization and Viterbi Decoding

General information
State: Published
Organisations: Department of Photonics Engineering, Coding, Department of Informatics and Mathematical Modeling, Computer Science and Engineering, Department of Telecommunication
Authors: Paaske, E. (Intern), Justesen, J. (Intern), Larsen, K. J. (Intern), Hansen, F. (Ekstern), Pedersen, S. (Intern), Sparsø, J. (Intern), Andersen, J. D. (Intern), Bach, T. B. (Intern), Garde, T. F. (Ekstern)
Publication date: 1998

Publication information
Publisher: Technical University of Denmark, Dept. of Telecommunication (now COM)
Original language: English
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 201012
Publication: Research - peer-review › Report – Annual report year: 1998

High Speed Frame Synchronization and Viterbi Decoding: Final Report
The study has been divided into two phases. The purpose of Phase 1 of the study was to describe the system structure and algorithms in sufficient detail to allow drawing the high level architecture of units containing frame synchronization and Viterbi decoding. After selection of which specific units to detail, the purpose of Phase 2 was to make VHDL models for the selected units. The overall development process is described in the report. The systems we consider are high data rate space communication systems. Also, the systems use some form of QPSK modulation and transmit data in frames separated by a sync marker and protected by error-correcting codes. We first give a survey of trends within the area of space modulation systems. We then discuss and define the interfaces and operating modes of the relevant system components. We present a list of system configurations that we find potentially useful. Algorithms for frame synchronization are described and analyzed. Further, the high level architecture of units that contain frame synchronization and various other functions needed in a complete system is presented. Two such units are described, one for placement before the Viterbi decoder and another for placement after the decoder. The unit for placement after the decoder was selected for detailing in Phase 2. We describe the detailed architecture in sufficient detail to allow modeling and verification of the models. The models aim at specifying all functional details and may be a first step towards a realization in a FPGA. Node synchronization performed within a Viterbi decoder is discussed, and the high level architectures of three possible implementations of Viterbi decoders are described: The first implementation uses a number of commercially available decoders while the the two others are completely new implementations aimed at ASICs, one for a data rate of 75 Mbit/s and the second for a data rate of 150 Mbit/s. The latter unit was selected for detailing in Phase 2. We describe the detailed architecture in sufficient detail to allow modeling and verification of the models. The models aim at specifying all functional details and may be a first step towards a realization in an ASIC.

General information
State: Published
Organisations: Department of Telecommunication, National Space Institute, Department of Information Technology
Authors: Paaske, E. (Intern), Justesen, J. (Intern), Larsen, K. J. (Intern), Hansen, F. (Intern), Pedersen, S. (Intern), Sparsø, J. (Intern), Andersen, J. D. (Intern), Bach, T. B. (Intern), Garde, T. (Intern)
Number of pages: 306
Publication date: 1998

Publication information
Original language: English
The design of an asynchronous Tiny RISC TM/TR4101 microprocessor core

This paper presents the design of an asynchronous version of the TR4101 embedded microprocessor core developed by LSI Logic Inc. The asynchronous processor, called ARISC, was designed using the same CAD tools and the same standard cell library that was used to implement the TR4101. The paper reports on the design methodology, the architecture, the implementation, and the performance of the ARISC. This includes a comparison with the TR4101, and a detailed breakdown of the power consumption in the ARISC. ARISC is our first attempt at an asynchronous
implementation and a number of simplifying decisions were made up front. Throughout the entire design we use four-phase handshaking in combination with a normally opaque latch controller. All logic is implemented using static logic standard cells. Despite this the ARISC performs surprisingly well: In 0.35 μm CMOS performance is 74-123 MIPS depending on the instruction mix, and at 74 MIPS the power efficiency is 635 MIPS/Watt.

**General information**

State: Published
Organisations: Department of Information Technology, Department of Informatics and Mathematical Modeling, LSI Logic Denmark
Authors: Christensen, K. T. (Intern), Jensen, P. (Ekstern), Korger, P. (Ekstern), Sparsø, J. (Intern)
Pages: 108-119
Publication date: 1998

**Host publication information**

Publisher: IEEE
ISBN (Print): 0-8186-8392-9
Main Research Area: Technical/natural sciences
Electronic versions:
Christensen.pdf
DOIs:
10.1109/ASYNC.1998.666498

**Bibliographical note**

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Source: orbit
Source-ID: 170083
Publication: Research - peer-review › Article in proceedings – Annual report year: 1998

**Compilation of lecture notes for "Summer School on Asynchronous Circuit Design", DTU, August 18-22**

**General information**

State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Sparsø, J. (Intern)
Publication date: 1997

**Publication information**

Original language: English
Main Research Area: Technical/natural sciences
Links:
http://www2.imm.dtu.dk/pubdb/p.php?4537
Source: orbit
Source-ID: 201143
Publication: Education › Compendium/lecture notes – Annual report year: 1997

**A low-power asynchronous data-path for a FIR filter bank**

This paper describes a number of design issues relating to the implementation of low-power asynchronous signal processing circuits. Specifically, the paper addresses the design of a dedicated processor structure that implements an audio FIR filter bank which is part of an industrial application. The algorithm requires a fixed number of steps and the moderate speed requirement allows a sequential implementation. The latter, in combination with a huge predominance of numerically small data values in the input data stream, is the key to a low-power asynchronous implementation. Power is minimized in two ways: by reducing the switching activity in the circuit, and by applying adaptive scaling of the supply voltage, in order to exploit the fact that the average case latency is 2-3 times better than the worst case. The paper reports on a study of properties of real life data, and discusses the implications it has on the choice of architecture, handshake-protocol, data-encoding, and circuit design. This includes a tagging scheme that divides the data-path into slices, and an asynchronous ripple carry adder that avoids a completion tree.

**General information**
Host publication information
Title of host publication: Proceedings of the second International Symposium on Asynchronous Circuits and Systems
Publisher: IEEE
Main Research Area: Technical/natural sciences
Electronic versions: Spar.pdf
DOIs: 10.1109/ASYNC.1996.494451

Bibliographical note
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Source: orbit
Source-ID: 167189
Publication: Research - peer-review › Article in proceedings – Annual report year: 1996

ACiD-WG workshop on asynchronous low-power VLSI

General information
State: Published
Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling, Department of Information Technology, South Bank University
Publication date: 1994

Publication information
Original language: English
Series: Uden navn
Number: ID-TR:1994-140
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 263193
Publication: Research - peer-review › Report – Annual report year: 1994

ACiD-WG workshop on Asynchronous Low-Power VLSI, Lyngby, Denmark, April 11-12

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling, Department of Information Technology
Publication date: 1994

Publication information
Publisher: Technical University of Denmark (DTU)
Original language: English
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 200613
Publication: Research - peer-review › Book – Annual report year: 1994
Low-power operation using self-timed circuits and adaptive scaling of the supply voltage

Recent research has demonstrated that for certain types of applications like sampled audio systems, self-timed circuits can achieve very low power consumption, because unused circuit parts automatically turn into a stand-by mode. Additional savings may be obtained by combining the self-timed circuits with a mechanism that adaptively adjusts the supply voltage to the smallest possible, while maintaining the performance requirements. This paper describes such a mechanism, analyzes the possible power savings, and presents a demonstrator chip that has been fabricated and tested. The idea of voltage scaling has been used previously in synchronous circuits, and the contributions of the present paper are: 1) the combination of supply scaling and self-timed circuitry which has some unique advantages, and 2) the thorough analysis of the power savings that are possible using this technique.
Delay-insensitive Multi-ring Structures
This paper describes a set of simple design and performance analysis techniques that have been successfully used to design a number of non-trivial delay-insensitive circuits. Examples are building blocks for digital filters and a vector multiplier using a serial-parallel multiply and accumulate algorithm. The vector multiplier has been laid out, submitted for fabrication, and successfully tested. This design is described in detail to illustrate the design and the performance analysis techniques. The design technique is based on a data flow approach using pipelines and rings that are composed into...
larger multi-ring structures. For this restricted class of structures, it becomes possible - even for circuits of realistic size and complexity - to analyze the performance and establish an understanding of the bottlenecks. The paper combines a number of previously published results and techniques, and the main contribution of the paper is the comprehensive, integrated presentation of the material, including a thorough description of the vector multiplier design example.

**General information**

State: Published  
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling, Department of Information Technology  
Authors: Sparsø, J. (Intern), Staunstrup, J. (Intern)  
Pages: 313-340  
Publication date: 1993  
Main Research Area: Technical/natural sciences

**Publication information**

Journal: Integration, the VLSI journal  
Volume: 15  
Issue number: 3  
ISSN (Print): 0167-9260  
Ratings:  
BFI (2018): BFI-level 1  
Web of Science (2018): Indexed yes  
BFI (2017): BFI-level 1  
Web of Science (2017): Indexed Yes  
BFI (2016): BFI-level 1  
Scopus rating (2016): SJR 0.241 SNIP 1.019 CiteScore 1.25  
BFI (2015): BFI-level 1  
Scopus rating (2015): SJR 0.247 SNIP 1.083 CiteScore 1.09  
Web of Science (2015): Indexed yes  
BFI (2014): BFI-level 1  
Scopus rating (2014): SJR 0.303 SNIP 1.198 CiteScore 1.19  
BFI (2013): BFI-level 1  
Scopus rating (2013): SJR 0.322 SNIP 1.03 CiteScore 1.28  
ISI indexed (2013): ISI indexed yes  
BFI (2012): BFI-level 1  
Scopus rating (2012): SJR 0.238 SNIP 1.23 CiteScore 1.19  
ISI indexed (2012): ISI indexed yes  
BFI (2011): BFI-level 1  
Scopus rating (2011): SJR 0.297 SNIP 0.768 CiteScore 1.23  
ISI indexed (2011): ISI indexed yes  
BFI (2010): BFI-level 1  
Scopus rating (2010): SJR 0.274 SNIP 0.963  
BFI (2009): BFI-level 1  
Scopus rating (2009): SJR 0.304 SNIP 0.952  
BFI (2008): BFI-level 1  
Scopus rating (2008): SJR 0.266 SNIP 0.747  
Scopus rating (2007): SJR 0.524 SNIP 1.552  
Scopus rating (2006): SJR 0.332 SNIP 0.998  
Scopus rating (2005): SJR 0.272 SNIP 1.15  
Scopus rating (2004): SJR 0.182 SNIP 0.646  
Scopus rating (2003): SJR 0.471 SNIP 0.773  
Scopus rating (2002): SJR 0.162 SNIP 0.64  
Scopus rating (2001): SJR 0.18 SNIP 0.134  
Scopus rating (2000): SJR 0.169 SNIP 0.242  
Scopus rating (1999): SJR 0.179 SNIP 0.372  
Original language: English  
Links:  
http://www2.imm.dtu.dk/pubdb/p.php?4403
Design and performance analysis of delay insensitive multi-ring structures

A set of simple design and performance analysis techniques that have been successfully used to design a number of nontrivial delay insensitive circuits is described. Examples are building blocks for digital filters and a vector multiplier using a serial-parallel multiply and accumulate algorithm. The vector multiplier circuit has been laid out, submitted for fabrication and successfully tested. Throughout the analysis elements from this design are used to illustrate the design and performance analysis techniques. The design technique is based on a data flow approach using pipelines and rings that are composed into larger multiring structures by joining and forking of signals. By limiting to this class of structures, it is possible, even for complex designs, to analyze the performance and establish an understanding of the bottlenecks.

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling, Department of Information Technology
Authors: Sparsø, J. (Intern), Staunstrup, J. (Intern)
Pages: 349-358
Publication date: 1993

Host publication information
Title of host publication: Proceeding of the 26th Hawaii International Conference on System Sciences
Volume: Volume 1
Publisher: IEEE
Main Research Area: Technical/natural sciences
Conference: Hawaii International Conference on Systems Sciences, Hawaii, US, 01/01/1993
Electronic versions:
Jens.pdf
DOIs:
10.1109/HICSS.1993.270630

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Source: orbit
Source-ID: 200383
Publication: Research - peer-review › Article in proceedings – Annual report year: 1993

Design of Self-timed Multipliers: A Comparison

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling, Department of Information Technology
Pages: 165-180
Publication date: 1993

Host publication information
Title of host publication: Asynchronous Design Methodologies
Publisher: Elsevier Science Publishers
Main Research Area: Technical/natural sciences
Conference: Asynchronous Design Methodologies, 01/01/1993
Source: orbit
Source-ID: 200384
Publication: Research - peer-review › Article in proceedings – Annual report year: 1993

Design and development of a very high speed Reed-Solomon encoder/decoder chip set: Architectural design report

General information
Design and development of a very high speed Reed-Solomon encoder/decoder chip set: Requirement analysis.

General information
State: Published
Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling
Authors: Bauduin, F. (Ekstern), Klootsema, R. (Ekstern), Rievers, S. (Ekstern), Dijkstra, E. D. (Ekstern), Paaske, E. (Ekstern), Justesen, J. (Ekstern), Larsen, K. J. (Ekstern), Sparsø, J. (Intern), Pedersen, S. (Ekstern)
Number of pages: 126
Publication date: 1992

Publication information
Publisher: Centre Suisse d'électronique et microtechnique S. A. (CSEM) and Technical University of Denmark
Original language: English
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 263197
Publication: Research - peer-review › Report – Annual report year: 1992

Design and Performance Analysis of Delay-Insensitive Multi-Ring Structures

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Sparsø, J. (Intern), Staunstrup, J. (Intern)
Publication date: 1992

Publication information
Publisher: Department of Computer Science, Technical University of Denmark
Original language: English
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 201039
Publication: Research - peer-review › Report – Annual report year: 1992

Design of delay insensitive circuits using multi-ring structures

The design and VLSI implementation of a delay insensitive circuit that computes the inner product of two vectors is described. The circuit is based on an iterative serial-parallel multiplication algorithm. The design is based on a data flow approach using pipelines and rings that are combined into larger multi ring structures by the joining and forking of signals. The implementation is based on a small set of building blocks (latches, combinational circuits and switches) that are composed of C-elements and simple gates. By following this approach, delay insensitive circuits with nontrivial functionality and reasonable performance are readily designed.

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Sparsø, J. (Intern), Staunstrup, J. (Intern), Dantzer-Sørensen, M. (Ekstern)
An area-efficient path memory structure for VLSI Implementation of high speed Viterbi decoders

Path storage and selection methods for Viterbi decoders are investigated with special emphasis on VLSI implementations. Two well-known algorithms, the register exchange, algorithm, REA, and the trace back algorithm, TBA, are considered. The REA requires the smallest number of storage elements, but the storage elements must be provided with multiplexers on the input and they have a poor density compared to RAM cells. Furthermore, a rather complicated interconnection structure is required. The TBA requires more than three times as many storage elements, but these can be realized as RAM cells. A new algorithm which combines the advantages of both the REA and the TBA is proposed. It requires only slightly more storage elements than the REA and most of the storage elements can be realized as RAM cells. For a standard decoder with constraint length $K = 7$, rate $R = 12$ and decoding depth $L = 56$, significant area savings compared to the REA and the TBA are achieved. Furthermore, the relative area savings increase for larger decoding depths, which might be desirable for punctured codes. Based on the new algorithm a test chip has been designed and fabricated in a 2 micron CMOS process using MOSIS like simplified design rules. The chip operates at 20 Mbit/s. The core of the chip measures 3.5 x 8.1 mm², and it contains approximately 50,000 transistors.

General information
State: Published
Organisations: Department of Photonics Engineering, Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Paaske, E. (Intern), Pedersen, S. (Intern), Sparsø, J. (Intern)
Pages: 79-91
Publication date: 1991
Main Research Area: Technical/natural sciences

Publication information
Journal: Integration, the VLSI journal
Volume: 12
Issue number: 2
ISSN (Print): 0167-9260
Ratings:
BFI (2018): BFI-level 1
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 1
Web of Science (2017): Indexed Yes
BFI (2016): BFI-level 1
Scopus rating (2016): SJR 0.241 SNIP 1.019 CiteScore 1.25
BFI (2015): BFI-level 1
Scopus rating (2015): SJR 0.247 SNIP 1.083 CiteScore 1.09
Web of Science (2015): Indexed yes
BFI (2014): BFI-level 1
Scopus rating (2014): SJR 0.303 SNIP 1.198 CiteScore 1.19
An area-efficient topology for VLSI implementation of Viterbi decoders and other shuffle-exchange type structures

A topology for single-chip implementation of computing structures based on shuffle-exchange (SE)-type interconnection networks is presented. The topology is suited for structures with a small number of processing elements (i.e. 32-128) whose area cannot be neglected compared to the area required for interconnection. The processing elements are implemented in pairs that are connected to form a ring. In this way three-quarters of the interconnections are between neighbors. The ring structure is laid out in two columns and the interconnection of nonneighbors is routed in the channel between the columns. The topology has been used in a VLSI implementation of the add-compare-select (ACS) module of a fully parallel K=7, R=1/2 Viterbi decoder. Both the floor-planning issues and some of the important algorithm and circuit-level aspects of this design are discussed. The chip has been designed and fabricated in a 2-μm CMOS process using MOSIS-like simplified design rules. The chip operates at speeds up to 19 MHz under worst-case conditions (V_DD=4.75 V and T_A=70 degrees C). The core of the chip (excluding pad cells) is 7.8*5.1 mm/sup 2/ and contains approximately 50000 transistors. The interconnection network occupies 32% of the area.
A Fully Parallel VLSI-implementation of the Viterbi Decoding Algorithm

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling, Department of Photonics Engineering
Authors: Sparsø, J. (Intern), Jørgensen, H. N. (Ekstern), Paaske, E. (Intern), Pedersen, S. (Intern), Rübner-Petersen, T. (Ekstern)
Publication date: 1989

Publication information
Publisher: Department of Computer Science, Technical University of Denmark
Original language: English
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 201041
Publication: Research - peer-review › Report – Annual report year: 1989

In this paper we describe the implementation of a $K = 7$, $R = 1/2$ single-chip Viterbi decoder intended to operate at 10-20 Mbit/sec. We propose a general, regular and area efficient floor-plan that is also suitable for implementation of decoders for codes with different generator polynomials or different values of $K$. The Shuffle-Exchange type interconnection network is implemented by organizing the 64 processing elements to form a ring. The ring is laid out in two columns, and the interconnections between non-neighbours are routed in the channel between the columns. The interconnection network occupies 32% of the area, and the global signals (including power) occupy a further 10%. A test-chip containing a pair of processing elements has been fabricated via NORCHIP (the Scandinavian CMOS IC prototype implementation service). This chip has been fully tested, and it operates correctly at speeds above 26 MHz under worst-case conditions ($VDD = 4.75$ V and $T_A = 70$ °C).

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling, Department of Telecommunication, Department of Information Technology, Technical University of Denmark
Authors: Sparsø, J. (Intern), Jørgensen, H. N. (Ekstern), Paaske, E. (Intern), Pedersen, S. (Intern), Rübner-Petersen, T. (Ekstern)
Pages: 232-235
Publication date: 1989

Host publication information
Title of host publication: Proceedings of the 15th European Solid-State Circuits Conference
Publisher: IEEE
ISBN (Print): 3-85403-101-7
Main Research Area: Technical/natural sciences
Electronic versions:
Sparse.pdf

Bibliographical note
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Source: orbit
Source-ID: 200387
Publication: Research - peer-review › Article in proceedings – Annual report year: 1989

Design and implementation of a full-custom single chip Viterbi decoder

General information
Hardware Architecture of a Node for the LAN-DTH High Speed Token Ring

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Jensen, M. N. (Ekstern), Skov, M. (Ekstern), Sparsø, J. (Intern)
Pages: 214-219
Publication date: 1987

Host publication information
Title of host publication: Proc. of EFOC/LAN'87 - Fifth Annual European Fibre Optic Communications and Local Aera Networks Conference
Main Research Area: Technical/natural sciences
Conference: Proc. of EFOC/LAN'87 - Fifth Annual European Fibre Optic Communications and Local Aera Networks Conference, 01/01/1987
Source: orbit
Source-ID: 200166
Publication: Research - peer-review › Article in proceedings – Annual report year: 1987

A POLYNET to VME-bus Interface Unit - Block diagram and principles of operation

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Sparsø, J. (Intern)
Publication date: 1986

Publication information
Publisher: Department of Computer Science, Technical University of Denmark
Original language: English
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 201042
Publication: Research - peer-review › Report – Annual report year: 1986

Hardware Architecture of a Node for the LAN-DTH High Speed Token Ring

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Sparsø, J. (Intern)
Publication date: 1986

Publication information
Original language: English
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 201043
Publication: Research - peer-review › Report – Annual report year: 1986
LAN-DTH - A Hierarchical Local Area Network based on a High Speed Optic Token Ring

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Jensen, M. N. (Ekstern), Sharp, R. I. (Ekstern), Skov, M. (Ekstern), Sparse, J. (Intern)
Pages: 339-351
Publication date: 1986

Host publication information
Title of host publication: Proc.of IFIP TC6/WG6.4 International In Depth Symposium on Local Communication Systems LAN and PBX
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 200167
Publication: Research - peer-review › Article in proceedings – Annual report year: 1986

Projects:

Real-Time Multi-Core Communication and Synchronization
Department of Applied Mathematics and Computer Science
Period: 01/09/2017 → 31/08/2019
Number of participants: 3
Phd Student:
Strøm, Tórur Biskopste (Intern)
Supervisor:
Sparse, Jens (Intern)
Main Supervisor:
Schoeberl, Martin (Intern)

Financing sources
Source: Internal funding (public)
Name of research programme: Samfinansieret - Andet
Project: PhD

Real-Time Multicore Systems
Department of Applied Mathematics and Computer Science
Period: 15/08/2017 → 14/08/2020
Number of participants: 3
Phd Student:
Baris, Oktay (Ekstern)
Supervisor:
Sparse, Jens (Intern)
Main Supervisor:
Schoeberl, Martin (Intern)

Financing sources
Source: Internal funding (public)
Name of research programme: Samfinansieret - Andet
Project: PhD

Real-Time Multicore Systems
Department of Applied Mathematics and Computer Science
Period: 15/08/2017 → 14/08/2020
Number of participants: 3
Phd Student:
Dynamic Partial Reconfiguration in FPGA based Multi-core Real-time Embedded Systems

Department of Applied Mathematics and Computer Science
Period: 15/11/2014 → 17/03/2018
Number of participants: 3
Phd Student:
Pozzarossa, Luca (Intern)
Supervisor:
Schoeberl, Martin (Intern)
Main Supervisor:
Sparsø, Jens (Intern)

Financing sources
Source: Internal funding (public)
Name of research programme: Samfinansieret - Andet
Project: PhD

Hardware/Software tradeoffs in Real-Time Multiprocessor Platforms

Department of Applied Mathematics and Computer Science
Period: 01/04/2013 → 26/10/2016
Number of participants: 6
Phd Student:
Sørensen, Rasmus Bo (Intern)
Supervisor:
Schoeberl, Martin (Intern)
Main Supervisor:
Sparsø, Jens (Intern)
Examiner:
Pop, Paul (Intern)
Audsley, Neil C. (Ekstern)
Lu, Zhonghai (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: Forskningsrådsfinansiering

Relations
Publications:
Time-Predictable Communication on a Time-Division Multiplexing Network-on-Chip Multicore
Project: PhD

Time-predictable VLIW Processor

Department of Applied Mathematics and Computer Science
Period: 15/01/2012 → 09/12/2015
Number of participants: 6
Phd Student:
Abbaspourseyedi, Sahar (Intern)
Supervisor:
Asynchronous Network-on-Chip for Time-Predictable Multi-Core Embedded Systems

Department of Applied Mathematics and Computer Science
Period: 01/10/2011 → 19/06/2015
Number of participants: 6
Phd Student:
Kasapaki, Evangelia (Intern)
Supervisor:
Schoeberl, Martin (Intern)
Main Supervisor:
Sparsø, Jens (Intern)
Examiner:
Nannarelli, Alberto (Intern)
Kirner, Raimund (Ekstern)
Pedersen, Rasmus Ulslev (Intern)

Financing sources
Source: Internal funding (public)
Name of research programme: Institut, samfinansiering

Multi-objective Design Space Exploration for (re)-configurable heterogeneous Multi-ASIP SoC platforms

Department of Applied Mathematics and Computer Science
Period: 01/11/2010 → 23/01/2015
Number of participants: 6
Phd Student:
Micconi, Laura (Intern)
Supervisor:
Pop, Paul (Intern)
Main Supervisor:
Madsen, Jan (Intern)
Examiner:
Sparsø, Jens (Intern)
Pimentel, Andrew David (Ekstern)
Sander, Ingo (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: 1/3 FUU, 1/3 inst 1/3 Andet

Adaptability and Autonomy in Embedded Systems

Department of Informatics and Mathematical Modeling
Period: 01/06/2008 → 28/09/2011
Number of participants: 6
Phd Student:
Boesen, Michael Reibel (Intern)  
Supervisor:  
Pop, Paul (Intern)  
Main Supervisor:  
Madsen, Jan (Intern)  
Examiner:  
Sparsø, Jens (Intern)  
Codinachs, David Merodio (Ekstern)  
Tempesti, Gianluca (Ekstern)  

**Financing sources**  
Source: Internal funding (public)  
Name of research programme: Offentlig finansiering  
Project: PhD

**Models and Analyses for Embedded Systems Design**  
Department of Informatics and Mathematical Modeling  
Period: 01/04/2007 → 02/02/2011  
Number of participants: 6  
Phd Student:  
Brekling, Aske Wiid (Intern)  
Supervisor:  
Madsen, Jan (Intern)  
Main Supervisor:  
Hansen, Michael Reichhardt (Intern)  
Examiner:  
Sparsø, Jens (Intern)  
Ravn, Anders P. (Intern)  
Vain, Jüri (Ekstern)  

**Financing sources**  
Source: Internal funding (public)  
Name of research programme: Forskningsrådsfinansiering  
Project: PhD

**Network-on-chip: Applikationer og topologioptimering**  
Department of Informatics and Mathematical Modeling  
Period: 01/10/2006 → 30/06/2010  
Number of participants: 6  
Phd Student:  
Stuart, Matthias Bo (Intern)  
Supervisor:  
Nannarelli, Alberto (Intern)  
Main Supervisor:  
Sparsø, Jens (Intern)  
Examiner:  
Pop, Paul (Intern)  
Jantsch, Axel (Ekstern)  
Pimentel, Andrew David (Ekstern)  

**Financing sources**  
Source: Internal funding (public)  
Name of research programme: DTU-lønnet stipendie  
Project: PhD

**Systemarkitekturer baseret på Network-on-Chip**  
Department of Informatics and Mathematical Modeling
Period: 01/10/2006 → 29/09/2010
Number of participants: 7
Phd Student:
Rasmussen, Morten Sleth (Intern)
Supervisor:
Karlsson, Sven (Intern)
Madsen, Jan (Intern)
Main Supervisor:
Sparsø, Jens (Intern)
Examiner:
Probst, Christian W. (Intern)
Grahn, Håkan (Ekstern)
Nurmi, Jari Antero (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: DTU-lønnet stipendie

Relations
Publications:
Support for Programming Models in Network-on-Chip-based Many-core Systems
Project: PhD

Asynkrone Network-on-Chip
Department of Informatics and Mathematical Modeling
Period: 01/10/2005 → 31/07/2009
Number of participants: 2
Phd Student:
Stensgaard, Mikkel Bystrup (Intern)
Main Supervisor:
Sparsø, Jens (Intern)

Financing sources
Source: Internal funding (public)
Name of research programme: DTU-lønnet stipendie
Project: PhD

High performance low cost digital controlled power conversion technology
Department of Electrical Engineering
Period: 01/10/2004 → 29/08/2008
Number of participants: 8
Phd Student:
Jakobsen, Lars Tønnes (Intern)
Supervisor:
Niemann, Hans Henrik (Intern)
Thomsen, Ole Cornelius (Intern)
Tøttrup, Peter (Ekstern)
Main Supervisor:
Andersen, Michael A. E. (Ekstern)
Examiner:
Sparsø, Jens (Intern)
Arefeen, Mohammed (Ekstern)
Nelms, R. Mark (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: InnovationsPhD
Project: PhD
Chip Area Interconnection Networks
Department of Informatics and Mathematical Modeling
Period: 01/09/2002 → 18/04/2006
Number of participants: 6
Phd Student:
Mahadevan, Shankar (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Sparsø, Jens (Intern)
Examiner:
Hansen, Michael Reichhardt (Intern)
Kuchcinski, Krzysztof (Ekstern)
Wolf, Wayne Hendrix (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: Anden EU-finansiering
Project: PhD

Intra-Chip Communication
Department of Informatics and Mathematical Modeling
Period: 01/09/2002 → 10/02/2006
Number of participants: 5
Phd Student:
Bjerregaard, Tobias (Intern)
Main Supervisor:
Sparsø, Jens (Intern)
Examiner:
Nannarelli, Alberto (Intern)
Ginosar, Ran (Ekstern)
Goossens, Kees (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: DTU-lønnet stipendie
Project: PhD

Hig-Level Synthesis of Asynchronous
Department of Informatics and Mathematical Modeling
Period: 01/08/2001 → 06/06/2005
Number of participants: 6
Phd Student:
Nielsen, Sune Fallgaard (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Sparsø, Jens (Intern)
Examiner:
Nannarelli, Alberto (Intern)
Lavagno, Luciano (Ekstern)
Peeters, Ad (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: DTU-lønnet stipendie
Project: PhD
**Integrated circuits in medical ultrasound**

Department of Electrical Engineering  
Period: 15/11/1999 → 22/08/2003  
Number of participants: 7  
Phd Student:  
Tomov, Borislav Gueorguiev (Intern)  
Supervisor:  
Bruun, Erik (Intern)  
Sparsø, Jens (Intern)  
Main Supervisor:  
Jensen, Jørgen Arendt (Intern)  
Examiner:  
Sørensen, Helge Bjarup Dissing (Intern)  
Roth, Ole (Ekstern)  
Öwall, Viktor (Ekstern)  

**Financing sources**  
Source: Internal funding (public)  
Name of research programme: Forskerakademiets Samfinansier  
Project: PhD

**Types for DSP Assembler Programs**

Department of Informatics and Mathematical Modeling  
Period: 01/04/1999 → 26/02/2004  
Number of participants: 6  
Phd Student:  
Larsen, Ken (Intern)  
Supervisor:  
Sestoft, Peter (Intern)  
Main Supervisor:  
Sparsø, Jens (Intern)  
Examiner:  
Nielsen, Hanne Riis (Intern)  
Hankin, Chris (Ekstern)  
Morissett, Greg (Ekstern)  

**Financing sources**  
Source: Internal funding (public)  
Name of research programme: Forskerakademiets Samfinansier  
Project: PhD

**Low Power Digital Signal Processing**

Department of Informatics and Mathematical Modeling  
Period: 01/09/1998 → 21/01/2003  
Number of participants: 4  
Phd Student:  
Paker, Ozgun (Intern)  
Main Supervisor:  
Sparsø, Jens (Intern)  
Examiner:  
Madsen, Jan (Intern)  
Piguet, Christian (Ekstern)  

**Financing sources**  
Source: Internal funding (public)  
Name of research programme: Ansat eksternt  
Project: PhD
**PATMOS'98 workshop**

Department of Information Technology  
Period: 01/01/1998 → 30/10/1998  
Number of participants: 3  
Project participant:  
Madsen, Jan (Intern)  
Stassen, Flemming (Intern)  
Project Manager, organisational:  
Sparsø, Jens (Intern)

**Financing sources**  
Source: Unknown  
Name of research programme: Ukendt  
Amount: 37,000.00 Danish Kroner  
Source: Unknown  
Name of research programme: Ukendt  
Amount: 25,000.00 Danish Kroner  
Source: Unknown  
Name of research programme: Ukendt  
Amount: 25,000.00 Danish Kroner

**Center for Microinstruments (CfM)**  
CfM is a collaboration between the Department of Information Technology and the Microelectronics Centre, and is headed by professor Jørgen Staunstrup. CfM is established with a donation from the Thomas B. Thriges fund, while an associated graduate school financially supported by the Research Academy. CfM is supported by a range of Danish companies. The research activities of CfM focus on: - Computer Aided Engineering for micromechanical transducers - Smart transducers: design of sensors and actuators with integrated signal processing - Low power design for digital signal processors The tools and technologies developed within CfM are demonstrated in two main applications: - system level design of transducers, interfaces and digital circuit processors for hearing aids, and - topology optimized microactuators.

Department of Micro- and Nanotechnology  
Department of Information Technology  
Department of Informatics and Mathematical Modeling  

Michigan Microsensor Inc.  
Period: 01/12/1997 → 01/01/2003  
Number of participants: 9  
Project participant:  
Hansen, Ole (Intern)  
Jonsmann, Jacques (Intern)  
Vestergaard, Ras Kaas (Intern)  
Najafi, Khalil (Intern)  
Ginnerup, Morten (Intern)  
Crary, Selden (Ekstern)  
Staunstrup, Jørgen (Intern)  
Sparsø, Jens (Intern)  
Project Manager, organisational:  
Bouwstra, Siebe (Intern)

**Financing sources**  
Source: Unknown  
Name of research programme: Ukendt  
Amount: 10,000,000.00 Danish Kroner  
Source: Unknown  
Name of research programme: Ukendt  
Amount: 10,000,000.00 Danish Kroner
The Thomas B. Thrige Centre for Microinstruments is an externally funded research project at DTU. The purpose of the centre is to perform research into methods and technologies for the design of electronic systems which integrate digital, analog and micromechanical components and embedded software in a single chip – a so-called “microinstrument” – which can accomplish signal collection, signal processing, data processing, communication and actuation. The centre was originally set up as a result of a donation of 5 million Danish crowns from the Thomas B. Thrige Foundation and further donations from the companies Oticon, Widex, GN Resound and Microtronic (now Sonion MEMS). Subsequently, a number of companies, institutions, university departments and some research projects have contributed to the co-funding of a series of Ph.D. projects. In addition to those companies already mentioned, the contributors involved have been BK Medical A/S, the Center for Fast Ultrasound Imaging, Ørsted*DTU, Mikroelektronikcentret, 3D Lab, Århus Kommunehospital, the IT University in Copenhagen, the Royal Veterinary and Agricultural University and the Research School in Microelectronics, which has co-funded 5 Ph.D. projects via a grant from the Danish Research Training Council (FUR). In total, the activities of the centre have involved funding and running 8 Ph.D. projects and a series of related activities, and the overall budget has been 10 million Danish crowns. The research has focused on two areas: (1) Digital integrated circuits and computer-based systems with focus on optimization of speed, energy consumption and effective use of resources, and (2) design and manufacturing techniques for micro-electro-mechanical systems (MEMS).

The Graduate School in Microelectronics was started in 1997 and its aim was to enhance (quantitatively and qualitatively) the Ph.d.-education in the area of Microelectronics. The Graduate School was funded by the Danish Research Training Council (in Danish: Forskeruddannelsesrådet) with 1 M kr. per year. The graduate school has co-funded summer schools, visiting professors and Ph.d.-scholarships. In total 8 Ph.d.-projects has been funded jointly by the Graduate School, private companies and research projects. The projects are hosted by MIC, Ørsted*DTU and IMM and the companies involved are: B-K Medical, Dicon, GN ReSound, NOKIA, Oticon, Sensor Technology Center and SonionMEMS.
Department of Informatics and Mathematical Modeling

Department of Electrical Engineering

Department of Micro- and Nanotechnology

Period: 01/01/1997 → 31/12/2001
Number of participants: 15

Project participant:
- Paker, Ozgun (Intern)
- Larsen, Ken (Intern)
- Holten-Lund, Hans Erik (Intern)
- Pedersen, Steen (Intern)
- Madsen, Jan (Intern)
- Jensen, Jørgen Arendt (Intern)
- Tomov, Borislav Gueorguiev (Intern)
- Andreani, Pietro (Intern)
- Wang, Xiaoyan (Intern)
- Hansen, Ole (Intern)
- Yalcinkaya, Arda Deniz (Intern)
- Menon, Aric Kumaran (Intern)
- Nielsson, Daniel (Ekstern)
- Larsen, Kristian Pontoppidan (Intern)

Project Manager, organisational:
- Sparse, Jens (Intern)

Financing sources
Source: Unknown
Name of research programme: Utkendt
Amount: 1,000,000.00 Danish Kroner

Teknologiudvikling for mikroakruatorer

Department of Micro- and Nanotechnology

Period: 01/07/1996 → 17/07/2000
Number of participants: 4

PhD Student:
- Jonsmann, Jacques (Intern)

Supervisor:
- Sigmund, Ole (Intern)

Main Supervisor:
- Bouwstra, Siebe (Ekstern)

Examiner:
- Sparse, Jens (Intern)

Financing sources
Source: Internal funding (public)
Name of research programme: Mic-Finansieret-SU
Project: PhD

Integreteret hardware/software kode-generering i Co-design

Department of Information Technology

Period: 01/08/1995 → 07/02/2000
Number of participants: 4

PhD Student:
- Grode, Jesper Nicolai Riis (Intern)

Supervisor:
- Madsen, Jan (Intern)

Main Supervisor:
High Speed Frame Synchronization and Viterbi Decoding
The purpose of the project is to develop VHDL models of units for frame synchronization and Viterbi decoding to be used by the European Space Agency (ESA) for satellite communication at very high data rates (150 Mbit/s). The project was started with a study of algorithms and system architectures, and the first phase resulted in a number of suggestions for different units. Two of these were selected for a detailed design in the second phase: A Viterbi decoder for a data rate of 150 Mbit/s operating at half the clock rate (i.e. 75 MHz) and a frame synchronization unit to be placed after the Viterbi decoder. VHDL models for these two units were produced and the project is continued outside DTU with the actual manufacturing of the two units: an ASIC for the Viterbi decoder is made by VTT in Finland and an FPGA for the frame synchronizer unit is made by TERMA Elektronik A/S in Denmark.

Testing Techniques for Self-Timed Circuits
Department of Informatics and Mathematical Modeling
Number of participants: 2
Phd Student: Jianwei, Liu (Intern)
Main Supervisor: Sparse, Jens (Intern)

Financing sources
Source: Internal funding (public)
**Kredsløbsteknikker for Asynkrone Systemer**

Department of Informatics and Mathematical Modeling  
Period: 01/02/1994 → 09/09/1997  
Number of participants: 4  
Phd Student: Nielsen, Lars Skovby (Intern)  
Main Supervisor: Sparsø, Jens (Intern)  
Examiner: Skelboe, Stig (Ekstern)  
Staunstrup, Jørgen (Intern)  

**Financing sources**  
Source: Internal funding (public)

**Designmetoder og teknikker for højhastigs VLSI-kredse**

Department of Electrical Engineering  
Period: 01/02/1993 → 14/01/1997  
Number of participants: 4  
Phd Student: Midtgaard, Jacob (Intern)  
Supervisor: Sparsø, Jens (Intern)  
Svensson, Christer (Ekstern)  
Main Supervisor: Olesen, Ole (Intern)  

**Financing sources**  
Source: Internal funding (public)

Asynchronous Circuit Design  
Asynchronous circuits operate without a global clock signal - the flow of data is controlled by local handshaking between modules and registers. This gives asynchronous circuits some unique characteristics that can be exploited to advantages (higher speed, lower power consumption, modularity and robustness). The research addresses methods and techniques for designing efficient circuits, and in particular circuits with low power consumption. The experimental part of this work is based on industrial applications and involves design and fabrication of various prototype IC's. From 2001 the activities have focused on high-level synthesis of asynchronous circuits and on network-on-chip. The activity represents a long term effort and it is funded through a number of sources including the ACiD working group (IST-1999-29119), the Thomas B. Thriges Foundation and a donation from Nokia.

Department of Information Technology  
Department of Informatics and Mathematical Modeling  
Period: 01/01/1992 → 01/01/9999  
Number of participants: 5  
Project participant: Nielsen, Sune Fallgaard (Intern)  
Mahadevan, Shankar (Intern)  
Bjerregaard, Tobias (Intern)  
Project Manager, organisational: Sparsø, Jens (Intern)  
Madsen, Jan (Intern)