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Publications:

A Controller for Dynamic Partial Reconfiguration in FPGA-Based Real-Time Systems
Publication: Research - peer-review › Article in proceedings – Annual report year: 2017

A resource-efficient network interface supporting low latency reconfiguration of virtual circuits in time-division multiplexing networks-on-chip
Publication: Research - peer-review › Journal article – Annual report year: 2017

Can Real-Time Systems Benefit from Dynamic Partial Reconfiguration?
Publication: Research - peer-review › Article in proceedings – Annual report year: 2017

High-level synthesis for reduction of WCET in real-time systems
Publication: Research - peer-review › Article in proceedings – Annual report year: 2017

Timing organization of a real-time multicore processor
Publication: Research - peer-review › Article in proceedings – Annual report year: 2017

An Area-Efficient TDM NoC Supporting Reconfiguration for Mode Changes
Publication: Research - peer-review › Article in proceedings – Annual report year: 2016

Argo: A Real-Time Network-on-Chip Architecture With an Efficient GALS Implementation
Publication: Research - peer-review › Journal article – Annual report year: 2015

Avionics Applications on a Time-Predictable Chip-Multiprocessor
Publication: Research - peer-review › Article in proceedings – Annual report year: 2016

Clock domain crossing modules for OCP-style read/write interfaces
Publication: Research › Report – Annual report year: 2016

Reconfiguration in FPGA-Based Multi-Core Platforms for Hard Real-Time Applications
Publication: Research - peer-review › Article in proceedings – Annual report year: 2016

State-based Communication on Time-predictable Multicore Processors
Publication: Research - peer-review › Article in proceedings – Annual report year: 2016
Time-Predictable Communication on a Time-Division Multiplexing Network-on-Chip Multicore
Publication: Research › Ph.D. thesis – Annual report year: 2016

Time-predictable Stack Caching
Publication: Research › Ph.D. thesis – Annual report year: 2016

An Asynchronous Time-Division-Multiplexed Network-on-Chip for Real-Time Systems
Publication: Research › Ph.D. thesis – Annual report year: 2015

Interfacing Hardware Accelerators to a Time-Division Multiplexing Network-on-Chip
Publication: Research - peer-review › Article in proceedings – Annual report year: 2015

Message Passing on a Time-predictable Multicore Processor
Publication: Research - peer-review › Article in proceedings – Annual report year: 2015

Models of Communication for Multicore Processors
Publication: Research - peer-review › Article in proceedings – Annual report year: 2015

T-CREST: Time-predictable multi-core architecture for embedded systems
Publication: Research - peer-review › Journal article – Annual report year: 2015

The Argo NOC: Combining TDM and GALS
Publication: Research - peer-review › Article in proceedings – Annual report year: 2015

A Loosely Synchronizing Asynchronous Router for TDM-Scheduled NOCs
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

A Metaheuristic Scheduler for Time Division Multiplexed Network-on-Chip
Publication: Research › Report – Annual report year: 2014

A Metaheuristic Scheduler for Time Division Multiplexed Network-on-Chip
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

Argo: A Time-Elastic Time-Division-Multiplexed NOC using Asynchronous Routers
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

A Time-predictable Memory Network-on-Chip
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

Open Core Protocol (OCP) Clock Domain Crossing Interfaces
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

Synthesis and Layout of an Asynchronous Network-on-Chip using Standard EDA Tools
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

A 65-nm CMOS Area Optimized De-synchronization Flow for sub-V_T Designs
Publication: Research - peer-review › Article in proceedings – Annual report year: 2013

An area-efficient network interface for a TDM-based Network-on-Chip
Publication: Research - peer-review › Article in proceedings – Annual report year: 2013
Current Trends in High-Level Synthesis of Asynchronous Circuits

Performance Analysis of a Hardware/Software-based Cache Coherence Protocol in Shared Memory MPSoCs

Synthesis of Topology Configurations and Deadlock Free Routing Algorithms for ReNoC-based Systems-on-Chip

A Reactive and Cycle-True IP Emulator for MPSoC Exploration

E-learning support for student's understanding of electronics

Network Traffic Generator Model for Fast Network-on-Chip Simulation

ReNoC: A Network-on-Chip Architecture with Reconfigurable Topology

A Scalable, Timing-Safe, Network-on-Chip Architecture with an Integrated Clock Distribution Method

Asynchronous design of Networks-on-Chip

A Traffic injection methodology with support for system-level synchronization

Custom Topology Generation for Network-on-Chip

Towards CDIO-based B.Eng. studies at the Technical University of Denmark

Simulation-based Modeling Frameworks for Networked Multi-processor System-on-Chip

The MANGO clockless network-on-chip: Concepts and implementation

A simple clockless Network-on-Chip for a commercial audio DSP chip

Implementation of Guaranteed Services in the MANGO Clockless Network-on-Chip
Packetizing OCP Transactions in the MANGO Network-on-Chip
Publication: Research - peer-review › Article in proceedings – Annual report year: 2006

Proceedings of ASYNC’2006 - 12th IEEE Intl. symposium on asynchronous circuits and systems
Publication: Research - peer-review › Book – Annual report year: 2006

Types for DSP Assembler Programs
Publication: Research › Ph.D. thesis – Annual report year: 2006

A Network Traffic Generator Model for Fast Network-on-Chip Simulation
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

An OCP Compliant Network Adapter for GALS-based SoC Design Using the MANGO Network-on-Chip
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

A Router Architecture for Connection-Oriented Service Guarantees in the MANGO Clockless Network-on-Chip
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

A Scheduling Discipline for Latency and Bandwidth Guarantees in Asynchronous Network-on-Chip
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

Behavioral synthesis of asynchronous circuits
Publication: Research › Ph.D. thesis – Annual report year: 2005

Modular SoC-Design using the MANGO clockless NoC (Invited talk)
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

Realistically Rendering SoC Traffic Patterns with Interrupt Awareness
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

A Channel Library for Asynchronous Circuit Design Supporting Mixed-Mode Modelling
Publication: Research - peer-review › Article in proceedings – Annual report year: 2004

A Low-Power Heterogeneous Multiprocessor Architecture for Audio Signal Processing
Publication: Research - peer-review › Journal article – Annual report year: 2004

Future Networks-on-Chip; will they be Synchronous or Asynchronous? (Invited talk)
Publication: Research - peer-review › Article in proceedings – Annual report year: 2004

Towards behavioral synthesis of asynchronous circuits - an implementation template targeting syntax directed compilation
Publication: Research - peer-review › Article in proceedings – Annual report year: 2004

Virtual Channel Designs for Guaranteeing Bandwidth in Asynchronous Network-on-chip
Publication: Research - peer-review › Article in proceedings – Annual report year: 2004

Compact beamforming in medical ultrasound scanners
Publication: Research › Ph.D. thesis – Annual report year: 2003

Low power digital signal processing
Publication: Research › Ph.D. thesis – Annual report year: 2003
The Synputer - A Novel MIMD Processor Targeting High Performance Low Power DSP Applications
Publication: Research - peer-review › Article in proceedings – Annual report year: 2003

Using SystemC to Model Asynchronous Communication at Different Levels of Abstraction
Publication: Research › Article in proceedings – Annual report year: 2003

A heterogeneous multi-core platform for low power signal processing in systems-on-chip
Publication: Research - peer-review › Article in proceedings – Annual report year: 2002

A Heterogenous Multi-Core Platform for Low Power Signal Processing
Publication: Research - peer-review › Article in proceedings – Annual report year: 2002

Embedded tutorial 1: Future Directions in Clocking Multi-Ghz Systems
Publication: Research - peer-review › Article in proceedings – Annual report year: 2002

High-level synthesis of asynchronous circuits from control data flow graph representations
Publication: Research › Article in proceedings – Annual report year: 2002

A heterogeneous multiprocessor architecture for low-power audio signal processing applications
Publication: Research - peer-review › Article in proceedings – Annual report year: 2001

Analysis of low-power SoC interconnection networks
Publication: Research - peer-review › Article in proceedings – Annual report year: 2001

Asynchronous circuit design - A tutorial
Publication: Research - peer-review › Book chapter – Annual report year: 2001

Principles of Asynchronous Circuit Design - A Systems Perspective
Publication: Research - peer-review › Book – Annual report year: 2001

Channel Abstraction and Statement Level Concurrency in VHDL++
Publication: Research - peer-review › Article in proceedings – Annual report year: 2000

Asynchronous Design using plain VHDL in a standard CAD-tool framework
Publication: Research › Article in proceedings – Annual report year: 1999

Designing Asynchronous Circuits for Low Power: An IFIR Filter: (Invited Paper)
Publication: Research - peer-review › Journal article – Annual report year: 1999

Proceedings of PATMOS'99: 9th Int. Workshop on Power and Timing Modeling, Optimization and Simulation
Publication: Research - peer-review › Book – Annual report year: 1999

Proceedings of PATMOS'99, 9th Int. Workshop on Power and Timing Modeling, Optimization and Simulation
Publication: Research - peer-review › Book – Annual report year: 1999

An 85 micro Watt Asynchronous Filter-Bank for a Digital Hearing Aid
Publication: Research › Article in proceedings – Annual report year: 1998

High Speed Frame Synchronization and Viterbi Decoding
Publication: Research - peer-review › Report – Annual report year: 1998
High Speed Frame Synchronization and Viterbi Decoding: Final Report
Publication: Research - peer-review › Report – Annual report year: 1998

Lavenergi kredsløb
Publication: Research › Journal article – Annual report year: 1998

Proceedings of PATMOS '98
Publication: Research - peer-review › Book – Annual report year: 1998

Proceedings of PATMOS'98, 8th Int. Workshop on Power and Timing Modeling, Optimization and Simulation
Publication: Research - peer-review › Book – Annual report year: 1998

The design of an asynchronous Tiny RISC TM/TR4101 microprocessor core
Publication: Research - peer-review › Article in proceedings – Annual report year: 1998

Compilation of lecture notes for "Summer School on Asynchronous Circuit Design", DTU, August 18-22
Publication: Education › Compendium/lecture notes – Annual report year: 1997

A low-power asynchronous data-path for a FIR filter bank
Publication: Research - peer-review › Article in proceedings – Annual report year: 1996

ACiD-WG workshop on asynchronous low-power VLSI
Publication: Research - peer-review › Report – Annual report year: 1994

ACiD-WG workshop on Asynchronous Low-Power VLSI, Lyngby, Denmark, April 11-12
Publication: Research - peer-review › Book – Annual report year: 1994

Low-power operation using self-timed circuits and adaptive scaling of the supply voltage
Publication: Research - peer-review › Article in proceedings – Annual report year: 1994

Low-power operation using self-timed circuits and adaptive scaling of the supply voltage
Publication: Research - peer-review › Journal article – Annual report year: 1994

Temporale forhold i synkrone integrerede kredsløb med 2-fase klok
Publication: Education › Compendium/lecture notes – Annual report year: 1994

Delay-insensitive Multi-ring Structures
Publication: Research - peer-review › Journal article – Annual report year: 1993

Design and performance analysis of delay insensitive multi-ring structures
Publication: Research - peer-review › Article in proceedings – Annual report year: 1993

Design of Self-timed Multipliers: A Comparison
Publication: Research - peer-review › Article in proceedings – Annual report year: 1993

Design and development of a very high speed Reed-Solomon encoder/decoder chip set: Architectural design report
Publication: Research - peer-review › Report – Annual report year: 1992

Design and development of a very high speed Reed-Solomon encoder/decoder chip set: Requirement analysis.
Publication: Research - peer-review › Report – Annual report year: 1992
Design and Performance Analysis of Delay-Insensitive Multi-Ring Structures
Publication: Research - peer-review › Report – Annual report year: 1992

Design of delay insensitive circuits using multi-ring structures
Publication: Research - peer-review › Article in proceedings – Annual report year: 1992

An area-efficient path memory structure for VLSI Implementation of high speed Viterbi decoders
Publication: Research - peer-review › Journal article – Annual report year: 1991

An area-efficient topology for VLSI implementation of Viterbi decoders and other shuffle-exchange type structures
Publication: Research - peer-review › Journal article – Annual report year: 1991

Design of a Fully Parallel Viterbi Decoder
Publication: Research - peer-review › Article in proceedings – Annual report year: 1991

Struktureret konstruktion af digitale ASIC's
Publication: Education › Compendium/lecture notes – Annual report year: 1991

An Area-Efficient Topology for VLSI Implementation of Viterbi Decoders and other Shuffle-Exchange Type Structures
Publication: Research - peer-review › Report – Annual report year: 1990

Experiences from the design of a large VLSI chip
Publication: Research - peer-review › Article in proceedings – Annual report year: 1990

A Fully Parallel VLSI-implementation of the Viterbi Decoding Algorithm
Publication: Research - peer-review › Report – Annual report year: 1989

A Fully Parallel VLSI-implementation of the Viterbi Decoding Algorithm
Publication: Research - peer-review › Report – Annual report year: 1989

Design and implementation of a full-custom single chip Viterbi decoder
Publication: Research - peer-review › Article in proceedings – Annual report year: 1989

Hardware Architecture of a Node for the LAN-DTH High Speed Token Ring
Publication: Research - peer-review › Article in proceedings – Annual report year: 1987

A POLYNET to VME-bus Interface Unit - Block diagram and principles of operation
Publication: Research - peer-review › Report – Annual report year: 1986

Hardware Architecture of a Node for the LAN-DTH High Speed Token Ring
Publication: Research - peer-review › Report – Annual report year: 1986

LAN-DTH - A Hierarchical Local Area Network based on a High Speed Optic Token Ring
Publication: Research - peer-review › Article in proceedings – Annual report year: 1986

Projects:

Real-Time Multi-Core Communication and Synchronization
Project: PhD
Real-Time Multicore Systems
Project: PhD

Real-Time Multicore Systems
Project: PhD

Dynamic Partial Reconfiguration in FPGA based Multi-core Real-time Embedded Systems
Project: PhD

Hardware/Software tradeoffs in Real-Time Multiprocessor Platforms
Project: PhD

Time-predictable VLIW Processor
Project: PhD

Asynchronous Network-on-Chip for Time-Predictable Multi-Core Embedded Systems
Project: PhD

Multi-objective Design Space Exploration for (re)-configurable heterogeneous Multi-ASIP SoC platforms
Project: PhD

Adaptability and Autonomy in Embedded Systems
Project: PhD

Models and Analyses for Embedded Systems Design
Project: PhD

Network-on-chip: Applikationer og topologioptimering
Project: PhD

Systemarkitekturer baseret på Network-on-Chip
Project: PhD

Asynkrone Network-on-Chip
Project: PhD

High performance low cost digital controlled power conversion technology
Project: PhD

Chip Area Interconnection Networks
Project: PhD

Intra-Chip Communication
Project: PhD

High-Level Synthesis of Asynchronous
Project: PhD

Integrated circuits in medical ultrasound
Project: PhD
Types for DSP Assembler Programs
Project: PhD

Low Power Digital Signal Processing
Project: PhD

PATMOS’98 workshop
Project

Center for Microinstruments (CfM)
Project

Thomas B. Thryge Center for Microinstruments
Project

Graduate School in Microelectronics
Project

Teknologiudvikling for mikroakruatorer
Project: PhD

Integreret hardware/software kode-generering i Co-design
Project: PhD

High Speed Frame Synchronization and Viterbi Decoding
Project

Testing Techniques for Self-Timed Circuits
Project: PhD

Kredsløbsteknikker for Asynkrone Systemer
Project: PhD

Designmetoder og teknikker for højhastighs VLSI-kredse
Project: PhD

Asynchronous Circuit Design
Project