Jan Madsen - DTU Orbit (15/01/2018)

Jan Madsen

Organisations

Deputy head of Department, head of section, Department of Informatics and Mathematical Modeling
04/07/2003 → 07/04/2016 Former
jan@imm.dtu.dk
VIP

Computer Science and Engineering
25/02/2012 → 18/02/2013 Former
VIP

Embedded Systems Engineering
25/02/2012 → 18/02/2013 Former
VIP

Associate Professor, Department of Information Technology
04/07/2003 → 07/04/2016 Former
jan@it.dtu.dk
VIP

Copenhagen Center for Health Technology
21/11/2015 → present
VIP

Professor, Section Head, Deputy Director, Department of Applied Mathematics and Computer Science
27/12/2012 → present
jama@dtu.dk
VIP

Embedded Systems Engineering
18/02/2013 → present
VIP

Publications:

Pin-count reduction for continuous flow microfluidic biochips
Microfluidic biochips are replacing the conventional biochemical analyzers integrating the necessary functions on-chip. We are interested in flow-based biochips, where a continuous flow of liquid is manipulated using integrated microvalves, controlled from external pressure sources via off-chip control pins. Recent research has addressed the physical design of such biochips. However, such research has so far ignored the pin-count, which rises with the increase in the number of microvalves. Given a biochip architecture and a biochemical application, we propose an algorithm for reducing the number of control pins required to run the application. The proposed algorithm has been evaluated on several biochips, including the AquaFlux biochip from Microfluidic Innovations LLC.

General information
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A systematic and practical method for selecting systems engineering tools
The complexity of many types of systems has grown considerably over the last decades. Using appropriate systems engineering tools therefore becomes increasingly important. Starting the tool selection process can be intimidating because organizations often only have a vague idea about what they need. The tremendous number of available tools makes it difficult to get an overview and identify the best choice. Selecting wrong tools due to inappropriate analysis can have severe impact on the success of the company. This paper presents a systematic method for selecting systems engineering tools based on thorough analyses of the actual needs and the available tools. Grouping needs into categories, allow us to obtain a comprehensive set of requirements for the tools. The entire model-based systems engineering discipline was categorized for a modeling tool case to enable development of a tool specification. Correlating requirements and tool capabilities, enables us to identify the best tool for single-tool scenarios or the best set of tools for multi-tool scenarios. In both scenarios, we use gap analysis to prevent selection of infeasible tools. We used the method to select a traceability tool that has been in successful operation since 2013 at GN Hearing. We further utilized the method to select a set of tools that we used on pilot cases at GN Hearing for modeling, simulating and formally verifying embedded systems.

General information
State: Published
A Top-down Approach to Genetic Circuit Synthesis and Optimized Technology Mapping

Genetic logic circuits are becoming popular as an emerging field of technology. They are composed of genetic parts of DNA and work inside a living cell to perform a dedicated boolean function triggered by the presence or absence of certain proteins or other species.

Co-Simulation of Cyber-Physical System with Distributed Embedded Control

Cyber-Physical Systems (CPS) are integrations of computation and physical processes, with distributed embedded computation units, connected by network, controlling and monitoring a physical plant. The development of physical components is essentially different from the object-oriented software of the computation units. A major challenge developing CPS, is the nonlinear interaction between the discrete domain of the computational units and the continuous domain of the physical process. Model based development of both discrete and continuous systems has significantly benefited from specialized modelling and simulation tools in each domain. However, to realize the full potential of CPS, the abstraction-level of models and simulation has to unify both computation and physical dynamics. A solution to this, is a so called co-simulation where the coupled problem is divided into sub-systems where each constituent model can be solved by its optimum tool/solver in a distributed manner. This enables domain expert to work in domain specific tools while being able to simulate the complete CPS in a holistic manner. This dissertation provides a solution for doing co-simulation of CPS with distributed embedded control. This research has been conducted in collaboration with MAN Diesel & Turbo (MD&T) using their CPS, consisting of a two-stroke low speed engine with a distributed engine control system, as case study. Adapting a distributed control system to enable co-simulation is not trivial. How the lower layers of the embedded system software has been adapted to enable a deterministic and temporally controlled simulation will be presented. This includes how multiple controllers are compiled to dynamic link libraries that can be executed in parallel by a main process. A method for controlling execution and time progression on each controller has been developed along with a scheduling and network communication solution. To enable co-simulation with tools for modelling physical dynamics, the Functional Mockup Interface (FMI) standard for co-simulation has been implemented in the control system simulation. The solutions presented are validated through a set co-simulation experiments using the MD&T engine control system and different physical dynamic modelling tools. During the research new applications and requirements to the co-simulation environment was discovered. In large organizations like MD&T, tools, platforms and architecture used by different departments often deviate, making co-simulation and model exchange difficult. In collaboration with the EU Horizon 2020
project; Integrated Tool-chain for the model based design of Cyber-Physical Systems (INTO-CPS), a distributed co-
simulation was made possible, that was able to co-simulate sub-systems of any architecture (32/64bit) and platform
(Windows/Linux). Furthermore, when developing safety critical CPS that include a Human Machine Interface (HMI), the
human interaction and cognitive assessment is of great importance. However, it is often difficult to obtain quantitative and
evidence based data on the human in the loop. With an extension to the co-simulation environment it is possible to
connect the control system simulation with the HMI in a hybrid co-simulation. In the hybrid co-simulation scenarios
requiring human interaction can be formulated and tracked. The collected data can be used for analyzing the system
applicability and intuitiveness, insuring correct and secure operation of MD&T engines. Validation and verification on
hardware and engine test-benches is a major part of the development cost at MD&T. With the possibility of simulating the
complete distributed control system, engineers are able to verify more of the component design before moving to the
hardware test-bench. Furthermore, by introducing co-simulation, engineers can investigate and validate the holistic system
dynamics during development before moving to the Engine test-bench and do model sharing between departments,
reducing redundant modelling efforts. This research provides a solution for doing co-simulation of CPS with distributed
control and proves that co-simulation can improve the development process, by reducing the amount of design and test
loops during the design phase, thereby reducing the overall verification and validation cost.

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Authors: Pedersen, N. (Intern), Madsen, J. (Intern)
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Distributed co-simulation of embedded control software with exhaust gas recirculation water handling system using INTO-
CPS
Engineering complex Cyber-Physical Systems, such as emission reduction control systems for large two-stroke engines,
require advanced modelling of both the cyber and physical aspects. Different tools are specialised for each of these
domains and a combination of tools validating different properties is often desirable. However, it is non-trivial to be able to
combine such different models of different constituent elements. In order to reduce the need for expensive tests on the
real system it is advantageous to be able to combine such heterogeneous models in a joint co-simulation in order to
reduce the overall costs of validation. This paper demonstrates how this can be achieved for a commercial system
developed by MAN Diesel & Turbo using a newly developed tool chain based on the Functional Mock-up Interface
standard for co-simulation supporting different operating systems. The generality of the suggested approach also enables
future scenarios incorporating constituent models supplied by sub-suppliers while protecting their Intellectual Property.

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Organisations: Copenhagen Center for Health Technology, Department of Applied Mathematics and Computer Science ,
Embedded Systems Engineering, Aarhus University, MAN Diesel & Turbo, MAN Diesel and Turbo SE
Authors: Pedersen, N. (Ekstern), Lausdahl, K. (Ekstern), Sanchez, E. V. (Ekstern), Larsen, P. G. (Ekstern), Madsen, J.
(Intern)
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Co-Simulation, Cyber-Physical-Systems, Distributed Simulation, Embedded Control System, Exhaust Gas Recirculation,
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Source: Scopus
Helbredstjek af dansk sundhedsteknologi: Sektorudviklingsrapport
Sådan kan samarbejde mellem industrien, universiteterne og sundhedsvæsenet skabe gode løsninger til forebyggelse, diagnostik, patientbehandling og rehabilitering

General information
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Organisations: Office for Innovation & Sector Services, Copenhagen Center for Health Technology, Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Center for Energy Resources Engineering, Scientific Computing, Department of Management Engineering, Technology and Innovation Management, Department of Electrical Engineering, Biomedical Engineering, Department of Micro- and Nanotechnology, Nano Bio Integrated Systems, Department of Photonics Engineering, Diode Lasers and LED Systems, Department of Energy Conversion and Storage, Electrofunctional materials, IT Service, National Space Institute, Innovation and Research-based consultancy, Department of Chemical and Biochemical Engineering, The Danish Polymer Centre, Office for Research and Relations, It-branchen, manjourn.dk
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Logic analysis and verification of n-input genetic logic circuits
Nature is using genetic logic circuits to regulate the fundamental processes of life. These genetic logic circuits are triggered by a combination of external signals, such as chemicals, proteins, light and temperature, to emit signals to control other gene expressions or metabolic pathways accordingly. As compared to electronic circuits, genetic circuits exhibit stochastic behavior and do not always behave as intended. Therefore, there is a growing interest in being able to analyze and verify the logical behavior of a genetic circuit model, prior to its physical implementation in a laboratory. In this paper, we present an approach to analyze and verify the Boolean logic of a genetic circuit from the data obtained through stochastic analog circuit simulations. The usefulness of this analysis is demonstrated through different case studies illustrating how our approach can be used to verify the expected behavior of an n-input genetic logic circuit.

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Methods and Tools for the Analysis, Verification and Synthesis of Genetic Logic Circuits,

Synthetic biology has emerged as an important discipline in which engineers and biologists are working together to design new and useful biological systems composed of genetic circuits. The purpose of developing genetic circuits is to carry out desired logical functions inside a living cell. This usually requires simulating the mathematical models of these genetic circuits and perceive whether or not the circuit behaves appropriately. Furthermore, synthetic biology utilizes the concepts from electronic design automation (EDA) of abstraction and automated construction to generate genetic circuits with the aim to reduce the in-vitro (wet-lab) experiments. To address this, several automated tools have been developed to improve the process of genetic design automation (GDA) with different capabilities. This thesis attempts to contribute to the advancement of GDA tools by introducing capabilities which we believe that no other existing GDA tools support. First, we introduce a user-friendly simulation tool, called D-VASim, which allows user to perform virtual laboratory experimentation by dynamically interacting with the model during runtime. This dynamic interaction with the model gives user a feeling of being in the lab performing wet-lab experiments virtually. This tool allows users to perform both deterministic and stochastic simulations. Next, this dissertation introduces a methodology to perform timing analyses of genetic logic circuits, which allows user to analyze the threshold value and propagation delays of genetic logic circuits. In this thesis, it has been demonstrated, through in-silico experimentation, that the threshold value and propagation delay plays a vital role in the correct functioning of genetic circuit. It has also been shown how some circuit parameters effect these two important design characteristics. This thesis also introduces an automated approach to analyze the behavior of genetic logic circuits from the simulation data. With this capability, the boolean logic of complex genetic circuits can be analyzed and/or verified automatically. It is also shown in this thesis that the proposed approach is effective to determine the variation in the behavior of genetic circuits when the circuit’s parameters are changed.

In addition, the thesis also attempts to propose a synthesis and technology mapping tool, called GeneTech, for genetic circuits. It allows users to construct a genetic circuit by only specifying its behavior in the form of boolean expression. For technology mapping, this tool uses a gates library developed by the collective efforts of the researchers at MIT and Boston universities. It is shown experimentally that the tool is able to provide all feasible solutions, containing different genetic components, to achieve the specified boolean behavior. Finally, it has been shown how D-VASim can be used along with other tools for useful purposes, like model checking. With respect to this, an experimental workflow is proposed for checking genetic circuits using the statistical model checking (SMC) utility of the Uppaal tool and the timing analysis capability of D-VASim. We further demonstrated how the reliability of a simulation can be improved by using the real parameter values. In this regard, the relationship between the simulation parameters and real parameters have been derived.

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Authors: Baig, H. (Intern), Madsen, J. (Intern), Pop, P. (Intern)
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Paper-Based Digital Microfluidic Chip for Multiple Electrochemical Assay Operated by a Wireless Portable Control System
The printing and modular fabrication of a paper-based active microfluidic lab on a chip implemented with electrochemical sensors (ECSs) is developed and integrated on a portable electrical control system. The electrodes of a chip plate for active electrowetting actuation of digital drops and an ECS for multiple analysis assays are fabricated by affordable printing techniques. For enhanced sensitivity of the sensor, the working electrode is modified through the electrochemical method, namely by reducing graphene with voltammetry and coating gold nanoparticles by amperometry. Detachable sensor and
absorber modules are assembled modularly on an open chip plate, forming various novel hybridized open–closed chip formats. By varying the coupled or decoupled sensor modules, excellent detection of three diagnostic biological molecules is demonstrated (glucose, dopamine, and uric acid in human serum). With a newly designed portable power supply and wireless control system, the active paper-based chip platform can be utilized as an advanced point-of-care device for multiple assays in digital microfluidics.

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**Scheduling and Fluid Routing for Flow-Based Microfluidic Laboratories-on-a-Chip**
Microfluidic laboratories-on-chip (LoCs) are replacing the conventional biochemical analyzers and are able to integrate the necessary functions for biochemical analysis on-chip. There are several types of LoCs, each having its advantages and limitations. In this paper we are interested in flow-based LoCs, in which a continuous flow of liquid is manipulated using integrated microvalves. By combining several microvalves, more complex units, such as micropumps, switches, mixers and multiplexers, can be built. We consider that the architecture of the LoC is given, and we are interested in synthesizing an implementation, consisting of the binding of operations in the application to the functional units of the architecture, the scheduling of operations and the routing and scheduling of the fluid flows, such that the application completion time is minimized. To solve this problem, we propose a List Scheduling based Application Mapping (LSAM) framework and evaluate it by using real-life as well as synthetic benchmarks. When biochemical applications contain fluids that may adsorb on the substrate on which they are transported, the solution is to use rinsing operations for contamination avoidance. Hence, we also propose a rinsing heuristic, which has been integrated in the LSAM framework.

**General information**
State: Accepted/In press
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, University of California at Riverside
Authors: Minhass, W. H. (Intern), McDaniel, J. (Ekstern), Raagaard, M. L. (Intern), Brisk, P. (Ekstern), Pop, P. (Intern), Madsen, J. (Intern)
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Simulation Approach for Timing Analysis of Genetic Logic Circuits

Constructing genetic logic circuits is an application of synthetic biology in which parts of the DNA of a living cell are engineered to perform a dedicated Boolean function triggered by an appropriate concentration of certain proteins or by different genetic components. These logic circuits work in a manner similar to electronic logic circuits, but they are much more stochastic and hence much harder to characterize. In this article, we introduce an approach to analyze the threshold
value and timing of genetic logic circuits. We show how this approach can be used to analyze the timing behavior of single and cascaded genetic logic circuits. We further analyze the timing sensitivity of circuits by varying the degradation rates and concentrations. Our approach can be used not only to characterize the timing behavior but also to analyze the timing constraints of cascaded genetic logic circuits, a capability that we believe will be important for design automation in synthetic biology.

**General information**

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Organisations: Embedded Systems Engineering, Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Copenhagen Center for Health Technology
Authors: Baig, H. (Intern), Madsen, J. (Intern)
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**Synthesis of on-chip control circuits for mVLSI biochips**

Microfluidic VLSI (mVLSI) biochips help perform biochemistry at miniaturized scales, thus enabling cost, performance and other benefits. Although biochips are expected to replace biochemical labs, including point-of-care devices, the off-chip pressure actuators and pumps are bulky, thereby limiting them to laboratory environments. To address this issue, researchers have proposed methods to reduce the number of off-chip pressure sources, through integration of on-chip pneumatic control logic circuits fabricated using three-layer monolithic membrane valve technology. Traditionally, mVLSI biochip physical design was performed assuming that all of the control logic is off-chip. However, the problem of mVLSI biochip physical design changes significantly, with introduction of on-chip control, since along with physical synthesis, we also need to (i) perform on/off-chip control partitioning, (ii) on-chip control circuit design and (iii) the integration of on-chip control in the placement and routing design tasks. In this paper we present a design methodology for logic synthesis and physical synthesis of mVLSI biochips that use on-chip control. We show how the proposed methodology can be successfully applied to generate biochip layouts with integrated on-chip pneumatic control.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Xilinx Asia Pacific, Singapore, sgp, Technical University of Denmark
Authors: Potluri, S. (Ekstern), Schneider, A. R. (Intern), Hørslev-Petersen, M. (Ekstern), Pop, P. (Intern), Madsen, J. (Intern)
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System-Level Sensitivity Analysis of SiNW-bioFET-Based Biosensing Using Lockin Amplification

Although Silicon Nanowire biological Field-Effect Transistors (SiNW-bioFETs) have steadily demonstrated their ability to detect biological markers at ultra-low concentration, they have not yet translated into routine diagnostics applications. One of the challenges inherent to the technology is that it requires an instrumentation capable of recovering ultra-low signal variations from sensors usually designed and operated in a highly-resistive configuration. Often overlooked, the SiNW-bioFET/instrument interactions are yet critical factors in determining overall system biodetection performances.

Here, we carry out for the first time the system-level sensitivity analysis of a generic SiNW-bioFET model coupled to a custom-design instrument based on the lock-in amplifier. By investigating a large parametric space spanning over both sensor and instrumentation specifications, we demonstrate that systemwide investigations can be instrumental in identifying the design trade-offs that will ensure the lowest Limits-of-Detection. The generic character of our analytical model allows us to elaborate on the most general SiNW-bioFET/instrument interactions and their overall implications on detection performances. Our model can be adapted to better match specific sensor or instrument designs to either ensure that ultra-high sensitivity SiNW-bioFETs are coupled with an appropriately sensitive and noise-rejecting instrumentation, or to best tailor SiNW-bioFET design to the specifications of an existing instrument.
Taming Living Logic using Formal Methods

One of the goals of synthetic biology is to build genetic circuits to control the behavior of a cell for different application domains, such as medical, environmental, and biotech. During the design process of genetic circuits, biologists are often interested in the probability of a system to work under different conditions. Since genetic circuits are noisy and stochastic in nature, the verification process becomes very complicated. The state space of stochastic genetic circuit models is usually too large to be handled by classical model checking techniques. Therefore, the verification of genetic circuit models is usually performed by the statistical approach of model checking. In this work, we present a workflow for checking genetic circuit models using a stochastic model checker (Uppaal) and a stochastic simulator (D-VASim). We demonstrate with experimentations that the proposed workflow is not only sufficient for the model checking of genetic circuits, but can also be used to design the genetic circuits with desired timings.
Hearing systems have evolved over many years from simple mechanical devices (horns) to electronic units consisting of microphones, amplifiers, analog filters, loudspeakers, batteries, etc. Digital signal processors replaced analog filters to provide better performance and new features. Central processors were added to provide many functions for monitoring and controlling other parts of the devices. Hearing systems have thus evolved into complex embedded system. Radio systems were added to allow hearing aids to communicate with accessories, auxiliary equipment, third-party products, etc. Many new features are enabled by such radio communication. Monitoring and controlling hearing aids from remote control devices or smart phones have been incorporated into several products. Direct audio streaming between hearing aids and dedicated streaming devices or smart phones is possible with some products. Also emerging are advanced features that are based on interactions with internet services, clouds, etc. Hearing systems are thus evolving into large and complex smart systems. Designing complex embedded systems or large smart systems are notoriously difficult. Many systems are still developed using document-based methods, where requirements and proposed architecture are described textually with the addition of a few figures and tables. Such documents cannot be subjected to testing, so it is impossible to predict the functionality and performance or even feasibility of the intended systems. Replacing documents with models have several advantages. Models can be simulated and analyzed such that functionality and performance can be predicted before any parts have been built. Potential flaws in the specification can therefore be corrected in early phases, which may reduce development effort and costs. This thesis concerns methods for identifying, selecting and implementing tools for various aspects of model-based systems engineering. A comprehensive method was proposed that include several novel steps such as techniques for analyzing the gap between requirements and tool capabilities. The method was verified with good results in two case studies for selection of a traceability tool (single-tool scenario) and a set of modeling tools (multi-tool scenarios). Models must be subjected to testing to allow engineers to predict functionality and performance of systems. Test-first strategies are known to produce good results in software development. This thesis concerns methods for test-driven modeling of hearing systems. A method is proposed for test-driven modeling of embedded systems of medium complexity. It utilizes formal model checking to guarantee functionality and performance. Test-driven design space exploration is enabled by using statistical model checking to obtain estimates that are verified formally at the final stages of the method. The method was applied with good results to a case study, where two solutions to a design problem were developed and verified. Feasible ranges for critical parameters were identified. Both solution conformed to all requirements. Smart systems are typically too large and complex to be verified by formal model checking, and the research showed that statistical model checking in its current form cannot be used for verifying such systems. A new method is therefore proposed for test-driven modeling of smart systems. The method uses formal verification of basic interactions. Simulations are used for verifying the overall system. To predict performance for scenarios that are too large to be simulated, the method uses mathematical forecasting based on simulating series of smaller scenarios, fitting simulation results to estimator functions, and extrapolating beyond the simulated data set. Mathematical forecasting allowed us to predict the performance of system scenarios that were much too large to be simulated. Such performance estimates may be somewhat imprecise but are nevertheless valuable because they provide answers that cannot be obtained otherwise. The research has thus proposed and verified methods for selecting modeling tools and for test-driven systems modeling for the benefit of GN Hearing and other organizations involved in development of complex embedded systems of large smart systems.
Test-driven modeling and development of cloud-enabled cyber-physical smart systems

Embedded products currently tend to evolve into large and complex smart systems where products are enriched with services through clouds and other web technologies. The complex characteristics of smart systems make it very difficult to guarantee functionality, safety, security and performance. Using test-driven modeling (TDM) is likely to be the best way to design smart systems such that these qualities are ensured. However, the TDM methods that are applied to development of simpler systems do not scale to smart systems because the modeling technologies cannot handle the complexity and size of the systems. In this paper, we present a method for test-driven modeling that scales to very large and complex systems. The method uses a combination of formal verification of basic interactions, simulations of complex scenarios, and mathematical forecasting to predict system behavior and performance. We utilized the method to analyze, design and develop various scenarios for a cloud-enabled medical system. Our approach provides a versatile method that may be adapted and improved for future development of very large and complex smart systems in various domains.

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Volume management for fault-tolerant continuous-flow microfluidics
Recent advancements in microfluidic biochips allow for easier and faster design and fabrication of increasingly complex biochips to replace conventional laboratories. A roadblock in the deployment of biochips however is their low reliability. Physical defects can be introduced during the fabrication process, and may lead to failure of the biochemical application. This can be costly because of the reduced manufacturing yield, the need to redo lengthy experiments, using expensive reagents, and can be safety-critical, e.g., in case of a cancer misdiagnosis. Researchers have started to propose fault models and test techniques for continuous flow biochips. Six typical defects: Block, leak, misalignment, faulty pumps, degradation of valves and dimensional errors have been identified. The resulting faults can be abstracted into blocks and leaks for simplicity. Both fault types can occur in the control-as well as the flow channel, some common causes being environmental particles, imperfections in molds or bubbles in the PDMS gel. While some faults may be detected before the execution of an application by introducing a test run, other faults occur only during runtime as a result of deterioration or caused by the applied pressure. If such a fault is detected during runtime, e.g. with a CCD camera, we propose a just in time solution that calculates and assigns fluid volumes to alternate components and routes allowing for the completion of the application despite the occurring fault.

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Waste-aware fluid volume assignment for flow-based microfluidic biochips

Microfluidic biochips are replacing the conventional biochemical analysers integrating the necessary functions on-chip. We are interested in Flow-Based Microfluidic Biochips (FBMB), where a continuous flow of liquid is manipulated using integrated microvalves. Using microvalves and channels, more complex Fluidic Units (FUs) such as switches, micropumps, mixers and separators can be constructed. When running a biochemical application on a FBMB, fluid volumes are dispensed from input reservoirs and used by the FUs. Given a biochemical application and a biochip, we are interested in determining the fluid volume assignment for each operation of the application, such that the FUs volume requirements are satisfied, while over- and underflow are avoided and the total volume of fluid used is minimized. We propose an algorithm for this fluid assignment problem. Compared to previous work, our method is able to minimize the fluid consumption through optimal fluid assignment and reuse of fluid waste. Due to the algorithm's low complexity, fluid requirements can also be calculated during runtime for error recovery or statically unknown cases.

A Pin-Count Reduction Algorithm for Flow-Based Microfluidic Biochips

Microfluidic biochips are replacing the conventional biochemical analyzers integrating the necessary functions on-chip. We are interested in flow-based biochips, where a continuous flow of liquid is manipulated using integrated microvalves, controlled from external pressure sources via off-chip control pins. Recent research has addressed the physical design of such biochips. However, such research has so far ignored the pin-count, which rises with the increase in the number of microvalves. Given a biochip architecture and a biochemical application, we propose an algorithm for reducing the number of control pins required to run the application. The proposed algorithm has been evaluated using several benchmarks.
D-VASim: An Interactive Virtual Laboratory Environment for the Simulation and Analysis of Genetic Circuits

Simulation and behavioral analysis of genetic circuits is a standard approach of functional verification prior to their physical implementation. Many software tools have been developed to perform in silico analysis for this purpose, but none of them allow users to interact with the model during runtime. The runtime interaction gives the user a feeling of being in the lab performing a real world experiment. In this work, we present a user-friendly software tool named D-VASim (Dynamic Virtual Analyzer and Simulator), which provides a virtual laboratory environment to simulate and analyze the behavior of genetic logic circuit models represented in an SBML (Systems Biology Markup Language). Hence, SBML models developed in other software environments can be analyzed and simulated in D-VASim. D-VASim offers deterministic as well as stochastic simulation; and differs from other software tools by being able to extract and validate the Boolean logic from the SBML model. D-VASim is also capable of analyzing the threshold value and propagation delay of a genetic circuit model.
D-VASim: A Software Tool to Simulate and Analyze Genetic Logic Circuits

The Challenge:
Creating a software tool for the simulation and analysis of genetic logic circuits to help researchers performing wet lab experiments virtually, because the manual process of wet lab experimentation of genetic logic circuits is time consuming and a challenging task for early-stage researchers with limited experience in the field of biology.

The Solution:
Using LabVIEW to develop a user-friendly simulation tool named Dynamic Virtual Analyzer and Simulator (D-VASim), which is the first software tool in the domain of synthetic biology that provides a virtual laboratory environment to perform run-time interactive simulation and analysis of genetic logic circuits.

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Evolvable Smartphone-Based Platforms for Point-Of-Care In-Vitro Diagnostics Applications
The association of smart mobile devices and lab-on-chip technologies offers unprecedented opportunities for the emergence of direct-to-consumer in vitro medical diagnostics applications. Despite their clear transformative potential, obstacles remain to the large-scale disruption and long-lasting success of these systems in the consumer market. For instance, the increasing level of complexity of instrumented lab-on-chip devices, coupled to the sporadic nature of point-of-care testing, threatens the viability of a business model mainly relying on disposable/consumable lab-on-chips. We argued recently that system evolvability, defined as the design characteristic that facilitates more manageable transitions between system generations via the modification of an inherited design, can help remedy these limitations. In this paper, we discuss how platform-based design can constitute a formal entry point to the design and implementation of evolvable smart device/lab-on-chip systems. We present both a hardware/software design framework and the implementation details of a platform prototype enabling at this stage the interfacing of several lab-on-chip variants relying on current- or impedance-based biosensors. Our findings suggest that several change-enabling mechanisms implemented in the higher abstraction software layers of the system can promote evolvability, together with the design of change-absorbing hardware/software interfaces. Our platform architecture is based on a mobile software application programming interface coupled to a modular hardware accessory. It allows the specification of lab-on-chip operation and post-analytic functions at the mobile software layer. We demonstrate its potential by operating a simple lab-on-chip to carry out the detection of dopamine using various electroanalytical methods.

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Evolvable Smartphone-Based Point-of-Care Systems For In-Vitro Diagnostics
Recent developments in the life-science -omics disciplines, together with advances in micro- and nanoscale technologies offer unprecedented opportunities to tackle some of the major healthcare challenges of our time. Lab-on-Chip technologies coupled with smart-devices in particular, constitute key enablers for the decentralization of many in-vitro medical diagnostics applications to the point-of-care, supporting the advent of a preventive and personalized medicine. Although the technical feasibility and the potential of Lab-on-Chip/smart-device systems is repeatedly demonstrated, direct-to-consumer applications remain scarce. This thesis addresses this limitation. After identifying system evolvability as a key enabler to the adoption and long-lasting success of next-generation point-of-care systems by favoring the integration
of new technologies, streamlining the reengineering efforts for system upgrades and limiting the risk of premature system obsolescence. Among possible strategies, platform-based design represents a particularly suitable entry point to the development of evolvable systems. One necessary condition is for change-absorbing and change-enabling mechanisms to be incorporated in the platform architecture at initial design-time. Important considerations arise as to where in Lab-on-Chip/smart-device platforms can these mechanisms be integrated, and how to implement them. Our investigation revolves around the silicon-nanowire biological field effect transistor, a promising biosensing technology for the detection of biological analytes at ultra low concentrations. We discuss extensively the sensitivity and instrumentation requirements set by the technology before we present the design and implementation of an evolvable smartphone-based platform capable of interfacing lab-on-chips embedding such sensors. We elaborate on the implementation of various architectural patterns throughout the platform and present how these facilitated the evolution of the system towards one accommodating for electrochemical sensing. Model-based development was undertaken throughout the engineering process. A formal SysML system model fed our evolvability assessment process. We introduce, in particular, a model-based methodology enabling the evaluation of modular scalability: the ability of a system to scale the current value of one of its specification by successively reengineering targeted system modules. The research work presented in this thesis provides a roadmap for the development of evolvable point-of-care systems, including those targeting direct-to-consumer applications. It extends from the early identification of anticipated change, to the assessment of the ability of a system to accommodate for these changes. Our research should thus interest industrials eager not only to disrupt, but also to last in a shifting socio-technical paradigm.

General information
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Organisations: Department of Management Engineering, Engineering Systems, Department of Micro- and Nanotechnology, Nano Bio Integrated Systems
Authors: Patou, F. (Intern), Svendsen, W. E. (Intern), Dimaki, M. (Intern), Madsen, J. (Intern)
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FMI for Co-Simulation of Embedded Control Software
Increased complexity of cyber-physical systems within the maritime industry demands closer cooperation between engineering disciplines. The functional mockup interface (FMI) is an initiative aiding cross-discipline interaction by providing a widely accepted standard for model exchange and co-simulation. The standard is supported by a number of modelling tools. However, to implement it on an existing platform requires adaptation. This paper investigates how to adapt the software of an embedded control system to comply with the FMI for co-simulation standard. In particular, we suggest a way of advancing the clock of a real time operating system (RTOS), by overwriting the idle thread and waiting for a signal to start execution until return to idle. This approach ensures a deterministic and temporal execution of the simulation across multiple nodes. As proof of concept, a co-simulation is conducted, showing that the control system of an SCR (selective catalyst reduction) emission reduction system can be packed in a functional mockup unit (FMU) and co-simulated with a physical model, built in Ptolemy II. Results show that FMI can be used for co-simulation of an embedded SCR control software and for control software development.

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Authors: Pedersen, N. (Intern), Bojsen, T. (Ekstern), Madsen, J. (Intern), Vejlgaard-Laursen, M. (Ekstern)
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Microfluidic Very Large Scale Integration (VLSI): Modeling, Simulation, Testing, Compilation and Physical Synthesis

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Model-Based Evaluation Of System Scalability: Bandwidth Analysis For Smartphone-Based Biosensing Applications

Scalability is a design principle often valued for the engineering of complex systems. Scalability is the ability of a system to change the current value of one of its specification parameters. Although targeted frameworks are available for the evaluation of scalability for specific digital systems, methodologies enabling scalability analysis of multidomain, complex systems, are still missing. In acknowledgment of the importance for complex systems to present the ability to change or evolve, we present in this work a system-level model-based methodology allowing the multidisciplinary parametric evaluation of scalability. Our approach can be used to determine how a set of limited changes to targeted system modules could affect design specifications of interest. It can also help predict and trace system bottlenecks over several product generations, offering system designers the chance to to better plan re-engineering efforts for scaling a system specification efficaciously.

We demonstrate the value of our methodology by investigating a smartphone-based biosensing instrumentation platform. Specifically, we carry out scalability analysis for the system’s bandwidth specification: the maximum analog voltage waveform excitation frequency the system could output while allowing continuous acquisition and wireless streaming of bioimpedance measurements. We rely on several SysML modelling tools, including dependency matrices, as well as a fault-detection Simulink Stateflow executable model to conclude on how the successive re-engineering of 5 independent system modules, from the replacement of a wireless Bluetooth interface, to the revision of the ADC sample-and-hold operation could help increase system bandwidth.

Smartphone-based biosensing platform evolution: implementation of electrochemical analysis capabilities

Lab-on-Chip technologies offer great opportunities for the democratization of in-vitro medical diagnostics to the consumer-market. Despite the limitations set by the strict instrumentation and control requirements of certain families of these devices, new solutions are emerging. Smartphones now routinely demonstrate their potential as an interface of choice for operating complex, instrumented Lab-on-Chips. The sporadic nature of home-based in-vitro medical diagnostics testing calls for the development of systems capable of evolving with new applications or new technologies for Lab-on-Chip devices. We present in this work how we evolved the first generation of a smartphone/Lab-on-Chip platform designed for evolvability. We demonstrate how reengineering efforts can be confined to the mobile-software layer and illustrate some of the benefits of building evolvable systems. We implement electrochemical capabilities on our platform prototype and carry out cyclic voltammetry to measure dopamine concentrations over several orders of magnitude.
Synthesis of Application-Specific Fault-Tolerant Digital Microfluidic Biochip Architectures

Digital microfluidic biochips (DMBs) are microfluidic devices that manipulate droplets on an array of electrodes. Microfluidic operations, such as transport, mixing, and split, are performed on the electrode array to perform a biochemical application. All previous work assumes that the DMB architecture is given and most approaches consider a rectangular shape for the electrode array. However, nonrectangular application-specific architectures are common in practice. Hence, in this paper, we propose an approach to the synthesis of application-specific architectures, such that the cost of the architecture is minimized and the timing constraints of the biochemical application are satisfied. DMBs can be affected by permanent faults, which may lead to the failure of the biochemical application. Our approach introduces redundant electrodes to synthesize fault-tolerant architectures aiming at increasing the yield of DMBs. We have used a tabu search metaheuristic for this architecture synthesis problem. We have proposed a technique to evaluate the architecture alternatives visited during the search, in terms of their impact on the timing constraints of the application. The proposed architecture synthesis approach has been evaluated using several benchmarks.
Timing Analysis of Genetic Logic Circuits using D-VASim

A genetic logic circuit is a gene regulator network implemented by re-engineering the DNA of a cell, in order to control gene expression or metabolic pathways, through a logic combination of external signals, such as chemicals or proteins. As for electronic logic circuits, timing and propagation delay analysis may play a very significant role in the designing of genetic logic circuits. In this demonstration, we present the capability of D-VASim (Dynamic Virtual Analyzer and Simulator) to perform the timing and propagation delay analysis of genetic logic circuits. Using D-VASim, the timing and propagation delay analysis of single as well as cascaded genetic logic circuits can be performed. D-VASim allows user to change the circuit parameters during runtime simulation to observe its effect on the circuit’s timing behavior. The results obtained from D-VASim can be used not only to characterize the timing behavior of genetic logic circuits but also to analyze the timing constraints of cascaded genetic logic circuits.
A Probabilistic Approach for the System-Level Design of Multi-ASIP Platforms

Application Specific Instruction-set Processors (ASIPs) offer a good trade off between performance and flexibility when compared to general purpose processors or ASICs. Additionally, multiple ASIPs can be included in a single platform and they allow the generation of customized heterogeneous MPSoC with a relatively short time-to-market. While there are several commercial tools for the design of a single ASIP, there is still a lack of automation in the design of multi-ASIP platforms.

In this thesis we consider multi-ASIP platforms for real-time applications. Each ASIP is designed to run a specific group of tasks that we identify as a task cluster. With real-time applications, to decide how the tasks should be clustered, we perform a schedulability analysis of the system to verify if the deadlines of the applications can be met. However, to run a schedulability analysis, we need to know the WCET of each task that is available only after an ASIP is designed. Therefore, there is a circular dependency between the definition of the task clusters and the impossibility of defining them without knowing the WCET of the tasks as the ASIPs have not been defined yet.

Many approaches available in the literature break this circular dependency considering predefined task clusters or considering a small set of micro-architecture configurations for each ASIP. We propose an alternative approach that uses a probabilistic model to consider the design space of all possible micro-architecture configurations. We introduce a system-level Design Space Exploration (DSE) for the very early phases of the design that automatizes part of the multi-ASIP design flow. Our DSE is responsible for assigning the tasks to the different ASIPs exploring different platform alternatives. We perform a schedulability analysis for each solution to determine which one has the highest chances of meeting the deadlines of the applications and that should be considered in the next stages of the multi-ASIP design flow.

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A Smart Mobile Lab-on-Chip-Based Medical Diagnostics System Architecture Designed For Evolvability

Unprecedented knowledge levels in life sciences along with technological advances in micro- and nanotechnologies and microfluidics have recently conditioned the advent of Lab-on-Chip (LoC) devices for In-Vitro Medical Testing (IVMT). Combined with smart-mobile technologies, LoCs are pervasively giving rise to opportunities to better diagnose disease, predict and monitor personalised treatment efficacy, or provide healthcare decision-making support at the Point-of-Care (PoC). Although made increasingly available to the consumer market, the adoption of LoC-based PoC In-Vitro Medical Testing (IVMT) systems is still in its infancy. This attrition partly pertains to the intricacy of designing and developing complex systems, destined to be used sporadically, in a fast-pace evolving technological paradigm. System evolvability is therefore key in the design process and constitutes the main motivation for this work.

We introduce a smart-mobile and LoC-based system architecture designed for evolvability. By propagating LoC programmability, instrumentation, and control tools to the high-level abstraction smart-mobile software layer, our architecture facilitates the realisation of new use-cases and the accommodation for incremental LoC-technology developments. We demonstrate these features with an implementation allowing the interfacing of LoCs embedding current- or impedance-based biosensors such as Silicon Nanowire Field Effect Transistors (SiNW-FETs) or electrochemical transducers. Structural modifications of these LoCs or changes in their specific operation may be addressed by the sole reengineering of the mobile software layer, minimising system upgrade development and validation costs and efforts.

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Organisations: Department of Micro- and Nanotechnology, Nano Bio Integrated Systems, Center for Bachelor of Engineering Studies, Afdelingen for El-teknologi, Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Design of Mixed-Criticality Applications on Distributed Real-Time Systems

A mixed-criticality system implements applications of different safety-criticality levels onto the same platform. In such cases, the certification standards require that applications of different criticality levels are protected so they cannot influence each other. Otherwise, all tasks have to be developed and certified according to the highest criticality level, dramatically increasing the development costs. In this thesis we consider mixed-criticality real-time applications implemented on distributed partitioned architectures.

Partitioned architectures use temporal and spatial separation mechanisms to ensure that applications of different criticality levels do not interfere with each other. With temporal partitioning, each application is allowed to run only within predefined time slots, allocated on each processor. The sequence of time slots for all the applications on a processor are grouped within a Major Frame, which is repeated periodically. Each partition can have its own scheduling policy; we have considered non-preemptive static cyclic scheduling and fixed-priority preemptive scheduling policies. We assume that the communication network implements the TTEthernet protocol, which supports Time-Triggered (TT) messages transmitted based on static schedule tables, Rate Constrained (RC) messages with bounded end-to-end delay, and Best-Effort (BE) messages, for which no timing guarantees are provided. TTEthernet offers spatial separation for mixed-criticality messages through the concept of virtual links, and temporal separation, enforced through schedule tables for TT messages and bandwidth allocation for RC messages.

The objective of this thesis is to develop methods and tools for distributed mixed-criticality real-time systems. At the processor level, we are interested to determine (i) the mapping of tasks to processors, (ii) the assignment of tasks to partitions, (iii) the decomposition of tasks into redundant lower criticality tasks, (iv) the sequence and size of the partition time slots on each processor and (v) the schedule tables, such that all the applications are schedulable and the development and certification costs are minimized. We have proposed Simulated Annealing and Tabu Search metaheuristics to solve these optimization problems. The proposed algorithms have been evaluated using several benchmarks.

At the communication network level, we are interested in the design optimization of TTEthernet networks used to transmit mixed-criticality messages. Given the set of TT and RC messages, and the topology of the network, we are interested to optimize (i) the packing of messages in frames, (ii) the assignment of frames to virtual links, (iii) the routing of virtual links and (iv) the TT static schedules, such that all frames are schedulable and the worst-case end-to-end delay of the RC messages is minimized. We have proposed a Tabu Search-based metaheuristic for this optimization problem.

The proposed algorithm has been evaluated using several benchmarks. The optimization approaches have also been evaluated using realistic aerospace case studies. In this context, we have shown how to extend the proposed optimization frameworks to also take into account quality of service constraints. For TTEthernet networks, we have also proposed a topology selection method to reduce the cost of the architecture.
D-VASim: Dynamic Virtual Analyzer and Simulator for Genetic Circuits

A genetic circuit represents a gene regulator network that is triggered by a combination of external signals, such as chemicals, proteins, light or temperature, to emit signals to control gene expression or metabolic pathways accordingly. In order to match the intended behaviour, genetic circuits are either assembled from a standard library of well-defined genetic gates or from parts of an available library, for instance, BioBricks. The obtained behavior can be validated through in-silico analysis, solving reaction kinetics using ordinary differential equations (ODEs) or by stochastic simulation, with the aim to reduce the number of required in-vitro experiments.

We present a behavioural simulation and analysis tool that allows the biologist to carry out virtual lab experiments as an interactive process during simulation of the genetic circuit, rather than a batch process, which is current practice. We believe that this increases the insights gained from the analysis and allows for exploring more parameters in an intuitive manner.

Fault-Tolerant Digital Microfluidic Biochips: Compilation and Synthesis

Fault-Tolerant Digital Microfluidic Biochips: Compilation and Synthesis

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Introduction
This chapter presents an introduction to the microfluidics field and microfluidic biochips. We discuss the main fluid propulsion principles used by modern microfluidic platforms, with a focus on "digital" microfluidic biochips, which are the topic of this book. Digital microfluidic biochips manipulate the fluids as small "droplets" using electrokinetics, i.e., electrowetting-on-dielectric. Several application areas for biochips are discussed, and the motivation behind the work presented in this book is introduced. At the end of the chapter, we outline the structure of the book and an overview of the topics covered.

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Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Netcompany IT and business consulting A/S
Authors: Pop, P. (Intern), Alistar, M. (Intern), Stuart, E. (Ekstern), Madsen, J. (Intern)
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In this paper we propose a system-level synthesis for MPSoCs that integrates multiple Application Specific Instruction Set Processors (ASIPs). Each ASIP is customized for a specific set of tasks. The system-level synthesis is responsible for assigning the tasks to the ASIPs, exploring different platform alternatives. We can allocate tasks to the different ASIPs and determine if the applications are schedulable only knowing the worst-case execution time (WCET) of each task. We can estimate the WCET only after establishing the micro-architecture of the ASIP. At the same time, an ASIP micro-architecture can be derived only knowing the assignment of tasks to ASIP. To address this circular dependency, we propose an Uncertainty Model for the WCETs, which captures the performance of tasks running on a range of possible ASIP implementations. We propose a novel stochastic schedulability analysis to evaluate each multi-ASIP platform. We use an Evolutionary Algorithm-based approach to explore the design space of macro-architecture possibilities and we evaluate it using real case studies.
Test-driven modeling of embedded systems

To benefit maximally from model-based systems engineering (MBSE) trustworthy high quality models are required. From the software disciplines it is known that test-driven development (TDD) can significantly increase the quality of the products. Using a test-driven approach with MBSE may have a similar positive effect on the quality of the system models.
and the resulting products and may therefore be desirable. To define a test-driven model-based systems engineering (TD-MBSE) approach, we must define this approach for numerous sub disciplines such as modeling of requirements, use cases, scenarios, behavior, architecture, etc. In this paper we present a method that utilizes the formalism of timed automata with formal and statistical model checking techniques to apply TD-MBSE to the modeling of system architecture and behavior. The results obtained from applying it to an industrial case suggest that our method provides a sound foundation for rapid development of high quality system models.

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A flexible mobile-device biosensing instrumentation platform for point-of-care medical diagnostics applications

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A flexible mobile-device biosensing instrumentation platform for point-of-care medical diagnostics applications

The early diagnosis and monitoring of chronic diseases still constitutes today one of the major healthcare challenges in our society. Advances in nanotechnology and microfluidics have been increasingly empowering researchers and engineers with tools to develop integrated biosensing solutions helping to address this challenge. Specifically, Lab-on-Chip (LoC) devices have a key role to play in the advent of Point-of-Care (PoC) medical applications, driving a shift of the medical diagnostics paradigm and the transition from a centralized, technical, high-throughput biological sample analysis process to a diagnostician and patient-oriented field decision-making support system. The success of such systems requires the development of highly sensitive and specific biosensors to reliably detect small amounts of relevant biological markers. Nevertheless, the socio-technical complexity of the PoC medical diagnostics context necessitates considering broader requirements, notably in terms of usability, flexibility, and integration capabilities. These characteristics call for multi-disciplinary design methodologies inspired from the field of systems engineering and constitute the motivations for this work.

We present a mobile-device based, PoC biosensing instrumentation platform, designed for multiplexed high-impedance sensing and the electrochemical detection of biological species on a LoC. The proposed system is thus designed as a flexible, user-friendly hardware and software platform allowing programmable electrical readout from LoCs potentially comprehending varied transducers addressing different targeted biological markers. A smart-phone/tablet docking-station embeds the hardware interface necessary for the implementation of a smart-phone digital lock-in amplifier. The platform is tested with high-impedimetric measurements from Silicon-nanowire Field Effect Transistors embedded in a LoC. Programmable firmware and flexible hardware will in turn allow for standard voltammetry and electrical impedance spectroscopy to be performed. The design of a mobile app and standard mobile software libraries will ensure system evolvability, enabling application-specific biosensors readouts and adapted user interfacing.
A novel single-step, multipoint calibration method for instrumented Lab-on-Chip systems

Despite recent and substantial advances in biosensing, information and communication, and Lab-on-Chip (LoC) technologies, the success of Point-of-Care (PoC) diagnostics and monitoring systems is still challenged by stringent requirements for robustness, cost-effectiveness, and system integration. The pitfalls of PoC system adoption can be addressed early in the system design phase. They require a multidisciplinary design approach supported by systems engineering tools and methods. Considering this, we here present both a model and an implementation of a simple and rapid calibration scheme for instrument-based PoC blood biomarker analysis systems. Motivated by the complexity of associating high-accuracy biosensing using silicon nanowire field effect transistors with ease of use for the PoC system user, we propose a novel one-step, multipoint calibration method for LoC-based systems. Our approach specifically addresses the important interfaces between a novel microfluidic unit to integrate the sensor array and a mobile-device hardware accessory. A multi-point calibration curve is obtained by generating a defined set of reference concentrations from a single input. By consecutively splitting the flow perpendicular to the diffusion interface only one mixing step is required for each of the generated calibration solutions. This results in a compact design with a very small footprint of the microfluidic layout.
Compilation and Synthesis for Fault-Tolerant Digital Microfluidic Biochips

Microfluidic-based biochips are replacing the conventional biochemical analyzers, by integrating all the necessary functions for biochemical analysis using microfluidics. The digital microfluidic biochips (DMBs) manipulate discrete amounts of fluids of nanoliter volume, named droplets, on an array of electrodes to perform operations such as dispensing, transport, mixing, split, dilution and detection.

Researchers have proposed compilation approaches, which, starting from a biochemical application and a biochip architecture, determine the allocation, resource binding, scheduling, placement and routing of the operations in the application. During the execution of a bioassay, operations could experience transient faults, thus impacting negatively the correctness of the application. We have proposed both offline (design time) and online (runtime) recovery strategies. The online recovery strategy decides the introduction of the redundancy required for fault-tolerance. We consider both time redundancy, i.e., re-executing erroneous operations, and space redundancy, i.e., creating redundant droplets for fault-tolerance. Error recovery is performed such that the number of transient faults tolerated is maximized and the timing constraints of the biochemical application are satisfied.

Previous work has assumed that the biochip architecture is given, and most approaches consider a rectangular shape for the electrode array, where operations execute on rectangular "modules" formed of electrodes. However, non-regular application-specific architectures are common in practice. Hence, we have proposed an approach to the synthesis of application-specific architectures, such that the cost is minimized and the timing constraints of the application are satisfied.

We propose an algorithm to build a library of non-regular modules for a given application-specific architecture, so that the area of a non-regular application-specific biochip can be used effectively. During fabrication, DMBs can be affected by permanent faults, which may lead to the failure of the application. Our approach introduces redundant electrodes to synthesize fault-tolerant architectures aiming at increasing the yield of DMBs. We also propose a method to estimate, at design time, the application completion time in case of permanent faults in order to verify if an application can be successfully run on the architecture.

The proposed approaches were evaluated using several real-life case studies and synthetic benchmarks.

Although energy consumption of wireless sensor network has been studied extensively, we are far behind in understanding the dynamics of the power consumption along with energy production using harvesters. We introduce Energy Harvesting Routing Analysis (EHRA) as a formal modelling framework to study wireless sensor networks (WSN) with energy-harvesting capabilities. The purpose of the framework is to analyze WSNs at a high level of abstraction, that is, before the protocols are implemented and before the WSN is deployed. The conceptual basis of EHRA comprises the environment, the medium, computational and physical components, and it captures a broad range of energy-harvesting aware routing protocols. The generic concepts of protocols are captured by a many-sorted signature, and concrete routing protocols are specified by corresponding many-sorted algebras. A first analysis tool for EHRA is developed as a simulator implemented using the functional programming language F#. This simulator is used to analyze global properties of WSNs such as network fragmentation, routing trends, and energy profiles for the nodes. Three routing protocols, with a progression in the energy-harvesting awareness, are analyzed on a network that is placed in a heterogeneous environment.

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Energy Harvesting - Wireless Sensor Networks for Indoors Applications Using IEEE 802.11
The paper investigates the feasibility of using IEEE 802.11 in energy harvesting low-power sensing applications. The investigation is based on a prototype carbon dioxide sensor node that is powered by artificial indoors light. The wireless communication module of the sensor node is based on the RTX4100 module. RTX4100 incorporates a wireless protocol that duty-cycles the radio while being compatible with IEEE 802.11 access points. The presented experiments demonstrate sustainable operation but indicate a trade-off between the benefits of using IEEE 802.11 in energy harvesting applications and the energy-efficiency of the system.

General information
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Organisations: Department of Applied Mathematics and Computer Science, MakeThisWork
Authors: Fafoutis, X. (Intern), Sørensen, T. (Ekstern), Madsen, J. (Intern)
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Workshop: International Workshop on Enabling ICT for Smart Buildings, Hasselt, Belgium, 02/06/2014 - 02/06/2014
Main Research Area: Technical/natural sciences
Medium Access Control in Energy Harvesting - Wireless Sensor Networks

Focusing on Wireless Sensor Networks (WSN) that are powered by energy harvesting, this dissertation focuses on energy-efficient communication links between senders and receivers that are alternating between active and sleeping states of operation. In particular, the focus lies on Medium Access Control (MAC) protocols that are following the receiver-initiated paradigm of asynchronous communication. According to the receiver-initiated paradigm the communication is initiated by the receiver that states its availability to receive data through beacons. The sender is passively listening to the channel until it receives the beacon of interest.

In this context, the dissertation begins with an in-depth survey of all the receiver-initiated MAC protocols and presents their unique optimization features, which deal with several challenges of the link layer such as mitigation of the energy consumption, collision avoidance, provision of Quality of Service (QoS) and security. Focusing on the particular requirements of an energy harvesting application, the dissertation continues with the presentation of a MAC protocol, named ODMAC, which extends the receiver-initiated paradigm with several energy-efficient features that aim to adapt the consumed energy to match the harvested energy, distribute the load with respect to the harvested energy, decrease the overhead of the communication, address the requirements for collision avoidance, prioritize urgent traffic and secure the system against beacon replay attacks.

The performance and behavior of ODMAC and its features are compared to the state-of-the-art and evaluated using mathematical models, simulations and testbed experiments that are based on eZ430-rf2500 wireless development platform. The results validate the efficient use of the harvested energy and demonstrate sustainable operation.

General information

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Fafoutis, X. (Intern), Dragoni, N. (Intern), Madsen, J. (Intern)
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Performance Aspects of Synthesizable Computing Systems

Embedded systems are used in a broad range of applications that demand high performance within severely constrained mechanical, power, and cost requirements. Embedded systems implemented in ASIC technology tend to provide the highest performance, lowest power consumption and lowest unit cost. However, high setup and design costs make ASICs economically viable only for high volume production. Therefore, FPGAs are increasingly being used in low and medium volume markets. The evolution of FPGAs has reached a point where multiple processor cores, dedicated accelerators, and a large number of interfaces can be integrated on a single device.

This thesis consists of five parts that address performance aspects of synthesizable computing systems on FPGAs. First, it is evaluated how synthesizable processor cores can exploit current state-of-the-art FPGA architectures. This evaluation results in a processor architecture optimized for a high throughput on modern FPGA architectures. The current hardware implementation, the Tinuso I core, can be clocked as high as 376MHz on a Xilinx Virtex 6 device and consumes fewer hardware resources than similar commercial processor configurations. The Tinuso architecture leverages predicated execution to circumvent costly pipeline stalls due to branches and exposes hazards to the compiler to keep the hardware simple. Second, it is investigated if a production compiler, GCC, is able to successfully leverage predicated execution and schedule instructions so as to mitigate the hazards. The third part of this thesis describes the design and implementation of communication structures for Tinuso multicore configurations and evaluates the scalability of these systems. Forth, a case study shows how to map a high performance synthetic aperture radar application to a synthesizable multicore system. The proposed system includes 64 processor cores and a 2D mesh interconnect on a single FPGA device and consumes about 10 watt only. Finally, a task based programming model is proposed that allows for easily expressing parallelism and simplifies memory management.

General information
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Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Schleuniger, P. (Intern), Karlsson, S. (Intern), Madsen, J. (Intern)
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Performance_Aspects_of.pdf
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Tradeoff analysis for Dependable Real-Time Embedded Systems during the Early Design Phases

Embedded systems are becoming increasingly complex and have tight competing constraints in terms of performance, cost, energy consumption, dependability, flexibility, security, etc. The objective of this thesis is to propose design methods and tools for supporting the tradeoff analysis of competing design objectives during the early design phases, which are characterized by uncertainties. We consider safety-critical real-time applications modeled as task graphs, to be implemented on distributed heterogeneous architectures consisting of processing elements (PEs), interconnected by a shared communication channel. Tasks are scheduled using fixed-priority preemptive scheduling, and we use non-preemptive scheduling for messages.

As a first step, we address the problem of function-to-task decomposition. In this context we have assumed that the application functionality is captured by a set of functional blocks, with different safety requirements. We propose a Genetic Algorithm-based metaheuristic to solve the function-to-task decomposition problem. Our algorithm also decides the mapping of tasks to the PEs of a distributed architecture and the reliability of each PE in the architecture, such that the safety and integrity constraints are satisfied, the schedulability of the real-time application is guaranteed and the overall development and product unit costs are minimized.

Next, we investigate tradeoffs between performance, energy and reliability. Addressing energy and reliability simultaneously is especially challenging, since lowering the voltage to reduce the energy consumption has been shown to increase the transient fault rate. We are interested to tolerate transient faults and we use task replication for recovery. We propose a Tabu Search-based approach, which decides the mapping of tasks to processing elements, as well as the processor voltage and frequency levels for executing each task, such that transient faults are tolerated, the real-time constraints of the application are satisfied, and the energy consumed is minimized.

In this thesis, we target the early design phases, when decisions have a high impact on the subsequent implementation choices. However, due to a lack of information, the early design phases are characterized by uncertainties, e.g., in the worst-case execution times (WCETs), in the functionality requirements, or in the hardware component costs. In this context, we select the hardware components for the architecture and derive a mapping of tasks in the application, such that the resulted implementation is both robust and flexible. The architecture also has a high chance to have its unit cost within the cost budget. Robust means that the application has a high chance of being schedulable, considering the WCET uncertainties, whereas a flexible mapping has a high chance to successfully accommodate future functionality changes. We propose a Genetic Algorithm-based approach to solve this optimization problem. The proposed tradeoff analysis methods have been evaluated using several synthetic and real-life benchmarks.
Application-specific fault-tolerant architecture synthesis for digital microfluidic biochips

Microfluidic-based biochips are replacing the conventional biochemical analyzers, and are able to integrate onchip all the necessary functions for biochemical analysis using microfluidics. The digital microfluidic biochips are based on the manipulation of liquids not as a continuous flow, but as discrete droplets on an array of electrodes. Microfluidic operations, such as transport, mixing, split, are performed on this array by routing the corresponding droplets on a series of electrodes. Researchers have proposed several approaches for the synthesis of digital microfluidic biochips. All previous work assumes that the biochip architecture is given, and most approaches consider a rectangular shape for the electrode array. However, non-regular application-specific architectures are common in practice. Hence, in this paper, we propose an approach to the application-specific architecture synthesis. Our approach can also help the designer to increase the yield by introducing redundant electrodes to tolerate permanent faults. The proposed architecture synthesis algorithm has been evaluated using several benchmarks.

General information
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Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Alistar, M. (Intern), Pop, P. (Intern), Madsen, J. (Intern)
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ASAM: Automatic architecture synthesis and application mapping
This paper focuses on mastering the automatic architecture synthesis and application mapping for heterogeneous massively-parallel MPSoCs based on customizable application-specific instruction-set processors (ASIPs). It presents an overview of the research being currently performed in the scope of the European project ASAM of the ARTEMIS program. The paper briefly presents the results of our analysis of the main challenges to be faced in the design of such heterogeneous MPSoCs. It explains which system, design, and electronic design automation (EDA) concepts seem to be adequate to address the challenges and solve the problems. Finally, it discusses the ASAM design-flow, its main stages and tools and their application to a real-life case study.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Intel, STMicroelectronics, Technische Universität Eindhoven, Università degli studi di Cagliari
Authors: Jozwiak, L. (Ekstern), Lindwer, M. (Ekstern), Corvino, R. (Ekstern), Meloni, P. (Ekstern), Micconi, L. (Intern), Madsen, J. (Intern), Diken, E. (Ekstern), Gangadharan, D. (Intern), Jordans, R. (Ekstern), Pomata, S. (Ekstern), Pop, P. (Intern), Tuveri, G. (Ekstern), Raffo, L. (Ekstern), Notarangelo, G. (Ekstern)
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Biochemical Application Compilation and Architecture Synthesis for Fault-Tolerant Digital Microfluidic Biochips

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Control Synthesis for the Flow-Based Microfluidic Large-Scale Integration Biochips

In this paper we are interested in flow-based microfluidic biochips, which are able to integrate the necessary functions for biochemical analysis on-chip. In these chips, the flow of liquid is manipulated using integrated microvalves. By combining several microvalves, more complex units, such as micropumps, mixers, and multiplexers, can be built. In this paper we propose, for the first time to our knowledge, a top-down control synthesis framework for the flow-based biochips. Starting from a given biochemical application and a biochip architecture, we synthesize the control logic that is used by the biochip controller to automatically execute the biochemical application. We also propose a control pin count minimization scheme aimed at efficiently utilizing chip area, reducing macro-assembly around the chip and enhancing chip scalability. We have evaluated our approach using both real-life applications and synthetic benchmarks.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, National Cheng Kung University
Authors: Minhass, W. H. (Intern), Pop, P. (Intern), Madsen, J. (Intern), Ho, T. (Ekstern)
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Formal methods for design and simulation of embedded systems
Cyper physical systems (CPSs) are present in many variants in our daily life. The complexity of developing a CPS is quickly increasing and the interaction between different CPSs is increasingly important. The interaction of the systems is becoming more and more fluent and seamless.

This thesis presents the development of a formal systems modelling (ForSyDe) framework for modelling CPSs. The formalism of the framework makes computer aided design (CAD) a possibility for developing CPSs. The framework consists of four models of computation (MoCs): synchronous (SY), synchronous data flow (SDF), discrete event (DE), and continuous time (CT).

Usage of the framework is demonstrated with two use cases. A company use case featuring a hearing aid calibration device and the distributed energy harvesting aware routing (DEHAR) algorithm for wireless sensor networks (WSNs). These two use cases illustrate different design challenges. With the ForSyDe framework, the use cases are expressed as homogeneous and heterogeneous models.

The company use case illustrates that the ForSyDe framework handles systems with well defined interactions very well. The WSN use case illustrates that networked systems with complex interaction are more challenging to express naturally, yet the ForSyDe framework is able to express such systems.

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Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Jakobsen, M. K. (Intern), Madsen, J. (Intern), Hansen, M. R. (Intern)
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Place of publication: Kgs. Lyngby
Hierarchical DSE for multi-ASIP platforms

This work proposes a hierarchical Design Space Exploration (DSE) for the design of multi-processor platforms targeted to specific applications with strict timing and area constraints. In particular, it considers platforms integrating multiple Application Specific Instruction Set Processors (ASIPs) and each ASIP is automatically synthesized and tuned for a specific set of tasks. The definition of the platform (number of processors and their interconnection) and of the micro-architecture of each single ASIP are tightly coupled. Tasks can be allocated to the different ASIPs only knowing their performance and therefore the ASIP micro-architecture. At the same time an ASIP can be derived only knowing the functionality that it has to implement, i.e. the tasks that are assigned. We break this circular dependency with an iterative hierarchical DSE, applied at platform and micro-architecture level. We evaluate different platforms and micro-architecture alternatives to find a multi-ASIP platform targeted to the input application and able to meet the design constraints. We evaluate our design flow using a MJPEG encoder application.
Module-Based Synthesis of Digital Microfluidic Biochips with Droplet-Aware Operation Execution

Microfluidic biochips represent an alternative to conventional biochemical analyzers. A digital biochip manipulates liquids not as continuous flow, but as discrete droplets on a two-dimensional array of electrodes. Several electrodes are dynamically grouped to form a virtual device, on which operations are executed by moving the droplets. So far, researchers have ignored the locations of droplets inside devices, considering that all the electrodes forming the device are occupied throughout the operation execution. In this article, we consider a droplet-aware execution of microfluidic operations, which means that we know the exact position of droplets inside the modules at each time-step. We propose a Tabu Search-based metaheuristic for the synthesis of digital biochips with droplet-aware operation execution. Experimental results show that our approach can significantly reduce the application completion time, allowing us to use smaller area biochips and thus reduce costs.
Multi-ASIP Platform Synthesis for Event-Triggered Applications with Cost/Performance Trade-offs

In this paper, we propose a technique to synthesize a cost-efficient distributed platform consisting of multiple Application Specific Instruction Set Processors (multi-ASIPs) running applications with strict timing constraints. Multi-ASIP platform synthesis is a non-trivial task for two reasons. Firstly, we need to know the WCET of tasks in target applications to derive platforms (including synthesized ASIPs) in which the tasks are schedulable. However, the WCET of tasks can be known only after the ASIPs are synthesized. We break this circular dependency by using a probability distribution of the WCET of a task (further referred to as the WCET uncertainty model), which takes into account the underlying microarchitectural configurations for the ASIP implementation. Secondly, the datapath area of the multi-ASIPs synthesized is an important design factor that contributes significantly towards the overall cost of the platform. We propose an area estimation model and a WCET uncertainty model that consider the effect of task datapath similarity. Based on these two models, we support the designer in exploring cost/performance trade-offs during the platform synthesis. We propose an Evolutionary Algorithm-based approach to solve this multiobjective optimization problem. The proposed approach has been evaluated using several benchmarks and it provides a number of multi-ASIP platform solutions exploring the trade-offs in the cost/performance design space.

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Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Gangadharan, D. (Intern), Micconi, L. (Intern), Pop, P. (Intern), Madsen, J. (Intern)
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Publication date: 2013

Multi-ASIP Platform Synthesis for Real-Time Applications

In this paper we are interested in deriving a distributed platform, composed of heterogeneous processing elements, targeted to applications that have strict timing constraints. We consider that the platform may use multiple Application Specific Instruction Set Processors (ASIPs). An ASIP is synthesized and tuned for a specific set of tasks (i.e., a task cluster). During design space exploration (DSE), we evaluate each platform solution visited in terms of its cost and performance, i.e., its ability to execute the applications such that they meet their timing constraints. To determine if the applications are schedulable, we have to know the worst-case execution time (WCET) of each task. However, we can determine the WCETs only after the ASIPs are synthesized, which is time consuming and therefore cannot be done during DSE. To address this circular dependency (the ASIPs depend on the task clustering, and the WCETs of tasks, used to determine schedulability, depend on how ASIPs are synthesized), we propose an uncertainty model for the WCETs, which captures the range of possible ASIP implementations. Based on this model, we synthesize a multi-ASIP platform, such that the applications have a high chance of being schedulable and the cost constraints imposed on the platform are fulfilled. We propose an Evolutionary Algorithm-based approach, which uses a novel stochastic schedulability analysis to solve this optimization problem. The proposed approach has been evaluated using several benchmarks.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Micconi, L. (Intern), Gangadharan, D. (Intern), Pop, P. (Intern), Madsen, J. (Intern)
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Operation placement for application-specific digital microfluidic biochips

Microfluidic-based biochips are replacing the conventional biochemical analyzers, and are able to integrate on-chip all the necessary functions for biochemical analysis using microfluidics. The digital microfluidic biochips are based on the manipulation of liquids not as a continuous flow, but as discrete droplets on an array of electrodes. Microfluidic operations, such as transport, mixing, split, are performed on this array by routing the corresponding droplets on a series of electrodes. Researchers have proposed several approaches for the synthesis of digital microfluidic biochips. All previous work assumes that the biochip architecture is given, and consider a rectangular shape for the electrode array. However, non-regular application-specific architectures are common in practice. In this paper, we are interested in determining a placement of operations for application-specific biochips, such that the application completion time is minimized. The proposed algorithm has been evaluated using several benchmarks.

Quality-Driven Model-Based Design of MultiProcessor Embedded Systems for Highlydemanding Applications

The recent spectacular progress in modern nano-dimension semiconductor technology enabled implementation of a complete complex multi-processor system on a single chip (MPSoC), global networking and mobile wire-less communication, and facilitated a fast progress in these areas. New important opportunities have been created. The traditional applications can be served much better and numerous new sorts of embedded systems became technologically feasible and economically justified. Various monitoring, control, communication or multi-media systems that can be put on or embedded in (mobile, poorly accessible or distant) objects, installations, machines or devices, or even implanted in human or animal body can serve as examples. However, many of the modern embedded application impose very stringent functional and parametric demands. Moreover, the spectacular advances in microelectronics introduced unusual silicon and system complexity. The combination of the huge complexity with the stringent application requirements results in numerous serious design and development challenges, such as: accounting in design for more aspects and changed relationships among aspects, complex multi-objective MPSoC optimization, adequate resolution of numerous complex design tradeoffs, reduction of the design productivity gap for the increasingly complex and sophisticated systems, reduction of the time-to-market and development costs without compromising the system quality, etc. These challenges cannot be well addressed without an adequate system and design methodology adaptation. The adequate system and design paradigms to solve the problems seem to be the paradigms of: life-inspired systems, and quality-driven design. The first part of the tutorial is devoted to discussion of the issues and challenges in development of contemporary and future embedded systems and introduction of the quality-driven model-based design methodology based on the paradigms of life-inspired systems and quality-driven design earlier proposed by the first presenter of this tutorial. Subsequently, the actual industrial Intel's ASIP-based MPSoC technology is introduced, and situation, trends and problems are discussed in the area of heterogeneous MPSoCs based on adaptable ASIPs and hardware accelerators for highly-demanding applications.
Architectural Synthesis of Flow-Based Microfluidic Large-Scale Integration Biochips

Microfluidic biochips are replacing the conventional biochemical analyzers and are able to integrate the necessary functions for biochemical analysis on-chip. In this paper we are interested in flow-based biochips, in which the flow of liquid is manipulated using integrated microvalves. By combining several microvalves, more complex units, such as micropumps, switches, mixers, and multiplexers, can be built. The manufacturing technology, soft lithography, used for the flow-based biochips is advancing faster than Moore's law, resulting in increased architectural complexity. However, the designers are still using full-custom and bottom-up, manual techniques in order to design and implement these chips. As the chips become larger and the applications become more complex, the manual methodologies will not scale, becoming highly inadequate. Therefore, for the first time to our knowledge, we propose a top-down architectural synthesis methodology for the flow-based biochips. Starting from a given biochemical application and a microfluidic component library, we are interested in synthesizing a biochip architecture, i.e., performing component allocation from the library based on the biochemical application, generating the biochip schematic (netlist) and then performing physical synthesis (deciding the placement of the microfluidic components on the chip and performing routing of the microfluidic channels), such that the application completion time is minimized. We evaluate our proposed approach by synthesizing architectures for real-life applications as well as synthetic benchmarks.

General information
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Organisations: Department of Informatics and Mathematical Modeling, Embedded Systems Engineering, Computer Science and Engineering, Technical University of Denmark
Authors: Minhass, W. H. (Intern), Pop, P. (Intern), Madsen, J. (Intern), Blaga, F. S. (Ekstern)
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ASAM: Automatic Architecture Synthesis and Application Mapping

This paper focuses on mastering the automatic architecture synthesis and application mapping for heterogeneous massively-parallel MPSoCs based on customizable application-specific instruction-set processors (ASIPs). It presents an over-view of the research being currently performed in the scope of the European project ASAM of the ARTEMIS program. The paper briefly presents the results of our analysis of the main problems to be solved and challenges to be faced in the design of such heterogeneous MPSoCs. It explains which system, design, and electronic design automation (EDA) concepts seem to be adequate to resolve the problems and address the challenges. Finally, it introduces and briefly discusses the ASAM design-flow and its main stages.

General information
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Organisations: Department of Informatics and Mathematical Modeling, Embedded Systems Engineering, Technische Universität Eindhoven, Intel, Università degli studi di Cagliari
Authors: Jozwiak, L. (Ekstern), Lindwer, M. (Ekstern), Corvino, R. (Ekstern), Meloni, P. (Ekstern), Micconi, L. (Intern), Madsen, J. (Intern), Diken, E. (Ekstern), Gangadharan, D. (Intern), Jordans, R. (Ekstern), Pomata, S. (Ekstern), Pop, P.
Biochips: The Integrated Circuit of Biology

Microfluidic biochips integrate different biochemical analysis functionalities (e.g., dispensers, filters, mixers, separators, detectors) on-chip, miniaturizing the macroscopic chemical and biological processes often processed by lab-robots, to a sub-millimeter scale. These microsystems offer several advantages over the conventional biochemical analyzers, e.g., reduced sample and reagent volumes, speeded up biochemical reactions, ultra-sensitive detection and higher system throughput, with several assays being integrated on the same chip. Hence, microfluidic biochips are replacing the conventional biochemical analyzers, and are able to integrate on-chip all the necessary functions for biochemical analysis. Microfluidic biochips have an immense potential in multiple application areas, such as clinical diagnostics, advanced sequencing, drug discovery, and environmental monitoring, to name a few. Consequently, over the last decade, biochips have received significant attention both in academia and industry. The International Technology Roadmap for Semiconductors 2011 has listed "Medical" as a “Market Driver” for the future, and many companies related to biochips have already emerged in recent years and have reported significant profits.

Droplet-Aware Module-Based Synthesis for Fault-Tolerant Digital Microfluidic Biochips

Microfluidic biochips are replacing the conventional biochemical analyzers, and are able to integrate on-chip all the basic functions for biochemical analysis. On a “digital” biochip liquids are manipulated as discrete droplets on a two-dimensional microfluidic array of electrodes. Basic operations, such as mixing and dilution, are performed on the array, by routing the corresponding droplets on a group of electrodes, forming a virtual device. Initially researchers have ignored the locations of droplets during operation execution, and have considered that all electrodes inside devices are occupied. We have recently proposed a droplet-aware approach for the execution of operations on the microfluidic array, in which the locations of droplets inside devices are known at each time step. In this article we extend the droplet-aware approach to consider the synthesis of biochips which contain defective electrodes on the microfluidic array. We show that for such biochips knowing the exact locations of droplets during operation execution leads to significant improvements in the completion time of applications.
Energy-Harvesting Wireless Sensor Networks

Energy Harvesting comprises a promising solution to one of the key problems faced by battery-powered Wireless Sensor Networks, namely the limited nature of the energy supply (finite battery capacity). By harvesting energy from the surrounding environment, the sensors can have a continuous lifetime without any needs for battery recharge or replacement. However, energy harvesting introduces a change to the fundamental principles based on which WSNs are designed and realized. In this poster we sketch some of the key research challenges as well as our ongoing work in designing and realizing Wireless Sensor Networks with energy harvesting capability.
Online Synthesis for Error Recovery in Digital Microfluidic Biochips with Operation Variability

Microfluidic-based biochips are replacing the conventional biochemical analyzers, and are able to integrate on-chip all the necessary functions for biochemical analysis using microfluidics. The digital microfluidic biochips are based on the manipulation of liquids not as a continuous flow, but as discrete droplets. Researchers have presented approaches for the synthesis of digital microfluidic biochips, which, starting from a biochemical application and a given biochip architecture, determine the allocation, resource binding, scheduling, placement and routing of the operations in the application. The droplet volumes can vary erroneously due to parametric faults, thus impacting negatively the correctness of the application. Researchers have proposed approaches that synthesize offline predetermined recovery subroutines, which are activated online when errors occur. In this paper, we propose an online synthesis strategy, which determines the appropriate recovery actions at the moment when faults are detected. We have also proposed a biochemical application model which can capture both time-redundant and space-redundant recovery operations. Experiments performed on three real-life case studies show that, by taking into account the biochip configuration when errors occur, our online synthesis is able to reduce the application times.

Optimal Register Allocation by Augmented Left-Edge Algorithm on Arbitrary Control-Flow Structures

A new algorithm for optimal register allocation in context of high-level synthesis is presented. In this paper we show how the greedy left-edge algorithm can be leveraged to obtain a globally optimal allocation, that is computed in polynomial time. By splitting variables at block boundaries, allows for allocation to be done using only quasi-local and local allocation -
avoiding the complexity of true global allocation. As local allocation is much simpler than global allocation, this approach emphasizes efficiency and ease of implementation - at a cost of an increased number of register transfers compared to other allocators. Experiments show that runtime is linear for all practical purposes.

**General information**
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Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering, Embedded Systems Engineering, Technical University of Denmark
Authors: Ruvald Pedersen, M. (Ekstern), Madsen, J. (Intern)
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Main Research Area: Technical/natural sciences
Conference: 30th NORCHIP conference, Copenhagen, Denmark, 12/11/2012 - 12/11/2012
Register allocation, High-level synthesis
DOIs: 10.1109/NORCHIP.2012.6403107
Source: dtu Source-ID: n::oai:DTIC-ART:iel/377357942::24842
Publication: Research - peer-review › Article in proceedings – Annual report year: 2012

Robust and flexible mapping for real-time distributed applications during the early design phases
We are interested in mapping hard real-time applications on distributed heterogeneous architectures. An application is modeled as a set of tasks, and we consider a fixed-priority preemptive scheduling policy. We target the early design phases, when decisions have a high impact on the subsequent implementation choices. However, due to a lack of information, the early design phases are characterized by uncertainties, e.g., in the worst-case execution times (wcets), or in the functionality requirements. We model uncertainties in the wcets using the "percentile method". The uncertainties in the functionality requirements are captured using "future scenarios", which are task sets that model functionality likely to be added in the future. In this context, we derive a mapping of tasks in the application, such that the resulted implementation is both robust and flexible. Robust means that the application has a high chance of being schedulable, considering the wcet uncertainties, whereas a flexible mapping has a high chance to successfully accommodate the future scenarios. We propose a Genetic Algorithm-based approach to solve this optimization problem. Extensive experiments show the importance of taking into account the uncertainties during the early design phases.

**General information**
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Organisations: Department of Informatics and Mathematical Modeling, Embedded Systems Engineering, Computer Science and Engineering, Lund University
Authors: Gan, J. (Intern), Pop, P. (Intern), Gruian, F. (Ekstern), Madsen, J. (Intern)
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Publication: Research - peer-review › Conference abstract in proceedings – Annual report year: 2012

Routing-based synthesis of digital microfluidic biochips
Microfluidic biochips are replacing the conventional biochemical analyzers, and are able to integrate on-chip all the necessary functions for biochemical analysis. The "digital" biochips are manipulating liquids as discrete droplets on a two-dimensional array of electrodes. Basic microfluidic operations, such as mixing and dilution, are performed on the array, by
routing the corresponding droplets on a series of electrodes. So far, researchers have assumed that these operations are executed on virtual rectangular devices, formed by grouping several adjacent electrodes. One drawback is that all electrodes are considered occupied during the operation execution, although the droplet uses only one electrode at a time. Moreover, the operations can actually be performed by routing the droplets on any sequence of electrodes on the microfluidic array. Hence, in this paper, we eliminate the concept of virtual devices and allow the droplets to move on the chip on any route during operation execution. Thus, the synthesis problem is transformed into a routing problem. We develop an algorithm based on a Greedy Randomized Adaptive Search Procedure (GRASP) and we show that routing-based synthesis leads to significant improvements in the application completion time compared to traditional synthesis based on virtual devices. However, the disadvantage of the routing-based approach is that it may contaminate larger areas of the biochip, when synthesizing applications containing liquids which may adsorb on the surface of the microfluidic array. We have extended the GRASP-based algorithm to consider contamination avoidance during routing-based synthesis. Several real-life examples and synthetic benchmarks are used to evaluate the proposed approaches.

**General information**
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Organisations: Department of Informatics and Mathematical Modeling, DTU Data Analysis, Department of Mathematics, Computer Science and Engineering, Embedded Systems Engineering
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Synthesis of Biochemical Applications on Flow-Based Microfluidic Biochips using Constraint Programming

Microfluidic biochips are replacing the conventional biochemical analyzers and are able to integrate the necessary functions for biochemical analysis on-chip. In this paper we are interested in flow-based biochips, in which the flow of liquid is manipulated using integrated microvalves. By combining several microvalves, more complex units, such as micropumps, switches, mixers, and multiplexers, can be built. We propose a constraint programming (CP) based approach for the synthesis of biochemical applications on flow-based microfluidic biochips. We use a sequencing graph to model the biochemical application and consider that the biochip architecture is given. We model the architecture using a topology graph. We are interested in synthesizing an implementation, consisting of binding and scheduling of the biochemical operations onto the components of the architecture, such that the resource and dependency constraints are satisfied and the application completion time is minimized. Our CP framework generates optimal implementations and has been evaluated using synthetic as well as real-life case studies.

System-Level Modeling and Synthesis Techniques for Flow-Based Microfluidic Very Large Scale Integration Biochips

Microfluidic biochips integrate different biochemical analysis functionalities on-chip and offer several advantages over the conventional biochemical laboratories. In this thesis, we focus on the flow-based biochips. The basic building block of such a chip is a valve which can be fabricated at very high densities, e.g., 1 million valves per cm². By combining these valves, more complex units such as mixers, switches, multiplexers can be built up and the technology is therefore referred to as microfluidic Very Large Scale Integration (mVLSI).

The manufacturing technology for the mVLSI biochips has advanced faster than Moore’s law. However, the design methodologies are still manual and bottom-up. Designers use drawing tools, e.g., AutoCAD, to manually design the chip. In order to run the experiments, applications are manually mapped onto the valves of the chips (analogous to exposure of gate-level details in electronic integrated circuits). Since mVLSI chips can easily have thousands of valves, the manual process can be very time-consuming, error-prone and result in inefficient designs and mappings.

We propose, for the first time to our knowledge, a top-down modeling and synthesis methodology for the mVLSI biochips. We propose a modeling frame-work for the components and the biochip architecture. Using these models, we present an architectural synthesis methodology (covering steps from the schematic design to the physical synthesis), generating an application-specific mVLSI biochip. We also propose a framework for mapping the biochemical applications onto the mVLSI biochips, binding and scheduling the operations and performing fluid routing. A control synthesis framework for
determining the exact valve activation sequence required to execute the application is also proposed. In order to reduce the macro-assembly around the chip and enhance chip scalability, we propose an approach for the biochip pin count minimization. We also propose a throughput maximization scheme for the cell culture mVLSI biochips, saving time and reducing costs. We have extensively evaluated the proposed approaches using real-life case studies and synthetic benchmarks. The proposed framework is expected to facilitate programmability and automation, enabling the emergence of a large biochip market.

General information
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Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Minhass, W. H. (Intern), Pop, P. (Intern), Madsen, J. (Intern)
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System level modelling with open source tools
In this paper, we present a system level design methodology which allows designers to model and analyze their systems from the early stages of the design process until final implementation. The design methodology targets heterogeneous embedded systems and is based on a formal modeling framework, called ForSyDe. ForSyDe is available under the open source approach, which allows small and medium enterprises (SME) to get easy access to advanced modeling capabilities and tools. We give an introduction to the design methodology through the system level modeling of a simple industrial use case, and we outline the basics of the underlying ForSyDe model.

General information
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Organisations: Department of Informatics and Mathematical Modeling, Embedded Systems Engineering, Computer Science and Engineering, KTH - Royal Institute of Technology, Auditdata A/S
Authors: Jakobsen, M. K. (Intern), Madsen, J. (Intern), Niaki, S. H. A. (Ekstern), Sander, I. (Ekstern), Hansen, J. (Ekstern)
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A Bio-Inspired Self-Healing Reconfigurable Hardware Architecture: Concept, design, prototype, and evaluation

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Authors: Boesen, M. R. (Intern), Madsen, J. (Intern), Pop, P. (Intern)
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Place of publication: Kgs. Lyngby, Denmark
Application-Aware Optimization of Redundant Resources for the Reconfigurable Self-Healing eDNA Hardware Architecture

In this paper we are interested in the mapping of embedded applications on a dynamically reconfigurable self-healing hardware architecture known as the eDNA (electronic DNA) architecture. The architecture consists of an array of cells interconnected through a 2D-mesh topology. Each cell consists of a processor and an Arithmetic Logic Unit (ALU). Applications are modeled as task graphs. We propose a Tabu Search-based approach for the mapping of an application to the reconfigurable architecture, such that the performance is maximized. When faults occur, the self-healing moves the affected functionality to spare-cells. We optimize the number and placement of spare-cells such that the performance overhead is minimized in the fault-free scenario and the application degrades gracefully in case of faults. This has been done using three different spare-cell placement strategies. We use Monte Carlo simulation to determine the average performance overhead increase due to fault occurrences. The approach has been evaluated using a large number of benchmarks and have shown that the performance loss is reduced with 16% for the best spare-cell placement strategy.

Autonomous distributed self-organizing and self-healing hardware architecture - The eDNA concept

This paper presents the current state of the autonomous distributed self-organizing and self-healing electronic DNA (eDNA) hardware architecture (patent pending). In its current prototype state, the eDNA architecture is capable of responding to multiple injected faults by autonomously reconfiguring itself to accommodate the fault and keep the application running. This paper will also disclose advanced features currently available in the simulation model only. These features are future work and will soon be implemented in hardware. Finally we will describe step-by-step how an application is implemented on the eDNA architecture.
Biologically inspired hardware cell architecture

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Authors: Boesen, M. R. (Intern), Madsen, J. (Intern)
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Cell Culture Microfluidic Biochips: Experimental Throughput Maximization

Microfluidic biochips offer a promising alternative to a conventional biochemical laboratory, integrating all necessary functionalities on-chip in order to perform biochemical applications. Researchers have started to propose computer-aided design tools for the synthesis of such biochips. Our focus in this paper is on the optimization of how a biochemical application is performed on a biochip. In this paper, we consider cell culture biochips, where several cell colonies are exposed to soluble compounds and monitored in real-time to determine the right combination of factors that leads to the desired results. These biochips have high research potential, e.g., cancer research, stem cell, drug discovery. The application considered is a full-factorial experimental design, where all possible combinations of compounds are applied. We are interested to automatically synthesize (currently done manually) the settings of an experimental design, consisting of decision on the placement pattern of cell colonies and the insertion schedule of compounds such that the biochip throughput is maximized, thus increasing the system productivity, saving time and reducing costs. We have proposed a Simulated Annealing metaheuristic for experimental design generation for the cell culture microfluidic biochips, and we have evaluated our approach using multiple experimental setups.

General information
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Energy/Reliability Trade-offs in Fault-Tolerant Event-Triggered Distributed Embedded Systems

This paper presents an approach to the synthesis of low-power fault-tolerant hard real-time applications mapped on distributed heterogeneous embedded systems. Our synthesis approach decides the mapping of tasks to processing elements, as well as the voltage and frequency levels for executing each task, such that transient faults are tolerated, the timing constraints of the application are satisfied, and the energy consumed is minimized. Tasks are scheduled using fixed-priority preemptive scheduling, while replication is used for recovery from multiple transient faults. Addressing energy and reliability simultaneously is especially challenging, since lowering the voltage to reduce the energy consumption has been shown to increase the transient fault rate. We presented a Tabu Search-based approach which uses an energy/reliability trade-off model to find reliable and schedulable implementations with limited energy and hardware resources. We evaluated the algorithm proposed using several synthetic and real-life benchmarks.

Expressing Coarse-Grain Dependencies Among Tasks in Shared Memory Programs

Designers of embedded systems face tight constraints on resources, response time and cost. The ability to analyze embedded systems is essential to timely delivery of new designs. Many analysis techniques model parallel programs as task graphs. Task graphs capture the worst-case execution times of individual program tasks and the data dependencies among these. This paper introduces two compiler directives which let programmers annotate source code with data dependencies among tasks. Compiler analysis overapproximates the actual dependencies among tasks. The directives help eliminate potential data dependencies that do not occur at runtime. This lets tools compute more accurate task graphs from the annotated code. The correct use of the directives cannot be verified at compile time. Therefore, the check for correct use is done at runtime—not unlike dynamic array bounds checking in many languages. The overhead of verifying the correct use of the directives was measured on a set of benchmarks on two platforms. The overhead of runtime checks was found to be negligible in all instances.
Feedback Driven Annotation and Refactoring of Parallel Programs

This thesis combines programmer knowledge and feedback to improve modeling and optimization of software. The research is motivated by two observations. First, there is a great need for automatic analysis of software for embedded systems - to expose and model parallelism inherent in programs. Second, some program properties are beyond reach of
such analysis for theoretical and practical reasons - but can be described by programmers. Three aspects are explored. The first is annotation of the source code. Two annotations are introduced. These allow more accurate modeling of parallelism and communication in embedded programs. Runtime checks are developed to ensure that annotations correctly describe observable program behavior. The performance impact of runtime checking is evaluated on several benchmark kernels and is negligible in all cases. The second aspect is compilation feedback. Annotations are not effective unless programmers are told how and when they are beneficial. A prototype compilation feedback system was developed in collaboration with IBM Haifa Research Labs. It reports issues that prevent further analysis to the programmer. Performance evaluation shows that three programs perform significantly faster - up to 12.5x - after modification directed by the compilation feedback system. The last aspect is refinement of compilation feedback. Out of numerous issues reported, few are important to solve. Different compilers and compilation flags are used to estimate whether an issue can be resolved or not. On average, 43% of the issues reported can be categorized as potentially resolvable (27%) or unresolvable (15%).

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**Integration of the Reconfigurable Self-Healing eDNA Architecture in an Embedded System**
In this work we describe the first real world case study for the self-healing eDNA (electronic DNA) architecture by implementing the control and data processing of a Fourier Transform Spectrometer (FTS) on an eDNA prototype. For this purpose the eDNA prototype has been ported from a Xilinx Virtex 5 FPGA to an embedded system consisting of a PowerPC and a Xilinx Virtex 5 FPGA. The FTS instrument features a novel liquid crystal waveguide, which consequently eliminates all moving parts from the instrument. The addition of the eDNA architecture to do the control and data processing has resulted in a highly fault-tolerant FTS instrument. The case study has shown that the early stage prototype of the autonomous self-healing eDNA architecture is expensive in terms of execution time.

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Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling, NASA Jet Propulsion Laboratory
Authors: Boesen, M. R. (Intern), Keymeulen, D. (Ekstern), Madsen, J. (Intern), Lu, T. (Ekstern), Chao, T. (Ekstern)
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Integration of the Self-Healing eDNA Architecture in a Liquid Crystal Waveguide-based Fourier Transform Spectrometer

In this work we describe the first real world case study for the self-healing eDNA (electronic DNA) architecture by implementing the control and data processing of a Fourier Transform Spectrometer (FTS) on an eDNA prototype. For this purpose the eDNA prototype has been ported from a Xilinx Virtex 5 FPGA to an embedded system consisting of a PowerPC and a Xilinx Virtex 5 FPGA. The FTS instrument features a novel liquid crystal waveguide, which consequently eliminates all moving parts from the instrument. The addition of the eDNA architecture to do the control and data processing has resulted in a highly fault-tolerant FTS instrument. The case study has shown that the early stage prototype of the autonomous self-healing eDNA architecture is expensive in terms of execution time.

General information
State: Published
Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling, NASA Jet Propulsion Laboratory
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Modelling of Energy Harvesting Aware Wireless Sensor Networks

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Recent Research and Emerging Challenges in the System-Level Design of Digital Microfluidic Biochips

General information
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Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Pop, P. (Intern), Maftei, E. (Intern), Madsen, J. (Intern)
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Sows’ activity classification device using acceleration data – A resource constrained approach
This paper discusses the main architectural alternatives and design decisions in order to implement a sows’ activity classification model on electronic devices. The different possibilities are analyzed in practical and technical aspects, focusing on the implementation metrics, like cost, performance, complexity and reliability. The target architectures are divided into: server based, where the main processing element is a central computer; and embedded based, where the processing is distributed on devices attached to the animals. The initial classification model identifies the activities performed by the sows using a multi-process Kalman filter having, as input, 3-axes data from accelerometers. However, the power demanding hardware resources to run the filters require frequent battery recharges, making its use unsuitable in the current state-of-the-art. It motivated the development of a heuristic classification approach, focusing on the resource constrained characteristics of embedded systems. The new approach classifies the activities performed by the sows with accuracy close to 90%. It was implemented as a hardware module that can easily be instantiated to provide preprocessed information to models in order to detect important situations in the sows’ life, e.g. the onset of farrowing.
Synthesis of Digital Microfluidic Biochips with Reconfigurable Operation Execution

Microfluidic biochips are an alternative to conventional biochemical laboratories, and are able to integrate on-chip all the necessary functions for biochemical analysis. The "digital" biochips are manipulating liquids not as a continuous flow, but as discrete droplets on a two-dimensional array of electrodes. The main objective of this thesis is to develop top-down synthesis techniques for digital microfluidic biochips. So far, researchers have assumed that operations are executing on virtual modules of rectangular shape, formed by grouping adjacent electrodes, and which have a fixed placement on the microfluidic array. However, operations can actually execute by routing the droplets on any sequence of electrodes on the biochip. Thus, we have proposed a routing-based model of operation execution, and we have developed several associated synthesis approaches, which progressively relax the assumption that operations execute inside fixed rectangular modules. The proposed synthesis approaches consider that i) modules can dynamically move during their execution and ii) can have non-rectangular shapes. iii) We have relaxed the assumption that all electrodes are occupied during the operation execution, by taking into account the position of droplets inside modules. Finally, iv) we have eliminated the concept of virtual modules and have allowed the droplets to move on the chip on any route. In this context, we have also shown how contamination can be avoided. We have extensively evaluated the proposed approaches using several real-life case studies and synthetic benchmarks. The experiments show that by considering the dynamically reconfigurable nature of microfluidic operations, significant improvements can be obtained, decreasing the biochemical application completion times, reducing thus the biochip area and implementation costs.

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System-Level Modeling and Synthesis of Flow-Based Microfluidic Biochips

Microfluidic biochips are replacing the conventional biochemical analyzers and are able to integrate the necessary functions for biochemical analysis on-chip. There are several types of microfluidic biochips, each having its advantages and limitations. In this paper we are interested in flow-based biochips, in which the flow of liquid is manipulated using integrated microvalves. By combining several microvalves, more complex units, such as micropumps, switches, mixers, and multiplexers, can be built. Although researchers have proposed significant work on the system-level synthesis of droplet-based biochips, which manipulate droplets on a two-dimensional array of electrodes, no research on system-level synthesis of flow-based biochips has been reported so far. The focus has been on application modeling and component-level simulation. Therefore, for the first time to our knowledge, we propose a system-level modeling and synthesis approach for flow-based biochips. We have developed a topology graph-based model of the biochip architecture, and we have used a sequencing graph to model the biochemical applications. We consider that the architecture of the biochip is given, and we are interested to synthesize an implementation, consisting of the binding of operations in the application to the functional units of the architecture, the scheduling of operations and the routing and scheduling of the fluid flows, such that the application completion time is minimized. We propose a List Scheduling-based heuristic for solving this problem. The proposed heuristic has been evaluated using two real-life case studies and a set of four synthetic benchmarks.

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System Level Modelling and Performance Estimation of Embedded Systems
The advances seen in the semiconductor industry within the last decade have brought the possibility of integrating evermore functionality onto a single chip forming functionally highly advanced embedded systems. These integration possibilities also imply that as the design complexity increases, so does the design time and eort. This challenge is widely recognized throughout academia and the industry and in order to address this, novel frameworks and methods, which will automate design steps as well as raise the level of abstraction used to design systems, are being called upon. To support an efficient system level design methodology, a modelling framework for performance estimation and design space exploration at the system level is required. This thesis presents a novel component based modelling framework for system level modelling and performance estimation of embedded systems. The framework is simulation based and allows performance estimation to be carried out throughout all design phases ranging from early functional to cycle accurate and bit true descriptions of the system, modelling both hardware and software components in a unied way. Design space exploration and performance estimation is performed by having the framework produce detailed quantitative information about the system model under investigation. The project is part of the national Danish research project, Danish Network of Embedded Systems (DaNES), which is funded by the Danish National Advanced Technology Foundation. The project is carried out in collaboration with the Danish company and DaNES partner, Bang & Olufsen ICEpower. Bang & Olufsen ICEpower provides industrial case studies which will allow the proposed modelling framework to be exercised and assessed in terms of ease of use, production speed, accuracy and efficiency. The framework allows a given embedded system to be constructed and explored before a physical realization is present and it can be used in the design of completely new systems or for modification of legacy systems. The primary benefits of the framework are the possibilities of
exploring a large number of candidate systems within a short time frame leading to better designs, easier design verification through an iterative refinement of the executable system description, and finally the possibility of a reduction of the time-to-market of the design and implementation of the system under consideration. In practice, however, additional time spent on software development in order to provide commercial quality tools supporting the method is required.

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Programming Models and Tools for Intelligent Embedded Systems
Design automation and analysis tools targeting embedded platforms, developed using a component-based design approach, must be able to reason about the capabilities of the platforms. In the general case where nothing is assumed about the components comprising a platform or the platform topology, analysis must be employed to determine its capabilities. This kind of analysis is the subject of this dissertation. The main contribution of this work is the Service Relation Model used to describe and analyze the flow of service in models of platforms and systems composed of reusable components. Fundamental to the service relation model is the novel concept of service aggregation that simply states that one service is accessible through another. The usefulness and versatility of the Service Relation Model is demonstrated by means of three different applications. In the first application, the model is used for checking the consistency of a design with respect to the availability of services and resources. In the second application, a tool for automatically implementing the communication infrastructure of a process network application, the Service Relation Model is used for analyzing the capabilities of a platform and as a basis for efficient code generation. In the third application, the Service Relation Model and the concept of consistency are used to guide an automated procedure for designing systems composed of components.

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Support for Programming Models in Network-on-Chip-based Many-core Systems
This thesis addresses aspects of support for programming models in Network-on-Chip-based many-core architectures. The main focus is to consider architectural support for a plethora of programming models in a single system. The thesis has three main parts. The first part considers parallelization and scalability in an image processing application with the aim
of providing insight into parallel programming issues. The second part proposes and presents the tile-based Clupea many-core architecture, which has the objective of providing configurable support for programming models to allow different programming models to be supported by a single architecture. The architecture features a specialized network interface processor which allows extensive configurability of the memory system. Based on this architecture, a detailed implementation of the cache coherent shared memory programming model is presented. The third part considers modeling and evaluation of the Clupea architecture configured for support for cache coherent shared memory. An analytical model and the MC sim simulator, which provides detailed cycle-accurate simulation of many-core architectures, have been developed for the evaluation of the Clupea architecture. The evaluation shows that configurability causes a moderate increase of the application execution time. Considering the improved flexibility, this impact is considered acceptable as the architecture can potentially exploit application-specific optimizations and offers a valuable platform for comparing programming models.

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BIOLOGICALLY INSPIRED HARDWARE CELL ARCHITECTURE
Disclosed is a system comprising: - a reconfigurable hardware platform; - a plurality of hardware units defined as cells adapted to be programmed to provide self-organization and self-maintenance of the system by means of implementing a program expressed in a programming language defined as DNA language, where each cell is adapted to communicate with one or more other cells in the system, and where the system further comprises a converter program adapted to convert keywords from the DNA language to a binary DNA code; where the self-organisation comprises that the DNA code is transmitted to one or more of the cells, and each of the one or more cells is adapted to determine its function in the system; where if a fault occurs in a first cell and the first cell ceases to perform its function, self-maintenance is performed by that the system transmits information to the cells that the first cell has ceased to perform its function, and then the self-organisation is performed again in order to provide that a second cell undertakes the function of the first cell.

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One of the key design goals in Wireless Sensor Networks is long lasting or even continuous operation. Continuous operation is made possible through energy harvesting. Keeping the network operational imposes a demand to prevent network segmentation and power loss in nodes. It is therefore important that the best energy-wise route is found for each data transfer from a source node to the sink node. We present a new adaptive and distributed routing algorithm for finding energy optimised routes in a wireless sensor network with energy harvesting. The algorithm finds an energy efficient route from each source node to a single sink node, taking into account the current energy status of the network. By simulation, the algorithm is shown to be able to adapt to changes in harvested and stored energy. Simulations show that continuous operation is possible.

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Expressing Inter-task Dependencies between Parallel Stencil Operations

Complex embedded systems are designed under tight constraints on response time, resource usage and cost. Design space exploration tools help designers map and schedule embedded software to complex architectures such as heterogeneous MPSoC's. Task graphs are coarse grained representations of parallel program behaviour which are used to evaluate the feasibility of a particular design. However, automatically extracting an accurate task graph from source code is challenging. This paper investigates how to describe data dependencies to aid tools based on program analysis in extracting task graphs from source code. We will examine a common parallel programming pattern - stencil operations - and show that even for such codes with a regular control flow, the precise dependencies between two stencil operations cannot always be determined at compile time. We introduce a language construct which i) captures an upper bound on the number of dependencies between successive stencil operations and ii) instructs the compiler to generate code which ensures that the bound holds for each execution of the program. The impact of our proposal is evaluated using a micro-benchmark and two soft real-time embedded image processing applications. The coding effort is low - at most one line of code per parallel loop was added. The performance impact is evaluated on a quad-core Linux workstation and we observe no statistically significant slowdown.

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Modelling and Analysis of Embedded Systems Design

We present the MoVES languages: a language with which embedded systems can be specified at a stage in the development process where an application is identified and should be mapped to an execution platform (potentially multicore). We give a formal model for MoVES that captures and gives semantics to the elements of specifications in the MoVES language. We show that even for seemingly simple systems, the complexity of verifying real-time constraints can be overwhelming - but we give an upper limit to the size of the search-space that needs examining. Furthermore, the formal model exposes important scheduling situations that become central in establishing timed-automata models that can be used for analysis of MoVES specifications effectively. Finally we present the MoVES tool, which can conduct automatic verification of interesting properties of MoVES specifications. In several examples, we use the MoVES tool to conduct analysis that identifies timing anomalies. We also conduct design space exploration in an example using the MoVES tool. And we show that it can be used for analysis of systems that, in size, resemble industrially-interesting systems. We find that semantically-based verification is a promising approach for assisting developers of embedded systems. We provide examples of system verifications that, in size and complexity, point in the direction of industrially-interesting systems.
Routing-based Synthesis of Digital Microfluidic Biochips

Microfluidic biochips are replacing the conventional biochemical analyzers, and are able to integrate on-chip all the basic functions for biochemical analysis. The "digital" microfluidic biochips are manipulating liquids not as a continuous flow, but as discrete droplets on a two-dimensional array of electrodes. Basic microfluidic operations, such as mixing and dilution, are performed on the array, by routing the corresponding droplets on a series of electrodes. So far, researchers have assumed that these operations are executed on rectangular virtual devices, formed by grouping several adjacent electrodes. One drawback is that all electrodes are considered occupied during the operation execution, although the droplet uses only one electrode at a time. Moreover, the operations can actually execute by routing the droplets on any sequence of electrodes on the array. Hence, in this paper, we eliminate the concept of virtual modules and allow the droplets to move on the chip on any route during operation execution. Thus, the synthesis problem is transformed into a routing problem. We propose an approach derived from a Greedy Randomized Adaptive Search Procedure (GRASP) and we show that by considering routing-based synthesis, significant improvements can be obtained in the application completion time. The proposed heuristic has been evaluated using two real-life case studies and ten synthetic benchmarks.
System-level modeling and simulation of the cell culture microfluidic biochip ProCell

Microfluidic biochips offer a promising alternative to a conventional biochemical laboratory. There are two technologies for the microfluidic biochips: droplet-based and flow-based. In this paper we are interested in flow-based microfluidic biochips, where the liquid flows continuously through pre-defined micro-channels using valves and pumps. We present an approach to the system-level modeling and simulation of a cell culture microfluidic biochip called ProCell, Programmable Cell Culture Chip. ProCell contains a cell culture chamber, which is envisioned to run 256 simultaneous experiments (viewed as a 16 × 16 matrix). We use an inverted fluorescence microscope to observe the experiments in real-time, allowing kinetic data analysis. We are able to automatically adjust the current experimental setup thus allowing, for the first time, conditional experiments. We propose a biochip architecture model and a comprehensive fault model that captures permanent faults occurring during chip operation. Using the proposed modeling and simulation framework, we perform an architectural level evaluation of two cell culture chamber implementations. A qualitative success metric is also proposed to evaluate chip performance in the presence of partial failures. Our results show that significant improvements in efficiency can be obtained using redundancy, providing improved chances to complete an experiment even in the presence of faults. This decreases the experiment repetition rate while increasing system productivity, saving time and reducing costs.
Tabu Search-based Synthesis of Digital Microfluidic Biochips with Dynamically Reconfigurable Non-rectangular Devices

In this paper we are interested in mixed hard/soft real-time fault-tolerant applications mapped on distributed heterogeneous architectures. We use the Earliest Deadline First (EDF) scheduling for the hard real-time tasks and the Constant Bandwidth Server (CBS) for the soft tasks. The bandwidth reserved for the servers determines the quality of service (QoS) for soft tasks. CBS enforces temporal isolation, such that soft task overruns do not affect the timing guarantees of hard tasks. Transient faults in hard tasks are tolerated using checkpointing with rollback recovery. We have proposed a Tabu Search-based approach for task mapping and CBS bandwidth reservation, such that the deadlines for the hard tasks are satisfied, even in the case of transient faults, and the QoS for the soft tasks is maximized. Researchers have used fixed execution time models, such as the worst-case execution times for hard tasks and average execution times for soft tasks. However, we show that by using stochastic execution times for soft tasks, significant improvements can be obtained. The proposed strategy has been evaluated using an extensive set of benchmarks.

Task Mapping and Bandwidth Reservation for Mixed Hard/Soft Fault-Tolerant Embedded Systems

In this paper we are interested in mixed hard/soft real-time fault-tolerant applications mapped on distributed heterogeneous architectures. We use the Earliest Deadline First (EDF) scheduling for the hard real-time tasks and the Constant Bandwidth Server (CBS) for the soft tasks. The bandwidth reserved for the servers determines the quality of service (QoS) for soft tasks. CBS enforces temporal isolation, such that soft task overruns do not affect the timing guarantees of hard tasks. Transient faults in hard tasks are tolerated using checkpointing with rollback recovery. We have proposed a Tabu Search-based approach for task mapping and CBS bandwidth reservation, such that the deadlines for the hard tasks are satisfied, even in the case of transient faults, and the QoS for the soft tasks is maximized. Researchers have used fixed execution time models, such as the worst-case execution times for hard tasks and average execution times for soft tasks. However, we show that by using stochastic execution times for soft tasks, significant improvements can be obtained. The proposed strategy has been evaluated using an extensive set of benchmarks.
A compositional modelling framework for exploring MPSoC systems
This paper presents a novel compositional framework for system level performance estimation and exploration of Multi-
Processor System On Chip (MPSoC) based systems. The main contributions are the definition of a compositional model
which allows quantitative performance estimation to be carried out throughout all design phases ranging from early
functional specification to actual cycle accurate and bit true descriptions of the system. This is possible, because a
seamless refinement of models is supported by allowing the existence of models described at multiple levels of abstraction
to co-exist and communicate. In order to illustrate the use of the framework, a mobile digital audio processing platform,
supplied by the company Bang & Olufsen ICEpower a/s, is considered.

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A modelling and analysis framework for embedded systems

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Analysis of Quantitative Properties of Hardware Specifications

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Behavioral Synthesis of Asynchronous Circuits Using Syntax Directed Translation as Backend

The current state-of-the art in high-level synthesis of asynchronous circuits is syntax directed translation, which performs a one-to-one mapping of a HDL-description into a corresponding circuit. This paper presents a method for behavioral synthesis of asynchronous circuits which builds on top of syntax directed translation, and which allows the designer to perform automatic design space exploration guided by area or speed constraints. The paper presents an asynchronous implementation template consisting of a data-path and a control unit and its implementation using the asynchronous hardware description language Balsa [1]. This “conventional” template architecture allows us to adapt traditional synchronous synthesis techniques for resource sharing, scheduling, binding etc, to the domain of asynchronous circuits. A prototype tool has been implemented on top of the Balsa framework, and the method is illustrated through the implementation of a set of example circuits. The main contributions of the paper are: the fundamental idea, the template architecture and its implementation using asynchronous handshake components, and the implementation of a prototype tool.
eDNA: A Bio-Inspired Reconfigurable Hardware Cell Architecture Supporting Self-organisation and Self-healing

This paper presents the concept of a biological inspired reconfigurable hardware cell architecture which supports self-organisation and self-healing. Two fundamental processes in biology, namely fertilization-to-birth and cell self-healing have inspired the development of this cell architecture. In biology as well as in our hardware cell architecture it is the DNA which enables these processes. We propose a platform based on the electronic DNA (eDNA) and show through simulation, its capabilities as a new generation of robust reconfigurable hardware platforms. We have created a Java based simulator to simulate our self-organisation and self-healing algorithms and the results obtained from this looks promising.

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eDNA - A Bio-Inspired Reconfigurable Hardware Cell Architecture Supporting Self-organisation and Self-healing.pdf
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**Exploration of a digital audio processing platform using a compositional system level performance estimation framework**

This paper presents the application of a compositional simulation based system-level performance estimation framework on a non-trivial industrial case study. The case study is provided by the Danish company Bang & Olufsen ICEpower a/s and focuses on the exploration of a digital mobile audio processing platform. A short overview of the compositional performance estimation framework used is given followed by a presentation of how it is used for performance estimation using an iterative refinement process towards the final implementation. Finally, an evaluation in terms of accuracy and speed of simulations is discussed based on the presented design flow applied to the case study in question.

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**Formal Verification of an energy aware routing algorithm**

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**Identifying Inter-task Communication in Shared Memory Programming Models**

Modern computers often use multi-core architectures, covering clusters of homogeneous cores for high performance computing, to heterogeneous architectures typically found in embedded systems. To efficiently program such architectures, it is important to be able to par- tition and map programs onto the cores of the architecture. We believe that communication patterns need to become explicit in the source code to make it easier to analyze and partition parallel programs. Extraction of these patterns is difficult to automate due to limitations in compiler techniques when determining the effects of pointers. In this paper, we propose an OpenMP extension which allows programmers to explicitly declare the pointer based data-sharing between coarse-grain program parts. We present a dependency directive, expressing the input
and output relation between program parts and pointers to shared data, as well as a set of runtime operations which are
necessary to enforce declarations made by the programmer. The cost and scalability of the runtime operations are
evaluated using micro-benchmarks and a benchmark from the NAS parallel benchmark suite. The measurements show
that the overhead of the runtime operations is small. In fact, no performance degradation is found when using the runtime
operations in the benchmark from the NAS parallel benchmark suite.

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MoVES - A Framework for Modelling and Verifying Embedded Systems
The MoVES framework is being developed to assist in the early phases of embedded systems design. A system is
modelled as an application running on an execution platform. The application is modelled through the individual tasks, and
the execution platform is modelled through the processing elements, including the operating systems, and their
interconnections. The tasks and processing elements are characterized by their real-time properties. The framework can
be used to conduct schedulability analysis and has the potential to reason about different types of resource usage such as
memory usage and power consumption. A simple specification language for embedded systems and a verification
backend are presented. The framework has a modular, parameterized structure supporting easy extension and adaptation
of the specification language as well as of the verification backend. We show, using a number of small examples, how
MoVES can be used to model and analyze embedded systems.

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**Tabu Search-Based Synthesis of Dynamically Reconfigurable Digital Microfluidic Biochips**

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**Task Migration for Fault-Tolerance in Mixed-Criticality Embedded Systems**
In this paper we are interested in mixed-criticality embedded applications implemented on distributed architectures. Depending on their time-criticality, tasks can be hard or soft real-time and regarding safety-criticality, tasks can be fault-tolerant to transient faults, permanent faults, or have no dependability requirements. We use Earliest Deadline First (EDF) scheduling for the hard tasks and the Constant Bandwidth Server (CBS) for the soft tasks. The CBS parameters determine the quality of service (QoS) of soft tasks. Transient faults are tolerated using checkpointing with roll-back recovery. For tolerating permanent faults in processors, we use task migration, i.e., restarting the safety-critical tasks on other processors. We propose a Greedy-based on-line heuristic for the migration of safety-critical tasks, in response to permanent faults, and the adjustment of CBS parameters on the target processors, such that the faults are tolerated, the deadlines for the hard real-time tasks are satisfied and the QoS for soft tasks is maximized. The proposed online adaptive approach has been evaluated using several synthetic benchmarks and a real-life case study.

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**System-Level Design Methodologies for Networked Multiprocessor Systems-on-Chip**
The first part of the thesis presents an overview of the existing theories and practices of modeling and simulation of multiprocessor systems-on-chip. The systematic categorization of the plethora of existing programming models at various levels of abstraction is the main contribution here which is the first such attempt in the published literature. The second part of the thesis deals with the issues related to the development of system-level design methodologies for networked
multiprocessor systems-on-chip at various levels of design abstraction with special focus on the modeling and design of wireless integrated sensor networks which are an emerging class of networked embedded computer systems. The work described here demonstrates how to model multiprocessor systems-on-chip at the system level by abstracting away most of the lower-level details albeit retaining the parameters most relevant at the system-level. The multiprocessor modeling framework is then extended to include models of networked multiprocessor systems-on-chip which is then employed to model wireless sensor networks both at the sensor node level as well as the wireless network level. In the third and the final part, the thesis covers the issues related to the design, implementation and testing of a system-on-chip-based wireless sensor node development platform, specifically, for the Hogthrob project. This part also deals with the cycle-accurate model of the multiprocessor system-on-chip and its possible extensions to the transaction-level model. The thesis, as a whole makes contributions by describing a design methodology for networked multiprocessor embedded systems at three layers of abstraction from system-level through transaction-level to the cycle accurate level as well as demonstrating it practically by implementing a wireless sensor node design.

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Reconfigurable Architectures: From Physical Implementation to Dynamic Behaviour Modelling

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Adaptive Embedded Systems – Challenges of Run-Time Resource Management
Understanding and efficiently controlling the dynamic behavior of adaptive embedded systems is a challenging endeavor. The challenges come from the often very complicated interplay between the application, the application mapping, and the underlying hardware architecture. With MPSoC, we have the technology to design and fabricate dynamically reconfigurable hardware platforms. However, such platforms will pose new challenges to tools and methods to efficiently explore these platforms at run-time. This talk will address some of the challenges of run-time resource management in adaptive embedded systems.

General information
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A Reactive and Cycle-True IP Emulator for MPSoC Exploration

The design of MultiProcessor Systems-on-Chip (MPSoC) emphasizes intellectual-property (IP)-based communication-centric approaches. Therefore, for the optimization of the MPSoC interconnect, the designer must develop traffic models that realistically capture the application behavior as executing on the IP core. In this paper, we introduce a Reactive IP Emulator (RIPE) that enables an effective emulation of the IP-core behavior in multiple environments, including bit and cycle-true simulation. The RIPE is built as a multithreaded abstract instruction-set processor, and it can generate reactive traffic patterns. We compare the RIPE models with cycle-true functional simulation of complex application behavior (tasksynchronization, multitasking, and input/output operations). Our results demonstrate high-accuracy and significant speedups. Furthermore, via a case study, we show the potential use of the RIPE in a design-space-exploration context.
A service based component model for composing and exploring MPSoC platforms

This paper presents an abstract service based modelling method for use in performance estimation and design space exploration of Multi Processor System On Chip (MPSoC) based systems. The method provides the infrastructure for composing abstract hardware and software models of stream based systems which can be used to produce detailed quantitative information regarding runtime properties of a given system through simulations. The method is based on a service oriented model of computation which is a modified version of Hierarchical Coloured Petri Nets.

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A service based estimation method for MPSoC performance modelling

This paper presents an abstract service based estimation method for MPSoC performance modelling which allows fast, cycle accurate design space exploration of complex architectures including multi processor configurations at a very early stage in the design phase. The modelling method uses a service oriented model of computation based on Hierarchical Colored Petri Nets and allows the modelling of both software and hardware in one unified model. To illustrate the potential of the method, a small MPSoC system, developed at Bang & Olufsen ICEpower a/s, is modelled and performance estimates are produced for various configurations of the system in order to explore the best possible implementation.

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Publication: Research - peer-review › Article in proceedings – Annual report year: 2008

Component-based Service Availability Checking

General information
State: Published
Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling
Authors: Sørensen, P. V. B. (Intern), Madsen, J. (Intern)
Publication date: 2008

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Publisher: Department of Computer Science, Tallinn Technical University
Main Research Area: Technical/natural sciences
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Consistency Check for Component-Based Design of Embedded Systems using SAT-Solving

General information
State: Published
Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling
Authors: Sørensen, P. V. B. (Intern), Madsen, J. (Intern)
Number of pages: 106
Pages: 93-96
Publication date: 2008
Design, Automation, and Test In Europe: The Most Influential Papers of 10 Years DATE

The Design, Automation, and Test in Europe (DATE) conference celebrated in 2007 its tenth anniversary. As a tribute to the chip and system-level design and design technology community, this book presents a compilation of the three most influential papers of each year. This provides an excellent historical overview of the evolution of a domain that contributed substantially to the growth and competitiveness of the circuit electronics and systems industry. The papers were grouped in six sections: - System Level Design; - Networks on Chip; - Modeling, Simulation and Run-Time Management; - Digital Systems in CMOS and Beyond; - Physical Design and Validation; - Test and Verification. The winners of the prestigious EDAA Lifetime Achievement Award as well as other recognized experts in their field wrote an introduction to each section, summarizing the history in their domain and indicating how the selected DATE papers contributed to it.

Models and formal verification of multiprocessor system-on-chips

In this article we develop a model for applications running on multiprocessor platforms. An application is modelled by task graphs and a multiprocessor system is modelled by a number of processing elements, each capable of executing tasks according to a given scheduling discipline. We present a discrete model of computation for such systems and characterize the size of the computation tree it suffices to consider when checking for schedulability. Analysis of multiprocessor system on chips is a major challenge due to the freedom of interrelated choices concerning the application level, the configuration of the execution platform and the mapping of the application onto this platform. The computational model provides a basis for formal analysis of systems. The model is translated to timed automata and a tool for system verification and simulation has been developed using Uppaal as backend. We present experimental results on rather small systems with high complexity, primarily due to differences between best-case and worst-case execution times. Considering worst-case execution times only, the system becomes deterministic and using a special version of {Uppaal}, where the no history is saved, we could verify a smart-phone application consisting of 103 tasks executing on 4 processing elements.
MT-ADRES: multi-threading on coarse-grained reconfigurable architecture

The coarse-grained reconfigurable architecture ADRES (architecture for dynamically reconfigurable embedded systems) and its compiler offer high instruction-level parallelism (ILP) to applications by means of a sparsely interconnected array of functional units and register files. As high-ILP architectures achieve only low parallelism when executing partially sequential code segments, which is also known as Amdahl's law, this article proposes to extend ADRES to MT-ADRES (multi-threaded ADRES) to also exploit thread-level parallelism. On MT-ADRES architectures, the array can be partitioned in multiple smaller arrays that can execute threads in parallel. Because the partition can be changed dynamically, this extension provides more flexibility than a multi-core approach. This article presents details of the enhanced architecture and results obtained from an MPEG-2 decoder implementation that exploits a mix of thread-level parallelism and instruction-level parallelism.

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Embedded Systems Engineering, Freescale Semiconductor, IMEC
Authors: Wu, K. (Intern), Kanstein, A. (Ekstern), Madsen, J. (Intern), Berekovic, M. (Ekstern)
Pages: 761-776
Publication date: 2008
Main Research Area: Technical/natural sciences

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Web of Science (2018): Indexed yes
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Web of Science (2017): Indexed Yes
BFI (2016): BFI-level 1
Scopus rating (2016): SJR 0.279 SNIP 0.67 CiteScore 0.73
BFI (2015): BFI-level 1
Scopus rating (2015): SJR 0.209 SNIP 0.411 CiteScore 0.57
BFI (2014): BFI-level 1
Scopus rating (2014): SJR 0.254 SNIP 0.606 CiteScore 0.59
BFI (2013): BFI-level 1
Scopus rating (2013): SJR 0.289 SNIP 0.702 CiteScore 0.83
ISI indexed (2013): ISI indexed yes
BFI (2012): BFI-level 1
Scopus rating (2012): SJR 0.243 SNIP 0.592 CiteScore 0.65
ISI indexed (2012): ISI indexed yes
BFI (2011): BFI-level 1
Scopus rating (2011): SJR 0.254 SNIP 0.516 CiteScore 0.61
ISI indexed (2011): ISI indexed yes
BFI (2010): BFI-level 1
Scopus rating (2010): SJR 0.214 SNIP 0.412
BFI (2009): BFI-level 1
Scopus rating (2009): SJR 0.284 SNIP 0.455
BFI (2008): BFI-level 1
Scopus rating (2008): SJR 0.329 SNIP 0.595
Web of Science (2008): Indexed yes
Scopus rating (2007): SJR 0.345 SNIP 0.728
Scopus rating (2006): SJR 0.306 SNIP 0.754
Scopus rating (2005): SJR 0.2 SNIP 0.603
Scopus rating (2004): SJR 0.293 SNIP 0.773
Scopus rating (2003): SJR 0.289 SNIP 0.672
Network Traffic Generator Model for Fast Network-on-Chip Simulation

For Systems-on-Chip (SoCs) development, a predominant part of the design time is the simulation time. Performance evaluation and design space exploration of such systems in bit- and cycle-true fashion is becoming prohibitive. We propose a traffic generation (TG) model that provides a fast and effective Network-on-Chip (NoC) development and debugging environment. By capturing the type and the timestamp of communication events at the boundary of an IP core in a reference environment, the TG can subsequently emulate the core's communication behavior in different environments. Access patterns and resource contention in a system are dependent on the interconnect architecture, and our TG is designed to capture the resulting reactiveness. The regenerated traffic, which represents a realistic workload, can thus be used to undertake faster architectural exploration of interconnection alternatives, effectively decoupling simulation of IP cores and of interconnect fabrics. The results with the TG on an AMBA interconnect show a simulation time speedup above a factor of 2 over a complete system simulation, with close to 100% accuracy.

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Embedded Systems Engineering, University of Bologna
Authors: Mahadevan, S. (Intern), Ang, F. (Ekstern), Olsen, R. G. (Ekstern), Sparse, J. (Intern), Madsen, J. (Intern)
Number of pages: 515
Pages: 173-184
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Editors: Lauwereins, R., Madsen, J.
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Main Research Area: Technical/natural sciences
Conference: 2005 Design, Automation and Test in Europe Conference and Exposition , Munich, Germany, 07/03/2005 - 07/03/2005
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NORCHIP

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Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling
Authors: Vesterbacka, M. (Ekstern), Madsen, J. (Intern)
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Publication date: 2008
Main Research Area: Technical/natural sciences

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Journal: IET Computers and Digital Techniques
Volume: 2
Issue number: 4

General information
State: Published
Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling, Operations Research, Department of Management Engineering
Authors: Maftei, E. (Intern), Pop, P. (Intern), Madsen, J. (Intern), Stidsen, T. K. (Intern)
Publication date: 2008

Host publication information
System-level verification of multi-core embedded systems using timed automata

**General information**
State: Published
Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern), Hansen, M. R. (Intern), Knudsen, K. S. (Ekstern), Nielsen, J. E. (Ekstern), Brekling, A. W. (Intern)
Pages: 9302-9307
Publication date: 2008

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Towards Traceability in Descriptive Software Models

**General information**
State: Published
Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling
Authors: Larsen, P. (Intern), Hansen, M. R. (Intern), Madsen, J. (Intern)
Pages: 63-72
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Publisher: Department of Computer Science, Tallinn Technical University
Main Research Area: Technical/natural sciences
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Publication: Research - peer-review › Article in proceedings – Annual report year: 2008

Towards Understanding and Managing the Dynamic Behavior of Run-Time Reconfigurable Architectures

**General information**
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Embedded Systems Engineering, Technical University of Denmark
Authors: Wu, K. (Intern), Hansen, E. R. (Ekstern), Madsen, J. (Intern)
Pages: 97-102
Publication date: 2008

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Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 233393
Three Dimensional Measurements in Medical Data

General information
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Organisations: Department of Informatics and Mathematical Modeling, Image Analysis and Computer Graphics, Computer Science and Engineering
Authors: Jakobsen, B. (Intern), Christensen, N. J. (Intern), Pedersen, S. (Intern), Madsen, J. (Intern)
Publication date: Sep 2007

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Original language: English
Series: IMM-PHD-2008-183
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 210320
Publication: Research › Ph.D. thesis – Annual report year: 2007

ARTS: A SystemC-based framework for multiprocessor Systems-on-Chip modelling
One of the challenges of designing a heterogeneous multiprocessor SoC is to find the right partitioning of the application for the target platform architecture. The right partitioning is dependent on the characteristics of the processors and the network connecting them as well as the application. We present an abstract system-level modelling and simulation framework (ARTS) which allows for cross-layer modelling and analysis covering the application layer, middleware layer, and hardware layer. ARTS allows MPSoC designers to explore and analyze the network performance under different traffic and load conditions, consequences of different task mappings to processors (software or hardware) including memory and power usage, and effects of RTOS selection, including scheduling, synchronization and resource allocation policies. We present the application and platform models of ARTS as well as their implementation in SystemC. We present the usage of the ARTS framework as seen from platform developers' point of view, where new components may be created and integrated into the framework, and from application designers' point of view, where existing components are used to explore possible implementations. The latter is illustrated through a case study of a real-time, smart phone application consisting of 5 applications with a total of 114 tasks mapped onto different platforms. Finally, we discuss the simulation performance of the ARTS framework in relation to scalability.

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Mahadevan, S. (Intern), Virk, K. M. (Intern), Madsen, J. (Intern)
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Main Research Area: Technical/natural sciences

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Scopus rating (2016): SJR 0.182 SNIP 0.702 CiteScore 0.62
BFI (2015): BFI-level 2
Scopus rating (2015): SJR 0.175 SNIP 0.517 CiteScore 0.71
Web of Science (2015): Indexed yes
BFI (2014): BFI-level 2
Scopus rating (2014): SJR 0.154 SNIP 0.28 CiteScore 0.62
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Scopus rating (2013): SJR 0.218 SNIP 0.894 CiteScore 0.67
ISI indexed (2013): ISI indexed yes
BFI (2012): BFI-level 2
Scopus rating (2012): SJR 0.171 SNIP 0.626 CiteScore 0.59
ISI indexed (2012): ISI indexed yes
Web of Science (2012): Indexed yes
BFI (2011): BFI-level 2
Scopus rating (2011): SJR 0.201 SNIP 0.616 CiteScore 0.46
ISI indexed (2011): ISI indexed yes
BFI (2010): BFI-level 2
Scopus rating (2010): SJR 0.306 SNIP 0.828
BFI (2009): BFI-level 2
Scopus rating (2009): SJR 0.167 SNIP 0.388
BFI (2008): BFI-level 2
Scopus rating (2008): SJR 0.258 SNIP 0.498
Scopus rating (2007): SJR 0.12 SNIP 0.492
Web of Science (2007): Indexed yes
Scopus rating (2006): SJR 0.14 SNIP 0.475
Scopus rating (2005): SJR 0.309 SNIP 1.686
Scopus rating (2004): SJR 0.242 SNIP 0.783
Scopus rating (2003): SJR 0.5 SNIP 0.871
Scopus rating (2002): SJR 0.22 SNIP 0.532
Scopus rating (2001): SJR 0.418 SNIP 0.573
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Scopus rating (1999): SJR 0.168 SNIP 0.586
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DOIs:
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Source-ID: 208726
Publication: Research - peer-review › Journal article – Annual report year: 2007

A Traffic injection methodology with support for system-level synchronization

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Mahadevan, S. (Intern), Angiolini, F. (Ekstern), Sparsø, J. (Intern), Benini, L. (Ekstern), Madsen, J. (Intern)
Number of pages: 344
Pages: 145-161
Publication date: 2007

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Publisher: Springer
Editors: Reis, R., Osseiran, A.
ISBN (Print): 978-0-387-73660-0

Series: IFIP International Federation for Information Processing
Number: 240
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 191613
Publication: Research - peer-review › Book chapter – Annual report year: 2007
COSMOS: A System-Level Modelling and Simulation Framework for Coprocessor-Coupled Reconfigurable Systems

Dynamically reconfigurable systems demand complicated run-time management. Due to resource constraints and reconfiguration latencies, efficient reconfiguration strategies that can reduce the overhead cost of dynamic reconfiguration need to be studied. In this paper, we i) propose a reconfigurable task model which extends the classical real-time task model to support the additional states and latencies needed to capture dynamically reconfigurable behavior, ii) propose a coprocessor-coupled reconfigurable architecture which has hardware runtime support for task execution, task reallocation and resource management, and iii) present a SystemC based framework to model and simulate coprocessor-coupled reconfigurable systems. We illustrate how COSMOS may be used to capture the dynamic behavior of such systems and emphasize the need for capturing the system aspects of such systems in order to deal with future design challenges of dynamically reconfigurable systems.

Functional Testing of Wireless Sensor Node Designs

Wireless sensor networks are networked embedded computer systems with stringent power, performance, cost and form-factor requirements along with numerous other constraints related to their pervasiveness and ubiquitousness. Therefore, only a systematic design methodology coupled with an efficient test approach can enable their conformance to design and deployment specifications. We discuss off-line, hierarchical, functional testing of complete wireless sensor nodes containing configurable logic through a combination of FPGA-based board test and Software-Based Self-Test (SBST) techniques. The proposed functional test methodology has been applied to a COTS-based sensor node development platform and can be applied, in general, for testing all types of wireless sensor node designs.
Hardware modelling language and verification of design properties

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Brekling, A. W. (Intern), Hansen, M. R. (Intern), Madsen, J. (Intern)
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Main Research Area: Technical/natural sciences
Conference: Nordic Workshop on Programming Theory 2007, Olso, 01/01/2007
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Publication: Research - peer-review › Article in proceedings – Annual report year: 2007

If Formal Analysis is the Answer – What was the Question?
A key challenge of implementing an embedded systems application on a heterogeneous multiprocessor SoC platform is to find the right mapping of the application onto the platform architecture. The right mapping is dependent on the characteristics of the processors and the network connecting them, as well as the application. As many embedded systems are heavily resource constrained and often safety-critical, there is a strong desire to be able to reason about properties of the system. Although the classical approach of simulation may help us in gaining confidence, it will never be able to make guarantees. However, formal models have promises of being able to give such guarantees – but, can we formally model complex MPSoC systems? And if so, what kind of system properties can we expect to be able to formally verify?

General information
State: Published
Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern)
Publication date: 2007

Publication information
Original language: English
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 233414
Publication: Research › Sound/Visual production (digital) – Annual report year: 2007

MOVES - A tool for Modeling and Verification of Embedded Systems
We demonstrate MOVES, a tool which allows designers of embedded systems to explore possible implementations early in the design process. The demonstration of MOVES will show how designers can explore different designs by changing the mapping of tasks on processing elements, the number and/or speed of processing elements, the size of local memories, and the operating systems (scheduling algorithm).

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Ellebæk, J. (Ekstern), Knudsen, K. S. (Ekstern), Brekling, A. W. (Intern), Hansen, M. R. (Intern), Madsen, J. (Intern)
Publication date: 2007

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Publisher: EEDA
Main Research Area: Technical/natural sciences
MT-ADRES: Multithreading on Coarse-Grained Reconfigurable Architecture
The coarse-grained reconfigurable architecture ADRES (Architecture for Dynamically Reconfigurable Embedded Systems) and its compiler offer high instruction-level parallelism (ILP) to applications by means of a sparsely interconnected array of functional units and register files. As high-ILP architectures achieve only low parallelism when executing partially sequential code segments, which is also known as Amdahl's law, this paper proposes to extend ADRES to MT-ADRES (Multi-Threaded ADRES) to also exploit thread-level parallelism. On MT-ADRES architectures, the array can be partitioned in multiple smaller arrays that can execute threads in parallel. Because the partition can be changed dynamically, this extension provides more flexibility than a multi-core approach. This article presents details of the enhanced architecture and results obtained from an MPEG-2 decoder implementation that exploits a mix of thread-level parallelism and instruction-level parallelism.

General Information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering, Freescale Semiconductor, IMEC
Authors: Wu, K. (Intern), Kanstein, A. (Ekstern), Madsen, J. (Intern), Berekovic, M. (Ekstern)
Pages: 26-38
Publication date: 2007

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Volume: 4419/2007
Publisher: Springer Berlin / Heidelberg
Main Research Area: Technical/natural sciences
DOIs: 10.1007/978-3-540-71431-6
Source: orbit
Source-ID: 209874
Publication: Research - peer-review › Article in proceedings – Annual report year: 2007
Simulation-based Modeling Frameworks for Networked Multi-processor System-on-Chip

This thesis deals with modeling aspects of multi-processor system-on-chip (MpSoC) design affected by the on-chip interconnect, also called the Network-on-Chip (NoC), at various levels of abstraction. To begin with, we undertook a comprehensive survey of research and design practices of networked MpSoC. The survey presents the challenges of modeling and performance analysis of the hardware and the software components used in such devices. These challenges are further exasperated in a mixed abstraction workspace, which is typical of complex MpSoC design environment. We provide two simulation-based frameworks: namely ARTS and RIPE, that allows to model hardware (computation time, power consumption, network latency, caching effect, etc.) and software (application partition and mapping, operating system scheduling, interrupt handling, etc.) aspects from system-level to cycle-true abstraction. Thereby, we can realistically model the application executing on the architecture. This includes e.g. accurate modeling of synchronization, cache refills, context switching effects, etc., which are critically dependent on the architecture and the performance of the NoC. The foundation of the ARTS model is abstract tasks, while the foundation of the RIPE model is cycle-count. For ARTS, using different case-studies with over one hundred tasks (five applications) from the mobile multimedia domain, we show the potential of the framework under real-time constraints. For RIPE, first using six applications we derive the requirements to model the application and the architecture properties independent of the NoC, and then use these applications to successfully validate the approach against a reference cycle-true system. The presence of a standard socket at the intellectual property (IP) and the NoC interface in both the ARTS and the RIPE frameworks allows easy incorporation of IP cores from either frameworks, into a new instance of the design. This could pave the way for seamless design evaluation from system-level to cycle-true abstraction in future component-based MpSoC design practice.
Evolving MPSoC Solutions

A key challenge of implementing an embedded systems application on a heterogeneous multiprocessor SoC platform is to find the right partitioning of the application onto the platform architecture. The right partitioning is dependent on the characteristics of the processors and the network connecting them, as well as the application. We present an evolutionary approach to solve the problem of mapping a set of task graphs onto a heterogeneous multiprocessor platform. The objective is to meet all real-time deadlines subject to minimizing system cost and power consumption, while staying within bounds on local memory sizes and interface buffer sizes. Our approach allows to explore the mapping onto a fixed platform architecture as well as to a flexible platform architecture where architectural changes are explored during the mapping. We demonstrate our approach through an exploration of a smart phone application.
Evolving MPSoC Solutions

A key challenge of implementing an embedded systems application on a heterogeneous multiprocessor SoC platform is to find the right partitioning of the application onto the platform architecture. The right partitioning is dependent on the characteristics of the processors and the network connecting them, as well as the application. We present an evolutionary approach to solve the problem of mapping a set of task graphs onto a heterogeneous multiprocessor platform. The objective is to meet all real-time deadlines subject to minimizing system cost and power consumption, while staying within bounds on local memory sizes and interface buffer sizes. Our approach allows to explore the mapping onto a fixed platform architecture as well as to a flexible platform architecture where architectural changes are explored during the mapping. We demonstrate our approach through an exploration of a smart phone application.

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Madsen, J. (Intern)
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Source-ID: 191592
Publication: Research - peer-review › Article in proceedings – Annual report year: 2006

Extending Lifetime of Wireless Sensor Networks using Forward Error Correction

Communication between nodes in wireless sensor networks (WSN) is susceptible to transmission errors caused by low signal strength or interference. These errors manifest themselves as lost or corrupt packets. This often leads to retransmission, which in turn results in increased power consumption reducing node and network lifetime. In this paper, a convolution code FEC with Viterbi decoding on Mica2 nodes was implemented and evaluated to explore the possibility of extending the lifetime of a degrading WSN. Results were presented which suggest that our approach could be used in a WSN when increasing distance and channel noise degrade the network.

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Authors: Donapudi, S. U. (Ekstern), Obel, C. O. (Ekstern), Madsen, J. (Intern)
Publication date: 2006

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Publisher: IEEE
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Madsen.pdf
DOIs:
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Copyright: 2006 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE
Source: orbit
Source-ID: 253199
Publication: Research - peer-review › Article in proceedings – Annual report year: 2006

Morphware - Fremtidens Embedded System Platform

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Embedded Systems Engineering
Multicore Processing and ARTEMIS - An incentive to develop the European Multiprocessor research

Even though multiprocessor architectures have been developed for a long time now, the approach was mostly focusing on multi-chip realizations. Clustering computers or micro-processors on the same board was the solution to manage complex applications vs. performance requirements. It is only in the recent period that technological advances allow for a change of this paradigm towards on-chip distributed platforms, or multi-core, or multi processor system-on-chip (MPSOC). A multiprocessor architecture may be defined as: onchip clusters of heterogeneous functionality modules, cooperating in the implementation of multiple concurrent applications. Architecturally, MPSOC combine characteristics from both distributed (DS) and on-chip systems (SOC). However, addressing issues from either one of these later paradigms will not necessarily bring optimal benefits to MPSOC. For instance, in MPSOC, differently to a traditional SOC view, concurrency at all levels plays a deterministic role, while problems such as power consumption, addressable separately in the nodes of a DS, must be unitary considered. Thus, distinct research and development issues must be defined for MPSOC, building on the indispensable experience in DS and SOC, and other related domains. Primarily motivated by market concerns, and also by the promises of the available billion transistor technology, MPSOC is increasingly becoming the preferred target for embedded systems (ES) implementations. Furthermore, the possibility to fit a huge number of different applications onto such a platform, poses important challenges to the realization of such systems. Leaving long time ago the application specific approach, the domain specific solution will soon also become insufficient as an application mapping paradigm, due to the increasing interaction between separate areas of the same industrial field, or even between distinct industrial domains (such as photo-mobile-phones, in car / on plane / on train multimedia systems, to cite just a few of the most popular ones).

Multi-Objective Design Space Exploration of Embedded System Platforms

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Madsen, J. (Intern), Stidsen, T. K. (Intern), Kjærulff, P. (Intern), Mahadevan, S. (Intern)
Publication date: 2006
Multi-Objective Design Space Exploration of Embedded System Platforms
In this paper we present a multi-objective genetic algorithm to solve the problem of mapping a set of task graphs onto a heterogeneous multiprocessor platform. The objective is to meet all real-time deadlines subject to minimizing system cost and power consumption, while staying within bounds on local memory sizes and interface buffer sizes. Our approach allows for mapping onto a fixed platform or onto a flexible platform where architectural changes are explored during the mapping. We demonstrate our approach through an exploration of a smart phone, where five task graphs with a total of 530 tasks after hyper period extension are mapped onto a multiprocessor platform. The results show four non-inferior solutions which tradeoffs the various objectives.

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling, Operations Research, Arcanic A/S
Authors: Madsen, J. (Intern), Stidsen, T. K. (Intern), Kjærluff, P. (Intern), Mahadevan, S. (Intern)
Publication date: 2006

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Source: orbit
Source-ID: 200969
Publication: Research - peer-review › Report – Annual report year: 2006

Multi-Objective Design Space Exploration of Embedded System Platforms
In this paper we present a multi-objective genetic algorithm to solve the problem of mapping a set of task graphs onto a heterogeneous multiprocessor platform. The objective is to meet all real-time deadlines subject to minimizing system cost and power consumption, while staying within bounds on local memory sizes and interface buffer sizes. Our approach allows for mapping onto a fixed platform or onto a flexible platform where architectural changes are explored during the mapping. We demonstrate our approach through an exploration of a smart phone, where five task graphs with a total of 530 tasks after hyper period extension are mapped onto a multiprocessor platform. The results show four non-inferior solutions which tradeoffs the various objectives.

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling, Operations Research
Authors: Madsen, J. (Intern), Stidsen, T. K. (Intern), Kjærluff, P. (Intern), Mahadevan, S. (Intern)
Pages: 185-194
Publication date: 2006

Host publication information
Volume: IFIP International Federation for Information Processing , Vol. 225
Place of publication: Berlin
Publisher: Springer
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 196102
Publication: Research - peer-review › Book chapter – Annual report year: 2007

A Network Traffic Generator Model for Fast Network-on-Chip Simulation
For Systems-on-Chip (SoCs) development, a predominant part of the design time is the simulation time. Performance evaluation and design space exploration of such systems in bit- and cycle-true fashion is becoming prohibitive. We propose a traffic generation (TG) model that provides a fast and effective Network-on-Chip (NoC) development and debugging environment. By capturing the type and the timestamp of communication events at the boundary of an IP core in a reference environment, the TG can subsequently emulate the core’s communication behavior in different environments. Access patterns and resource contention in a system are dependent on the interconnect architecture, and our TG is designed to capture the resulting reactivity. The regenerated traffic, which represents a realistic workload,
can thus be used to undertake faster architectural exploration of interconnection alternatives, effectively decoupling simulation of IP cores and of interconnect fabrics. The results with the TG on an AMBA interconnect show a simulation time speedup above a factor of 2 over a complete system simulation, with close to 100% accuracy.

**General information**

**State:** Published

**Organisations:** Computer Science and Engineering, Department of Informatics and Mathematical Modeling

**Authors:** Mahadevan, S. (Intern), Angiolini, F. (Ekstern), Storgaard, M. (Ekstern), Olsen, R. (Ekstern), Sparsø, J. (Intern), Madsen, J. (Intern)

**Pages:** 780-785

**Publication date:** 2005

**Host publication information**

**Title of host publication:** Design, Automation and Test in Europe

**ISBN (Print):** 0-7695-2288-2

**Main Research Area:** Technical/natural sciences

**Conference:** 2005 Design, Automation and Test in Europe Conference and Exposition, Munich, Germany, 07/03/2005 - 07/03/2005

**Electronic versions:**

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DOIs:

10.1109/DATE.2005.22

**Bibliographical note**

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Source: orbit

Source-ID: 185716

Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

**ARTS: A System-Level Framework for Modeling MPSoC Components and Analysis of their Causality**

Designing complex heterogeneous multiprocessor System on Chip (MPSoC) requires support for modeling and analysis of the different layers i.e. application, operating system (OS) and platform architecture. This paper presents an abstract system-level modeling framework, called ARTS, to support the MPSoC designers in modeling the different layers and understanding their causalities. While others have developed tools for static analysis and modeled limited correlations (processor-memory or processor-communication), our model captures the impact of dynamic and unpredictable OS behaviour on processor, memory and communication performance. In particular, we focus on analyzing the impact of application mapping on the processor and memory utilization taking the on-chip communication latency into account. A case-study of real-time multimedia application consisting of 114 tasks on a 6-processor platform for a handheld terminal shows our frameworks co-exploration capabilities.

**General information**

**State:** Published

**Organisations:** Computer Science and Engineering, Department of Informatics and Mathematical Modeling

**Authors:** Mahadevan, S. (Intern), Storgaard, M. (Ekstern), Madsen, J. (Intern), Virk, K. M. (Intern)

**Publication date:** 2005

**Host publication information**

**Title of host publication:** 13th IEEE International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems (MASCOTS)

**Publisher:** IEEE Computer Society Press

**ISBN (Print):** 0-7695-2458-3

**Main Research Area:** Technical/natural sciences

**Conference:** 13th IEEE International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems (MASCOTS), 01/01/2005

**Electronic versions:**

Mahadevan.pdf

DOIs:

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**Bibliographical note**

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Behavioral synthesis of asynchronous circuits

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling, System-on-Chip Hardware, Embedded Systems Engineering
Authors: Nielsen, S. F. (Intern), Sparsø, J. (Intern), Madsen, J. (Intern)
Publication date: 2005

Publication information
Original language: English
Series: IMM-PHD-2005-144
Main Research Area: Technical/natural sciences
Electronic versions:
imm3866.ps
imm3866.pdf
Links:
http://www2.imm.dtu.dk/pubdb/p.php?3866
Source: orbit
Source-ID: 185930
Publication: Research › Ph.D. thesis – Annual report year: 2005

Cross-layer Modelling for Heterogeneous MPSoCs

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Madsen, J. (Intern)
Publication date: 2005

Host publication information
Title of host publication: Multiprocessor System-on-Chip Symposium
Main Research Area: Technical/natural sciences
Conference: Multiprocessor System-on-Chip Symposium, 01/01/2005
Links:
http://www2.imm.dtu.dk/pubdb/p.php?4206
Source: orbit
Source-ID: 185795
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

Design of A Development Platform for HW/SW Codesign of Wireless IOnintegrated Sensor Nodes

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Virk, K. M. (Intern), Leopold, M. (Ekstern), Madsen, J. (Intern), Bonnet, P. (Ekstern), Hansen, M. (Ekstern)
Publication date: 2005

Host publication information
Title of host publication: EUROMICRO Symposium on Digital System Design
Main Research Area: Technical/natural sciences
Links:
http://www2.imm.dtu.dk/pubdb/p.php?3920
Source: orbit
Source-ID: 185766
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005
Design Space Exploration for Heterogeneous, Networked MPSoC Design (Invited talk)

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern)
Publication date: 2005

Host publication information
Title of host publication: ARTIST Workshop on Distributed Embedded Systems
Main Research Area: Technical/natural sciences
Conference: ARTIST Workshop on Distributed Embedded Systems, 01/01/2005
Links:
http://www2.imm.dtu.dk/pubdb/p.php?4207
Source: orbit
Source-ID: 185793
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

Modular SoC-Design using the MANGO clockless NoC (Invited talk)

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Bjerregaard, T. (Intern), Sparsø, J. (Intern), Mahadevan, S. (Intern), Madsen, J. (Intern)
Publication date: 2005

Host publication information
Title of host publication: International Conference on Parallel Computing (PARCO'05)
Place of publication: PARCO
Publisher: PARCO
Main Research Area: Technical/natural sciences
Conference: International Conference on Parallel Computing (PARCO'05), 01/01/2005
Links:
http://www2.imm.dtu.dk/pubdb/p.php?3919
Source: orbit
Source-ID: 185785
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

Multiprocessor Systems - Modelling and Simulation

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern), Virk, K. M. (Intern)
Pages: 388-405
Publication date: 2005

Host publication information
Title of host publication: Embedded Systems Design: The ARTIST Roadmap for Research and Development : Lecture Notes in Computer Science
Publisher: Springer
Main Research Area: Technical/natural sciences
Links:
http://www2.imm.dtu.dk/pubdb/p.php?3916
Source: orbit
Source-ID: 185810
Publication: Research - peer-review › Book chapter – Annual report year: 2005

Realistically Rendering SoC Traffic Patterns with Interrupt Awareness

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Angiolini, F. (Ekstern), Mahadevan, S. (Ekstern), Madsen, J. (Intern), Benini, L. (Ekstern), Sparsø, J. (Intern)
Run-time Dynamic Reconfiguration: A Reality Check Based on FPGA Architectures from Xilinx

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Wu, K. (Intern), Madsen, J. (Intern)
Publication date: 2005

Host publication information
Title of host publication: NORCHIP Conference, 2005. 23rd
Main Research Area: Technical/natural sciences
Links:
Source: orbit
Source-ID: 185767
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

Sensor Networks: Towards Ambient Intelligence

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Madsen, J. (Intern)
Publication date: 2005

Host publication information
Title of host publication: DIAG Conference
Main Research Area: Technical/natural sciences
Conference: DIAG Conference, 01/01/2005
Links:
http://www2.imm.dtu.dk/pubdb/p.php?4208
Source: orbit
Source-ID: 185794
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

System-level Modeling of Wireless Integrated Sensor Networks

Wireless integrated sensor networks have emerged as a promising infrastructure for a new generation of monitoring and tracking applications. In order to efficiently utilize the extremely limited resources of wireless sensor nodes, accurate modeling of the key aspects of wireless sensor networks is necessary so that system-level design decisions can be made about the hardware and the software (applications and real-time operating system) architecture of sensor nodes. In this paper, we present a SystemC-based abstract modeling framework that enables system-level modeling of sensor network behavior by modeling the applications, real-time operating system, sensors, processor, and radio transceiver at the sensor node level and environmental phenomena, including radio signal propagation, at the sensor network level. We demonstrate the potential of our modeling framework by simulating and analyzing a small sensor network configuration.

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Virk, K. M. (Intern), Hansen, K. (Ekstern), Madsen, J. (Intern)
Publication date: 2005

Host publication information
System-Level Modelling and Simulation of MEMS-Based Sensors

The growing complexity of MEMS devices and their increased use in embedded systems (e.g., wireless integrated sensor networks) demands a disciplined approach for MEMS design as well as the development of techniques for system-level modeling of these devices so that a seamless integration with the existing embedded system design methodologies is possible. In this paper, we present a MEMS design methodology that uses VHDL-AMS based system-level model of a MEMS device as a starting point and combines the top-down and bottom-up design approaches for design, verification, and optimization. The capabilities of our proposed design methodology are illustrated through the design of a microaccelerometer.

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling, MicroNano Tribology and Modeling, Department of Micro- and Nanotechnology
Authors: Virk, K. M. (Intern), Madsen, J. (Intern), Shafique, M. (Intern), Menon, A. K. (Intern)
Publication date: 2005

Host publication information
Title of host publication: 9th IEEE International Multi-Topic Conference (INMIC)
Publisher: IEEE
ISBN (Print): 0-7803-9429-1
Main Research Area: Technical/natural sciences
Conference: 9th IEEE International Multi Topic Conference, Karachi, Pakistan, December 23-25, 2005, 01/01/2005
VHDL-AMS, Reduced-Order Model, Sensors, MEMS, SystemC, ystem-Level Model, Microaccelerometer, Wireless Sensor Networks
Electronic versions:
Madsen.pdf
DOIs:
10.1109/INMIC.2005.334503

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Source: orbit
Source-ID: 185763
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

The SoC-Mobinet Model in System-on-Chip Education

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Nurmi, J. (Ekstern), Madsen, J. (Intern), Ofner, E. (Ekstern), Isoaho, J. (Ekstern), Tenhunen, H. (Ekstern)
Publication date: 2005

Host publication information
Abstract System-on-Chip modelling in SystemC

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern), Virk, K. M. (Intern), Mahadevan, S. (Intern)
Publication date: 2004

Host publication information
Title of host publication: European SystemC Users Group Meeting (DATE 2004)
Main Research Area: Technical/natural sciences
Links:
Source: orbit
Source-ID: 154687
Publication: Research › Article in proceedings – Annual report year: 2004

A SystemC-Based Abstract Real-Time Operating System Model for Multiprocessor System-on-Chip

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern), Virk, K. M. (Intern), Gonzalez, M. J. (Ekstern)
Publication date: 2004

Host publication information
Title of host publication: Multiprocessor System-on-Chip
Publisher: Morgan Kaufmann
ISBN (Print): 0-12-385251-X
Main Research Area: Technical/natural sciences
Links:
Source: orbit
Source-ID: 154726
Publication: Research - peer-review › Book chapter – Annual report year: 2004

A system-level multiprocessor system-on-chip modeling framework
We present a system-level modeling framework to model system-on-chips (SoC) consisting of heterogeneous multiprocessors and network-on-chip communication structures in order to enable the developers of today’s SoC designs to take advantage of the flexibility and scalability of network-on-chip and rapidly explore high-level design alternatives to meet their system requirements. We present a modeling approach for developing high-level performance models for these SoC designs and outline how this system-level performance analysis capability can be integrated into an overall environment for efficient SoC design. We show how a hand-held multimedia terminal, consisting of JPEG, MP3 and GSM applications, can be modeled as a multiprocessor SoC in our framework.

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Virk, K. M. (Intern), Madsen, J. (Intern)
Publication date: 2004

Host publication information
Publisher: IEEE
ISBN (Print): 0-7803-8558-6
A system-level multiprocessor system-on-chip modelling framework

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Virk, K. M. (Intern), Madsen, J. (Intern)
Publication date: 2004

Design of a multi-mode channel-select and resampling-processor (ASIP)

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Blaickner, A. (Ekstern), Madsen, J. (Intern), Holten-Lund, H. E. (Intern), Bacher, M. (Ekstern)
Publication date: 2004

Network-Centric System-Level Model for Multiprocessor System-on-Chip Simulation

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern), Mahadevan, S. (Intern), Virk, K. M. (Intern)
Publication date: 2004
SoC-Mobinet, R&D and Education in System-on-Chip

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Ofner, E. (Ekstern), Nurmi, J. (Ekstern), Madsen, J. (Intern), Isoaho, J. (Ekstern), Tenhuen, H. (Ekstern)
Publication date: 2004

Host publication information
Title of host publication: International Symposium on System-on-Chip
Main Research Area: Technical/natural sciences
Links:
Source: orbit
Source-ID: 154651
Publication: Research - peer-review › Article in proceedings – Annual report year: 2004

System-level modeling for Wireless Sensor Networks (Invited talk)

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern)
Publication date: 2004

Host publication information
Title of host publication: MPSoC 2004, Saint-Maximin la Sainte Baume, France
Main Research Area: Technical/natural sciences
Links:
Source: orbit
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Publication: Research - peer-review › Article in proceedings – Annual report year: 2004

System-on-Chip Design Challenges for Future Embedded Systems (Invited talk)

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern)
Publication date: 2004

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Title of host publication: DATE 2004 Workshop on Embedded Systems Research in Europe
Main Research Area: Technical/natural sciences
Links:
Source: orbit
Source-ID: 154699
Publication: Research - peer-review › Article in proceedings – Annual report year: 2004

Towards behavioral synthesis of asynchronous circuits - an implementation template targeting syntax directed compilation

This paper presents a method for behavioral synthesis of asynchronous circuits. Our approach aims at providing a synthesis flow which is very similar to what is found in existing synchronous design tools. We adapt the synchronous behavioral synthesis abstraction into the asynchronous handshake domain by introducing a computation model, which resembles the synchronous datapath and control architecture, but which is completely asynchronous. The datapath and control architecture is then expressed in the Balsa-language, and using syntax directed compilation a corresponding handshake circuit implementation is produced. The paper also reports area, speed and power figures for a couple of
benchmark circuits, which have been synthesized to layout.

**General information**

State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Nielsen, S. F. (Intern), Sparsø, J. (Intern), Madsen, J. (Intern), Selvaraj, H. (ed.) (Ekstern)
Publication date: 2004

**Host publication information**

Title of host publication: EUROMICRO Symposium on Digital System Design
Publisher: IEEE
ISBN (Print): 0-7695-2203-3
Main Research Area: Technical/natural sciences
Conference: Euromicro Symposium on Digital System Design, 01/01/2004
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Source: orbit
Source-ID: 154641
Publication: Research - peer-review › Article in proceedings – Annual report year: 2004

**Wireless Sensor Networks for Sow Monitoring (Invited talk)**

**General information**

State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern)
Publication date: 2004

**Host publication information**

Title of host publication: CCCD Workshop 2004 Future Systems and Requirements, Lund
Main Research Area: Technical/natural sciences
Links:
Source: orbit
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Publication: Research - peer-review › Article in proceedings – Annual report year: 2004

**Abstract RTOS Modelling for Multiprocessor System-on-Chip**

**General information**

State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern), Virk, K. M. (Intern), Gonzalez, M. J. (Ekstern)
Pages: 147-150
Publication date: 2003

**Host publication information**

Title of host publication: International Symposium on System-on-Chip
Publisher: IEEE
Main Research Area: Technical/natural sciences
Links:
Source: orbit
Source-ID: 58542
Publication: Research - peer-review › Article in proceedings – Annual report year: 2003
Network-on-Chip Modeling for System-Level Multiprocessor Simulation

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern), Mahadevan, S. (Intern), Virk, K. M. (Intern), Gonzalez, M. J. (Ekstern)
Pages: 265-274
Publication date: 2003

Host publication information
Title of host publication: The 24th IEEE International Real-Time Systems Symposium
Publisher: IEEE Computer Society Press
Main Research Area: Technical/natural sciences
Links:
Source: orbit
Source-ID: 58541
Publication: Research - peer-review › Article in proceedings – Annual report year: 2003

Power Constrained High-Level Synthesis of Battery Powered Digital Systems
We present a high-level synthesis algorithm solving the combined scheduling, allocation and binding problem minimizing area under both latency and maximum power per clock-cycle constraints. Our approach eliminates the large power spikes, resulting in an increased battery lifetime, a property of utmost importance for battery powered embedded systems. Our approach extends the partial-clique partitioning algorithm by introducing power awareness through a heuristic algorithm which bounds the design space to those of power feasible schedules. We have applied our algorithm on a set of dataflow graphs and investigated the impact on circuit area when applying different power constraints.

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Nielsen, S. F. (Intern), Madsen, J. (Intern)
Pages: 1136-1137
Publication date: 2003

Host publication information
Title of host publication: DATE 2003
Publisher: IEEE
Main Research Area: Technical/natural sciences
Conference: 2003 Design, Automation and Test in Europe Conference and Exposition, Munich, Germany, 03/03/2003 - 03/03/2003
Electronic versions:
Madsen.pdf

Bibliographical note
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Source: orbit
Source-ID: 58548
Publication: Research - peer-review › Article in proceedings – Annual report year: 2003

Resource Allocation Model for Modelling Abstract RTOS on Multiprocessor System-on-Chip
Resource Allocation is an important problem in RTOS's, and has been an active area of research. Numerous approaches have been developed and many different techniques have been combined for a wide range of applications. In this paper, we address the problem of resource allocation in the context of modelling an abstract RTOS on multiprocessor SoC platforms. We discuss the implementation details of a simplified basic priority inheritance protocol for our abstract system model in SystemC.

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Virk, K. M. (Intern), Madsen, J. (Intern)
Pages: 48-51
Publication date: 2003
Using SystemC to Model Asynchronous Communication at Different Levels of Abstraction

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Mahadevan, S. (Intern), Bjerregaard, T. (Intern), Sparsø, J. (Intern), Madsen, J. (Intern)
Publication date: 2003

Design for scalability in 3D computer graphics architectures
This thesis describes useful methods and techniques for designing scalable hybrid parallel rendering architectures for 3D computer graphics. Various techniques for utilizing parallelism in a pipelines system are analyzed. During the Ph.D study a prototype 3D graphics architecture named Hybris has been developed. Hybris is a prototype rendering architecture which can be tailored to many specific 3D graphics applications and implemented in various ways. Parallel software implementations for both single and multi-processor Windows 2000 system have been demonstrated. Working hardware/software codesign implementations of Hybris for standard-cell based ASIC (simulated) and FPGA technologies have been demonstrated, using manual co-synthesis for translation of a Virtual Prototyping architecture specification written in C into both optimized C source for software and into a synthesizable VHDL specification for hardware implementation. A flexible VRML 97 3D scene graph engine with a Java interface and C++ interface has been implemented to allow flexible integration of the rendering technology into Java and C++ applications. A 3D medical visualization workstation prototype (3D-Med) is examined as a case study and an application of the Hybris graphics architecture.

Abstract RTOS modelling in SystemC

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Abstract RTOS modelling in SystemC

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern), Gonzalez, M. J. (Ekstern), Blaickner et al., A. (ed.) (Ekstern)
Publication date: 2002

A Sophomore Course in Codesign
We teach a hardware and software codesign course to second-year students who have expressed an interest in either electronics or informatics (computer science). The course emphasizes concepts and methods that are useful to both hardware and software developers and in particular to developers of embedded systems who must consider both disciplines as well as their interaction. We consider the course to be part of a search for better development methods and hope to increase the number of professional developers.
High-level synthesis of asynchronous circuits from control data flow graph representations

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Nielsen, S. F. (Intern), Sparsø, J. (Intern), Madsen, J. (Intern), Hammerstoft, J. (Ekstern), Hansen, J. S. (Ekstern)
Publication date: 2002

Host publication information
Title of host publication: Second ACiD-WG Workshop (of the european commission's fifth framework programme), Munich, Germany 28-29 January
Main Research Area: Technical/natural sciences
Links: http://www.scism.sbu.ac.uk/ccsv/ACiD-WG/Workshop2FP5/Programme/

Bibliographical note
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Source: orbit
Source-ID: 58101
Publication: Research - peer-review › Journal article – Annual report year: 2002

DOIs: 10.1109/MC.2002.1046983
SoC-Mobinet - A project for Collaborative System-on-Chip Curricula Development with Industrial Support

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Nurmi, J. (Ekstern), Isoaho, J. (Ekstern), Tenhunen, H. (Ekstern), Madsen, J. (Intern), Ofner, E. (Ekstern), Nielsen, I. R. (Ekstern)
Publication date: 2002

Host publication information
Title of host publication: Proceedings of the 4th European Workshop on Microelectronics Education, EWME
Main Research Area: Technical/natural sciences
Links:
Source: orbit
Source-ID: 58213
Publication: Research - peer-review › Article in proceedings – Annual report year: 2002

Power-over-Time Estimation for Processor Design

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Borum, K. (Ekstern), Gleerup, T. M. (Intern), Madsen, J. (Intern), Pedersen, S. (Intern)
Publication date: 2001

Host publication information
Title of host publication: Proceedings of NORCHIP'01
Main Research Area: Technical/natural sciences
Links:
Source: orbit
Source-ID: 57828
Publication: Research - peer-review › Article in proceedings – Annual report year: 2001

Embedded System Education for the Future

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling, Princeton University
Authors: Wolf, W. (Ekstern), Madsen, J. (Intern)
Pages: 23-30
Publication date: 2000
Main Research Area: Technical/natural sciences

Publication information
Journal: Proceedings of the IEEE
Volume: 88
Issue number: 1
Original language: English
Source: orbit
Source-ID: 175772
Publication: Research - peer-review › Journal article – Annual report year: 2000

Memory architecture for efficient utilization of SDRAM: a case study of the computation/memory access trade-off
This paper discusses the trade-off between calculations and memory accesses in a 3D graphics tile renderer for visualization of data from medical scanners. The performance requirement of this application is a frame rate of 25 frames per second when rendering 3D models with 2 million triangles, i.e. 50 million triangles per second, sustained (not peak). At present, a software implementation is capable of 3-4 frames per second for a 1 million triangle model. By using direct evaluation of certain interpolation parameters instead of forward differencing, writing back parameters to SDRAM is avoided. In software, forward differencing is usually better, but in this hardware implementation, the trade-off has made it possible to develop a very regular memory architecture with a buffering system, which can reach 95% bandwidth utilization using off-the-shelf SDRAM. This is achieved by changing the algorithm to use a memory access strategy with write-only and read-only phases, and a buffering system, which uses round-robin bank write-access combined with burst
VRML Visualization in a Surgery Planning and Diagnostics Application

This paper analyzes how the high-level languages Java and VRML can be used for 3D medical imaging and simulation on a PC.
Embedded System Synthesis under Memory Constraints

This paper presents a genetic algorithm to solve the system synthesis problem of mapping a time constrained single-rate system specification onto a given heterogeneous architecture which may contain irregular interconnection structures. The synthesis is performed under memory constraints, that is, the algorithm takes into account the memory size of processors and the size of interface buffers of communication links, and in particular the complicated interplay of these. The presented algorithm is implemented as part of the LY-COS cosynthesis system.

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern), Bjørn-Jørgensen, P. (Intern)
Pages: 188-192
Publication date: 1999

Host publication information
Title of host publication: Proceedings of the Seventh International Workshop on Hardware/Software Codesign, 1999. (CODES '99)
Place of publication: New York
Publisher: IEEE
ISBN (Print): 1-58113-132-1
Main Research Area: Technical/natural sciences
Conference: 7th International Workshop on Hardware/Software Codesign, Rome, Italy, 03/05/1999 - 03/05/1999
Electronic versions:
Madsen.pdf
DOIs:
10.1109/HSC.1999.777430

Bibliographical note
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Source: orbit
Source-ID: 175514
Publication: Research - peer-review › Article in proceedings – Annual report year: 1999

Graph based communication analysis for hardware/software codesign

In this paper we present a coarse grain CDFG (Control/Data Flow Graph) model suitable for hardware/software partitioning of single processes and demonstrate how it is necessary to perform various transformations on the graph structure before partitioning in order to achieve a structure that allows for accurate estimation of communication overhead between nodes mapped to different processors. In particular, we demonstrate how various transformations of control structures can lead to a more accurate communication analysis and more efficient implementations. The purpose of the transformations is to obtain a CDFG structure that is sufficiently fine grained as to support a correct communication analysis but not more fine grained than necessary as this will increase partitioning and analysis time.

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Knudsen, P. V. (Intern), Madsen, J. (Intern)
Pages: 131-135
Publication date: 1999

Host publication information
Title of host publication: Proceedings of the Seventh International Workshop on Hardware/Software Codesign, 1999. (CODES '99)
Place of publication: New York
Publisher: IEEE
ISBN (Print): 1-58113-132-1
Main Research Area: Technical/natural sciences
Conference: 7th International Workshop on Hardware/Software Codesign, Rome, Italy, 03/05/1999 - 03/05/1999
Electronic versions:
Knudsen.pdf
DOIs:
10.1109/HSC.1999.777407
Integrating communication protocol selection with hardware/software codesign

General information
State: Published
Organisations: Department of Information Technology, Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Knudsen, P. V. (Intern), Madsen, J. (Intern)
Pages: 1077-1095
Publication date: 1999
Conference: Unknown, 01/01/1999
Main Research Area: Technical/natural sciences

Publication information
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Ratings:
BFI (2018): BFI-level 1
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 1
Web of Science (2017): Indexed yes
BFI (2016): BFI-level 1
Scopus rating (2016): CiteScore 2.72 SJR 0.486 SNIP 1.816
Web of Science (2016): Indexed yes
BFI (2015): BFI-level 1
Scopus rating (2015): SJR 0.619 SNIP 1.658 CiteScore 2.41
BFI (2014): BFI-level 1
Scopus rating (2014): SJR 0.598 SNIP 1.915 CiteScore 2.18
BFI (2013): BFI-level 1
Scopus rating (2013): SJR 0.665 SNIP 1.853 CiteScore 2.27
ISI indexed (2013): ISI indexed yes
Web of Science (2013): Indexed yes
BFI (2012): BFI-level 1
Scopus rating (2012): SJR 0.65 SNIP 1.513 CiteScore 1.88
ISI indexed (2012): ISI indexed yes
BFI (2011): BFI-level 2
Scopus rating (2011): SJR 0.784 SNIP 1.595 CiteScore 2.08
ISI indexed (2011): ISI indexed yes
BFI (2010): BFI-level 2
Scopus rating (2010): SJR 0.775 SNIP 1.441
BFI (2009): BFI-level 1
Scopus rating (2009): SJR 0.878 SNIP 1.693
BFI (2008): BFI-level 2
Scopus rating (2008): SJR 0.889 SNIP 1.614
Web of Science (2008): Indexed yes
Scopus rating (2007): SJR 0.861 SNIP 1.765
Scopus rating (2006): SJR 0.847 SNIP 1.968
Web of Science (2006): Indexed yes
A Unified Component Modeling Approach for Performance Estimation in Hardware/Software Codesign

This paper presents an approach for abstract modeling of hardware/software architectures using Hierarchical Colored Petri Nets. The approach is able to capture complex behavioral characteristics often seen in software and hardware architectures, thus it is suitable for high level codesign issues such as performance estimation. In this paper, the development of a model of the ARM7 processor [5] is described to illustrate the full potential of the modeling approach. To further illustrate the approach, a cache model is also described. The approach and related tools are currently being implemented in the LYCOS system [12]. Details and the basic characteristics of the approach can be found in [8].

Communication Estimation for Hardware/Software Codesign

This paper presents a general high level estimation model of communication throughput for the implementation of a given communication protocol. The model, which is part of a larger model that includes component price, software driver object code size and hardware driver area, is intended to be general enough to be able to capture the characteristics of a wide range of communication protocols and yet to be sufficiently detailed as to allow the designer or design tool to efficiently explore tradeoffs between throughput, bus widths, burst/non-burst transfers and data packing strategies. Thus it provides a basis for decision making with respect to communication protocols/components and communication driver design in the initial design space exploration phase of a co-synthesis process where a large number of possibilities must be examined and where fast estimators are therefore necessary. The fill model allows for additional (money) cost, software code size and hardware area tradeoffs to be examined.
Hardware Resource Allocation for Hardware/Software Partitioning in the LYCOS System
This paper presents a novel hardware resource allocation technique for hardware/software partitioning. It allocates hardware resources to the hardware data-path using information such as data-dependencies between operations in the application, and profiling information. The algorithm is useful as a designer's/design tool's aid to generate good hardware allocations for use in hardware/software partitioning. The algorithm has been implemented in a tool under the LYCOS system. The results show that the allocations produced by the algorithm come close to the best allocations obtained by exhaustive search.

Integrating communication protocol selection with partitioning in hardware/software codesign
This paper explores the problem of determining the characteristics of the communication links in a computer system as well as determining the best functional partitioning. In particular, we present a communication estimation model and show, by the use of this model, the importance of integrating communication protocol selection with hardware/software partitioning. The communication estimation model allows for fast estimation but is still sufficiently detailed as to allow the designer or design tool to efficiently explore tradeoffs between throughputs, bus widths, burst/nonburst transfers, operating
frequencies of system components such as buses, CPU's, ASIC's, software code size, hardware area, and component prices. A distinct feature of the model is the modeling of driver processing of data (packing, splitting, compression, etc.) and its impact on communication throughput. The integration of communication protocol selection and communication driver design with hardware/software partitioning is illustrated by a number of design space exploration experiments carried out within the LYCOS cosynthesis system, using models of the PCI and USB protocols.

General information
State: Published
Organisations: Department of Information Technology, Computer Science and Engineering
Authors: Knudsen, P. V. (Intern), Madsen, J. (Intern)
Pages: 111-116
Publication date: 1998

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ISBN (Print): 0-8186-8623-5
Main Research Area: Technical/natural sciences
Conference: 11th International Symposium on System Synthesis, Hsinchu, Taiwan, 01/01/1998
Electronic versions:
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Bibliographical note
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Source: orbit
Source-ID: 170456
Publication: Research - peer-review › Article in proceedings – Annual report year: 1998

Performance Estimation for Hardware/Software Codesign

General information
State: Published
Organisations: Department of Information Technology, Technical University of Denmark, TIMA Laboratory
Authors: Grode, J. (Ekstern), Madsen, J. (Intern), Jerraya, A. (Ekstern)
Publication date: 1998

Host publication information
Title of host publication: Proceedings of the International Symposium on High Performance Computing
Main Research Area: Technical/natural sciences
Conference: International Symposium on High Performance Computing, Boston, USA, 01/01/1998
Source: orbit
Source-ID: 170460
Publication: Research - peer-review › Article in proceedings – Annual report year: 1998

Performance Estimation for Hardware/Software codesign using Hierarchical Colored Petri Nets

General information
State: Published
Organisations: Department of Information Technology, Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Grode, J. N. R. (Intern), Madsen, J. (Intern), Jerraya, A. (Ekstern)
Publication date: 1998

Host publication information
Title of host publication: Proceedings of the International Symposium on High Performance Computing, HPC'98
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 200099
Publication: Research - peer-review › Article in proceedings – Annual report year: 1998
Virtual Prototyping, a Case Study in Dataflow Oriented Codesign.
The main topic of this paper is a discussion of the design process we have used during development of an application specific computer system. We will focus on a case study involving a 3D computer graphics system we are currently developing, and how such a system can be optimized for speed. The paper focuses on (em how) a design is developed, in order to satisfy a set of requirements. In particular, we discuss the importance of always having a running software prototype of the entire system available. This software prototype also serves as the main medium for experimenting with new ideas for the algorithms, and the partitioning of computation blocks, memory and communication channels to either hardware or software. We call this process (em Virtual Prototyping), during which we are able to apply transformations to the design, eg. (em Loop Fusion) and (em Strip Mining) to improve data locality. An interesting consequence of this is that at the system integration scale the optimizations we perform to achieve good hardware performance, are in fact also contributing to improving the execution speed of the software prototype.

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering, Olicom
Authors: Holten-Lund, H. E. (Intern), Lütken, M. (Ekstern), Madsen, J. (Intern), Pedersen, S. (Intern)
Publication date: 1998

Host publication information
Title of host publication: Poster presentation at the 6th International Workshop on Hardware/Software Codesign
Main Research Area: Technical/natural sciences
Conference: CODES/CASHE '98, Seattle, Washington [USA], 01/01/1998
Source: orbit
Source-ID: 167711
Publication: Research - peer-review › Article in proceedings – Annual report year: 1998

Virtual Prototyping, A Method for Hardware/Software Codesign

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Holten-Lund, H. E. (Intern), Madsen, J. (Intern), Pedersen, S. (Intern)
Pages: 222-229
Publication date: 1998

Host publication information
Title of host publication: Proceedings of NORCHIP'98
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 200155
Publication: Research - peer-review › Article in proceedings – Annual report year: 1998

A Case Study of a Hybrid Parallel 3D Surface Rendering Graphics Architecture
This paper presents a case study in the design strategy used in building a graphics computer for drawing very complex 3D geometric surfaces. The goal is to build a PC based computer system capable of handling surfaces built from about 2 million triangles, and to be able to render a perspective view of these on a computer display at interactive frame rates, i.e. processing around 50 million triangles per second. The paper presents a hardware/software architecture called HPGA (Hybrid Parallel Graphics Architecture) which is likely to be able to carry out this task. The case study focuses on techniques to increase the clock frequency as well as the parallelism of the system. This paper focuses on the back-end graphics pipeline, which is responsible for rasterizing triangles, with a practically linear increase in performance. A pure software implementation of the proposed architecture is currently able to process 300,000 triangles per second on a Pentium PC, which compares favorably to other software renderers (e.g. OpenGL) and most add-on PC hardware renderers.

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Computer Science and Engineering
Authors: Holten-Lund, H. E. (Intern), Madsen, J. (Intern), Pedersen, S. (Intern)
Publication date: 1997

Host publication information
Title of host publication: SASIMI ’97 Proceedings
Main Research Area: Technical/natural sciences
Critical Path Driven Cosynthesis for Heterogeneous Target Architectures
This paper presents a critical path driven algorithm to produce a static schedule of a single-rate system onto a heterogeneous target architecture. Our algorithm is a list based scheduling algorithm which concurrently assigns tasks to processors and allocates nets to interprocessor communication. Experimental results show that our algorithm is able to find good results, as compared to other methods, in small amount of CPU time.
The Importance of Interfaces: A HW/SW Codesign Case Study

This paper presents a codesign case study in image analysis. The main objective is to stress the importance of handling HW/SW interfaces more precisely at the system level. In the presented case study, there is an intuitive and simple HW/SW interface, which is based upon the functional modules in the application. However, it is found that this seemingly sound choice caused a number of practical problems and sub-optimal solutions during the implementation of the prototype system.

Aspects of system modelling in Hardware/Software partitioning

This paper addresses fundamental aspects of system modelling and partitioning algorithms in the area of Hardware/Software Codesign. Three basic system models for partitioning are presented and the consequences of partitioning according to each of these are analyzed. The analysis shows the importance of making a clear distinction between the model used for partitioning and the model used for evaluation. It also illustrates the importance of having a realistic hardware model such that hardware sharing can be taken into account. Finally, the importance of integrating scheduling and allocation with partitioning is demonstrated.
Codesign Analysis of a Computer Graphics Application

This paper describes a codesign case study where a computer graphics application is examined with the intention to speed up its execution. The application is specified as a C program, and is characterized by the lack of a simple compute-intensive kernel. The hardware/software partitioning is based on information obtained from software profiling and the resulting design is validated through cosimulation. The achieved speed-up is estimated based on an analysis of profiling information from different sets of input data and various architectural options.

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling, DELTA
Authors: Madsen, J. (Intern), Brage, J. P. (Ekstern)
Pages: 121-145
Publication date: 1996
Main Research Area: Technical/natural sciences

Publication information
Journal: Design Automation of Embedded Systems
Volume: 1
Issue number: 1-2
Original language: English
Source: orbit
Source-ID: 166187
Publication: Research - peer-review › Journal article – Annual report year: 1996

PACE: A dynamic programming algorithm for hardware/software partitioning

This paper presents the PACE partitioning algorithm which is used in the LYCOS co-synthesis system for partitioning control/dataflow graphs into hardware and software parts. The algorithm is a dynamic programming algorithm which solves both the problem of minimizing system execution time with a hardware area constraint and the problem of minimizing hardware area with a system execution time constraint. The target architecture consists of a single microprocessor and a single hardware chip (ASIC, FPGA, etc.) which are connected by a communication channel. The algorithm incorporates a realistic communication model and thus attempts to minimize communication overhead. The time-complexity of the algorithm is \(O(n^2 \cdot \text{Ascr})\) and the space-complexity is \(O(n \cdot \text{Ascr})\) where \(\text{Ascr}\) is the total area of the hardware chip and \(n\) the number of code fragments which may be placed in either hardware or software.

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Knudsen, P. V. (Intern), Madsen, J. (Intern)
Pages: 85-92
Publication date: 1996

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Title of host publication: Proceedings. Fourth International Workshop on Hardware/Software Co-Design (Code/CASHE ’96)
Publisher: IEEE
ISBN (Print): 0-8186-7243-9
Main Research Area: Technical/natural sciences
Conference: Fourth International Workshop on Hardware/Software Co-Design (Code/CASHE ’96), Pittsburgh, Pennsylvania, USA, 01/01/1996
Electronic versions:
An Approach to Interface Synthesis

Presents a novel interface synthesis approach based on a one-sided interface description. Whereas most other approaches consider interface synthesis as optimizing a channel to existing client/server modules, we consider the interface synthesis as part of the client/server module synthesis (which may contain the re-use of existing modules). The interface synthesis approach describes the basic transformations needed to transform the server interface description into an interface description on the client side of the communication medium. The synthesis approach is illustrated through a point-to-point communication, but is applicable to synthesis of a multiple client/server environment. The interface description is based on a formalization of communication events.
A Codesign Case Study in Computer Graphics
The paper describes a codesign case study where a computer graphics application is examined with the intention to speed up its execution. The application is specified as a C program, and is characterized by the lack of a simple compute-intensive kernel. The hardware/software partitioning is based on information obtained from software profiling and the resulting design is validated through cosimulation. A locally developed interface model, Merlin, is used as the basis for cosimulation. The achieved speed-up is estimated based on an analysis of profile information.

A Flexible Architecture Representation for High Level Synthesis

Bibliographical note
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Modeling Shared Variables in VHDL
A set of concurrent processes communicating through shared variables is an often used model for hardware systems. This paper presents three modeling techniques for representing such shared variables in VHDL, depending on the acceptable constraints on accesses to the variables. Also a set of guidelines for handling atomic updates of multiple shared variables is given.

1. Introduction
It is often desirable to partition a computational system into discrete functional units which cooperates to.

Controller Synthesis and Verification

Deferral Based List Scheduling

Performance Aspects of Gate Matrix Layout
A New Layout Model For Automatic Gate Matrix Layout Generation

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Hald, B. G. (Ekstern), Madsen, J. (Intern)
Controller Synthesis Using Compiled Cells

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern), Hald, B. G. (Ekstern)
Publication date: 1992

Host publication information
Title of host publication: Proceedings of the NORCHIP Seminar'92
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 200110
Publication: Research › peer-review › Article in proceedings – Annual report year: 1992

Layout Synthesis using Compiled Cells

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern)
Publication date: 1992

Host publication information
Title of host publication: Proceedings of the NORCHIP Seminar'92
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 200220
Publication: Research › peer-review › Article in proceedings – Annual report year: 1992

Controller Synthesis in GAIA, A VHDL RT-Level Framework

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Pallisgaard, H. (Ekstern), Andersen, O. C. (Ekstern), Linqvist, L. (Ekstern), Madsen, J. (Intern)
Publication date: 1991

Host publication information
Title of host publication: Proceedings of the Second European Conference on VHDL Methods, EuroVHDL'91
Main Research Area: Technical/natural sciences
Source: orbit
Source-ID: 200313
Publication: Research › peer-review › Article in proceedings – Annual report year: 1991

Delay estimation for CMOS functional cells

Presents a new RC tree network model for delay estimation of CMOS functional cells. The model is able to reflect topological changes within a cell, which is of particular interest when doing performance driven layout synthesis. Further, a set of algorithms to perform worst case analysis on arbitrary CMOS functional cells using the proposed delay model, is presented. Both model and algorithms have been implemented as a part of a cell compiler (CELLO) working in an experimental silicon compiler environment.
Single-Level Wiring for CMOS Functional Cells

Flow Graph Modelling Using VHDL Bus Resolution Functions

Flow Graph Modelling Using VHDL Bus Resolution Functions
Novel Architecture Design Methodologies and Synthesis Strategies for Future ASIC Design

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern)
Publication date: 1990

Host publication information
Title of host publication: Proceedings of the 5th NORSILC/NORCHIP Seminar'90
Main Research Area: Technical/natural sciences
Seminar: 5th NORSILC/NORCHIP Seminar'90, Lund, Sweden, 30/10/1990 - 30/10/1990
Source: orbit
Source-ID: 200227
Publication: Research - peer-review › Article in proceedings – Annual report year: 1990

The Impact of Novel Algorithms, Architectural design Methodologies and Synthesis Strategies on Future ASIC Design

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern)
Publication date: 1990

Host publication information
Title of host publication: Proceedings of the ESPRIT Technical Conference
Main Research Area: Technical/natural sciences
Conference: Proceedings of the ESPRIT Technical Conference, 01/01/1990
Source: orbit
Source-ID: 200226
Publication: Research - peer-review › Article in proceedings – Annual report year: 1990

A New Approach to Optimal Cell Synthesis
A set of algorithms is presented for optimal layout generation of CMOS complex gates. The algorithms are able to handle global physical constraints, such as pin placement, and to capture timing aspects. Results show that this novel approach provides better solutions in area and speed compared to other methods. The algorithms have been implemented in a cell compiler (CELLO) working in an experimental silicon compiler environment.

General information
State: Published
Organisations: Computer Science and Engineering, Department of Information Technology
Authors: Madsen, J. (Intern)
Publication date: 1989

Host publication information
Title of host publication: Proceedings of the IEEE International Conference on Computer-Aided Design, ICCAD-89
Publisher: IEEE
ISBN (Print): 0-8186-1986-4
Main Research Area: Technical/natural sciences
Conference: International Conference on Computer-Aided Design, Santa Clara, CA, 01/01/1989
Electronic versions:
Jan.pdf
DOIs:
10.1109/ICCAD.1989.76965

Bibliographical note
Automatic Synthesis of Multilevel Combinational Logic

This paper describes a system for the synthesis of multilevel combinational logic, transforming functional description into mask layout. The system includes a logic synthesis part, partly consisting of tools developed at Eindhoven University of Technology, which has been interfaced to the layout synthesis part in the CATOE-system, developed at the DesignCenter of Electronics Institute. The various steps in the transformation are presented together with a complete design example, implementing a multi-output combinational decoder function.

A Dynamic Environment for VLSI Design Tools

This paper describes a system for the synthesis of multilevel combinational logic, transforming functional description into mask layout. The system includes a logic synthesis part, partly consisting of tools developed at Eindhoven University of Technology, which has been interfaced to the layout synthesis part in the CATOE-system, developed at the DesignCenter of Electronics Institute. The various steps in the transformation are presented together with a complete design example, implementing a multi-output combinational decoder function.
Digital Design Using Module Generators

General information
State: Published
Organisations: Computer Science and Engineering, Department of Informatics and Mathematical Modeling
Authors: Madsen, J. (Intern), Stassen, F. (Intern)
Publication date: 1986

Host publication information
Title of host publication: Proceedings of the 2nd NORSILC/NORCHIP Seminar
Main Research Area: Technical/natural sciences
Conference: Proceedings of the 2nd NORSILC/NORCHIP Seminar, 01/01/1986
Source: orbit
Source-ID: 200231
Publication: Research - peer-review › Article in proceedings – Annual report year: 1986

Projects:

Fog Computing Security
Technical University of Denmark
Period: 01/11/2017 → 31/10/2020
Number of participants: 3
Phd Student:
Kavaja, Juxhino (Ekstern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Dragoni, Nicola (Intern)

Financing sources
Source: Internal funding (public)
Name of research programme: Marie Curie (EU-stipendium)
Project: PhD

Fog Computing Security
Technical University of Denmark
Period: 01/11/2017 → 31/10/2020
Number of participants: 3
Phd Student:
Kavaja, Juxhino (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Dragoni, Nicola (Intern)

Financing sources
Source: Internal funding (public)
Name of research programme: Marie Curie (EU-stipendium)
Project: PhD

Resource Management in Fog Computing for Industrial Applications
Department of Applied Mathematics and Computer Science
Period: 01/08/2017 → 30/09/2017
Number of participants: 3
Phd Student:
Raagaard, Michael Lander (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Pop, Paul (Intern)

Financing sources
Source: Internal funding (public)
Name of research programme: Institut stipendie (DTU)
Project: PhD

Portable Diagnostic Laboratory to Diagnose Thyroid Gland Related Disorders
Department of Applied Mathematics and Computer Science
Period: 01/07/2017 → 30/06/2020
Number of participants: 4
Phd Student:
Tanev, Georgi Plamenov (Intern)
Supervisor:
Schjøler, Karin (Ekstern)
Svendsen, Winnie Edith (Intern)
Main Supervisor:
Madsen, Jan (Intern)

Financing sources
Source: Internal funding (public)
Name of research programme: Samfinansieret - Andet
Project: PhD

Analysis and Optimization of safety-Critical Embedded Systems
Department of Applied Mathematics and Computer Science
Period: 01/07/2015 → 30/06/2016
Number of participants: 3
Phd Student:
Laursen, Sune Mølgaard (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Pop, Paul (Intern)

Financing sources
Source: Internal funding (public)
Name of research programme: Anden EU-finansiering
Project: PhD

Compilation Techniques for Flow-based Microfluidic Biochips
Department of Applied Mathematics and Computer Science
Period: 15/06/2015 → 14/06/2018
Number of participants: 3
Phd Student:
Schneider, Alexander Rüdiger (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Pop, Paul (Intern)

Financing sources
**COMPUTE Software Group**

Many researchers create tools that could be very valuable to a broader audience. Using them, however, is often impeded by the required expertise and/or effort. This project aims at providing services to all of DTU Compute to help them make their tools and available to the world.

Our goal is to reach out to science and industry to promote the use of the tools and datasets we have created, and thus advance scientific progress at large and its economic dissemination. On a smaller scale, the individual stakeholders each will benefit in turn:

- Compute will benefit from increased visibility and newly established contacts and created collaboration opportunities,
- The sections will benefit by having more insight into the activities of other sections,
- Individual researchers can benefit by more citations and higher visibility.

**Department of Applied Mathematics and Computer Science**

**Software Engineering**

**Embedded Systems Engineering**

**Statistics and Data Analysis**

**Period:** 01/01/2015 → 31/12/2015

**Number of participants:** 4

**Acronym:** CSG

**Project participant:**

- Störrle, Harald (Intern)
- Madsen, Jan (Intern)
- Ersbøll, Bjarne Kjær (Intern)
- Kristensen, Kristian (Intern)

**Project**

A top-down approach to genetic circuit synthesis

**Department of Applied Mathematics and Computer Science**

**Period:** 15/08/2014 → 15/11/2017

**Number of participants:** 5

**Phd Student:**

- Baig, Hasan (Intern)

**Main Supervisor:**

- Madsen, Jan (Intern)

**Examiner:**

- Hansen, Michael Reichhardt (Intern)
- Bhatia, Swapnil (Ekstern)
- Myers, Chris John (Ekstern)

**Financing sources**

**Source:** Internal funding (public)

**Name of research programme:** Institut stipendie (DTU)

**Relations**

**Publications:**

Methods and Tools for the Analysis, Verification and Synthesis of Genetic Logic Circuits,

**Project:** PhD

**Simulation of distributed system with thermodynamic models**

**Department of Applied Mathematics and Computer Science**

**Period:** 01/04/2014 → 01/10/2017

**Number of participants:** 2

**Phd Student:**
Pedersen, Nicolai (Intern)
Main Supervisor:
Madsen, Jan (Intern)

**Financing sources**
Source: Internal funding (public)
Name of research programme: Samfinansierede - Virksomhed

**Relations**
Publications:
Co-Simulation of Cyber-Physical System with Distributed Embedded Control
Project: PhD

**Test-driven model-based development of complex embedded systems**
Department of Applied Mathematics and Computer Science
Period: 01/08/2013 → 16/08/2017
Number of participants: 8
Phd Student:
Munck, Allan (Intern)
Supervisor:
Lindqvist, Lars (Intern)
Mortensen, René (Ekstern)
Pop, Paul (Intern)
Main Supervisor:
Madsen, Jan (Intern)
Examiner:
Karlsson, Sven (Intern)
Larsen, Peter Gorm (Ekstern)
Nielsen, Peter Østergaard (Ekstern)

**Financing sources**
Source: Internal funding (public)
Name of research programme: Industrial PhD

**Relations**
Publications:
Test-Driven, Model-Based Systems Engineering.
Project: PhD

**Evolvable Smartphone-based Point-of-Care Systems for In-Vitro Diagnostics**
Department of Micro- and Nanotechnology
Period: 01/02/2013 → 02/11/2016
Number of participants: 7
Phd Student:
Patou, François (Intern)
Supervisor:
Dimaki, Maria (Intern)
Madsen, Jan (Intern)
Main Supervisor:
Svendsen, Winnie Edith (Intern)
Examiner:
Pop, Paul (Intern)
Romano-Rodriguez, Albert (Ekstern)
Shah, Pranjul Jaykumar (Intern)

**Financing sources**
Source: Internal funding (public)
Name of research programme: Marie Curie (EU-stipendium)
Relations
Publications:
Evolvable Smartphone-Based Point-of-Care Systems For In-Vitro Diagnostics
Project: PhD

Portable and predictable Performance Heterogeneous Embedded Manycores - Low Level System Stack
Department of Applied Mathematics and Computer Science
Period: 15/01/2013 → 01/12/2016
Number of participants: 6
Phd Student:
Brock-Nannestad, Laust (Intern)
Supervisor:
Probst, Christian W. (Intern)
Main Supervisor:
Karlsson, Sven (Intern)
Examiner:
Madsen, Jan (Intern)
Brorsson, Mats (Ekstern)
Själander, Magnus (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: 1/3 FUU, 1/3 inst 1/3 Andet
Project: PhD

Modelling and analysis for Cyber-Physical Systems
Department of Applied Mathematics and Computer Science
Period: 01/11/2011 → 30/09/2015
Number of participants: 6
Phd Student:
Dung, Phan Anh (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Hansen, Michael Reichhardt (Intern)
Examiner:
Haxthausen, Anne Elisabeth (Intern)
Sestoft, Peter (Intern)
Vain, Jüri (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: 1/3 FUU, 1/3 inst 1/3 Andet
Project: PhD

Optimized Networking for Energy Harvesting Wireless Sensor Network
Department of Applied Mathematics and Computer Science
Period: 01/03/2011 → 30/09/2014
Number of participants: 6
Phd Student:
Vuckovic, Dusan (Intern)
Supervisor:
Sørensen, Thomas (Ekstern)
Main Supervisor:
Madsen, Jan (Intern)
Examiner:
Dragoni, Nicola (Intern)
Ellervee, Peeter (Ekstern)
Nielsen, Peter Østergaard (Ekstern)

**Financing sources**
Source: Internal funding (public)
Name of research programme: Ansat eksternt
Project: PhD

**Optimized Networking for Energy Harvesting Wireless Sensor Networks**
Department of Applied Mathematics and Computer Science
Period: 01/12/2010 → 26/05/2014
Number of participants: 6
Phd Student:
Fafoutis, Xenofon (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Dragoni, Nicola (Intern)
Examiner:
Nannarelli, Alberto (Intern)
Plosila, Juha Petteri (Ekstern)
Vain, Jüri (Ekstern)

**Financing sources**
Source: Internal funding (public)
Name of research programme: Institut stipendie (DTU)
Project: PhD

**Multi-objective Design Space Exploration for (re)-configurable heterogeneous Multi-ASIP SoC platforms**
Department of Applied Mathematics and Computer Science
Period: 01/11/2010 → 23/01/2015
Number of participants: 6
Phd Student:
Micconi, Laura (Intern)
Supervisor:
Pop, Paul (Intern)
Main Supervisor:
Madsen, Jan (Intern)
Examiner:
Sparsø, Jens (Intern)
Pimentel, Andrew David (Ekstern)
Sander, Ingo (Ekstern)

**Financing sources**
Source: Internal funding (public)
Name of research programme: 1/3 FUU, 1/3 inst 1/3 Andet
Project: PhD

**Design Space Exploration for Application Mapping onto onto Heterogeneous Multiprocessor ASIPs**
Department of Applied Mathematics and Computer Science
Period: 15/10/2010 → 15/05/2011
Number of participants: 3
Phd Student:
Iordache, George Valentin (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Pop, Paul (Intern)
Financing sources
Source: Internal funding (public)
Name of research programme: 1/3 FUU, 1/3 inst 1/3 Andet
Project: PhD

Synthesis of Mixed-Criticality Applications on Multi-Core Systems to Reduce Certification Costs
Department of Applied Mathematics and Computer Science
Period: 01/09/2010 → 20/03/2014
Number of participants: 6
Phd Student:
Tamas-Selicean, Domitian (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Pop, Paul (Intern)
Examiner:
Schoeberl, Martin (Intern)
Ademaj, Astrit (Ekstern)
Chakraborty, Samarjit (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: 1/3 FUU, 1/3 inst 1/3 Andet
Project: PhD

Architecture concepts for improving programmability of multi-core architectures
Department of Applied Mathematics and Computer Science
Period: 15/06/2010 → 26/05/2014
Number of participants: 6
Phd Student:
Schleuniger, Pascal (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Karlsson, Sven (Intern)
Examiner:
Pop, Paul (Intern)
Grahn, Håkan (Ekstern)
Ramirez, Alex (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: Forskningsrådsfinansiering
Project: PhD

Design Methods for Droplet-Based Microfluidic Biochips with Operation Variability
Department of Applied Mathematics and Computer Science
Period: 01/01/2010 → 24/06/2014
Number of participants: 6
Phd Student:
Alistar, Mirela (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Pop, Paul (Intern)
Examiner:
Bille, Philip (Intern)
System-Level Design to Support Early Design Stages and Evolvable Development of Embedded Systems

Department of Applied Mathematics and Computer Science
Period: 15/12/2009 → 26/05/2014
Number of participants: 6
PhD Student:
Gan, Junhe (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Pop, Paul (Intern)
Examiner:
Nannarelli, Alberto (Intern)
Curescu, Calin (Ekstern)
Popentiu, Florin (Intern)

Financing sources
Source: Internal funding (public)
Name of research programme: Institut stipendie (DTU)
Project: PhD

Adaptable communication middleware for network on a chip based multi core architectures

Department of Informatics and Mathematical Modeling
Period: 01/10/2009 → 09/04/2013
Number of participants: 3
PhD Student:
Passas, Stavros (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Karlsson, Sven (Intern)

Financing sources
Source: Internal funding (public)
Name of research programme: 1/3 FUU, 1/3 inst 1/3 Andet
Project: PhD

System-Level Design of Continuous Flow Microfluidic Biochips

Department of Informatics and Mathematical Modeling
Period: 15/09/2009 → 07/03/2013
Number of participants: 6
PhD Student:
Minhass, Wajid Hassan (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Pop, Paul (Intern)
Examiner:
Nannarelli, Alberto (Intern)
Catthoor, Francky (Ekstern)
Chakrabarty, Krishnendu (Ekstern)

**Financing sources**
Source: Internal funding (public)
Name of research programme: Forskningsrådsfinansiering
Project: PhD

**Nordplus Framework Programme for Higher Education**
Nordic Master School in Innovative Information and Communication Technologies
Department of Applied Mathematics and Computer Science

Embedded Systems Engineering
Period: 01/09/2009 → 31/08/2013
Number of participants: 3
Acronym: NMS iICT
Project participant:
Stassen, Flemming (Intern)
Pop, Paul (Intern)
Madsen, Jan (Intern)

**Relations**
Activities:
Nordic Master School in Innovative ICT (NMS iICT) (External organisation)

**Formal methods for design and simulation of embedded systems**
Department of Informatics and Mathematical Modeling
Period: 01/06/2009 → 30/08/2013
Number of participants: 6
Phd Student:
Jakobsen, Mikkel Koefoed (Intern)
Supervisor:
Hansen, Michael Reichhardt (Intern)
Main Supervisor:
Madsen, Jan (Intern)
Examiner:
Dragoni, Nicola (Intern)
Plosila, Juha Petteri (Ekstern)
Vain, Jüri (Ekstern)

**Financing sources**
Source: Internal funding (public)
Name of research programme: 1/3 FUU, 1/3 inst 1/3 Andet
Project: PhD

**Analysis and Optimization of Embedded Systems**
Department of Informatics and Mathematical Modeling
Period: 01/08/2008 → 30/11/2010
Number of participants: 3
Phd Student:
Saraswat, Prabhat Kumar (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Pop, Paul (Intern)

**Financing sources**
Source: Internal funding (public)
Name of research programme: Institut stipendie (DTU) Samf.
Adaptability and Autonomy in Embedded Systems

Department of Informatics and Mathematical Modeling
Period: 01/06/2008 → 28/09/2011
Number of participants: 6
PhD Student:
Boesen, Michael Reibel (Intern)
Supervisor:
Pop, Paul (Intern)
Main Supervisor:
Madsen, Jan (Intern)
Examiner:
Sparsø, Jens (Intern)
Codinachs, David Merodio (Ekstern)
Tempesti, Gianluca (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: Offentlig finansiering
Project: PhD

A Framework for Modeling, Simulation ans Design Space Exploration of Digital Microfluidic Biochips

Department of Informatics and Mathematical Modeling
Period: 01/02/2008 → 31/08/2011
Number of participants: 6
PhD Student:
Maftei, Elena (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Pop, Paul (Intern)
Examiner:
Nannarelli, Alberto (Intern)
Chakrabarty, Krishnendu (Ekstern)
Peng, Zebo (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: Institut stipendie (DTU)
Project: PhD

A Flexible Audio SoC Design Methodology

Department of Informatics and Mathematical Modeling
Period: 01/12/2007 → 31/08/2011
Number of participants: 5
PhD Student:
Tranberg-Hansen, Anders Sejer (Intern)
Main Supervisor:
Madsen, Jan (Intern)
Examiner:
Pop, Paul (Intern)
Eles, Petru (Ekstern)
Lindwer, Menno (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: Offentlig finansiering
Power and Thermal Management of System-on-chips

Department of Informatics and Mathematical Modeling
Period: 15/10/2007 → 01/06/2011
Number of participants: 6
Phd Student:
Liu, Wei (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Nannarelli, Alberto (Intern)
Examiner:
Pop, Paul (Intern)
Alonso, David Atienza (Ekstern)
Tisserand, Arnaud (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: DTU-lønnet stipendie
Project: PhD

 Qualitative and Quantitative Security Analyses for ZigBee Wireless Sensor Networks

Department of Informatics and Mathematical Modeling
Period: 01/09/2007 → 30/03/2011
Number of participants: 6
Phd Student:
Yuksel, Ender (Intern)
Supervisor:
Nielsen, Flemming (Intern)
Main Supervisor:
Nielsen, Hanne Riis (Intern)
Examiner:
Madsen, Jan (Intern)
Gilmore, Stephen (Ekstern)
Martinelli, Fabio (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: DTU-lønnet stipendie
Project: PhD

 Models and Analyses for Embedded Systems Design

Department of Informatics and Mathematical Modeling
Period: 01/04/2007 → 02/02/2011
Number of participants: 6
Phd Student:
Brekling, Aske Wiid (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Hansen, Michael Reichhardt (Intern)
Examiner:
Sparso, Jens (Intern)
Ravn, Anders P. (Intern)
Vain, Juuri (Ekstern)
Financing sources
Source: Internal funding (public)
Name of research programme: Forskningsrådsfinansiering
Project: PhD

Tools for model-based software descriptions
Department of Informatics and Mathematical Modeling
Period: 01/02/2007 → 31/08/2011
Number of participants: 6
Phd Student:
Larsen, Per (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Karlsson, Sven (Intern)
Examiner:
Probst, Christian W. (Intern)
Cohen, Albert (Ekstern)
Stenström, Per (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: DTU-lønnet stipendie
Project: PhD

Systemarkitekturer baseret på Network-on-Chip
Department of Informatics and Mathematical Modeling
Period: 01/10/2006 → 29/09/2010
Number of participants: 7
Phd Student:
Rasmussen, Morten Sleth (Intern)
Supervisor:
Karlsson, Sven (Intern)
Madsen, Jan (Intern)
Main Supervisor:
Sparsø, Jens (Intern)
Examiner:
Probst, Christian W. (Intern)
Grahn, Håkan (Ekstern)
Nurmi, Jari Antero (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: DTU-lønnet stipendie

Relations
Publications:
Support for Programming Models in Network-on-Chip-based Many-core Systems
Project: PhD

Physical Models and Robust Estimation in Sensor Network Security
Department of Informatics and Mathematical Modeling
Period: 01/05/2006 → 31/08/2006
Number of participants: 2
Phd Student:
Rasmussen, Kasper Bonne (Intern)
Main Supervisor:
Madsen, Jan (Intern)
Financing sources
Source: Internal funding (public)
Name of research programme: Forskningsrådsfinansiering
Project: PhD

Programming Models and Tools for Intelligent Embedded Systems
Department of Informatics and Mathematical Modeling
Period: 01/03/2006 → 29/09/2010
Number of participants: 5
Phd Student:
Sørensen, Peter Verner Bojsen (Intern)
Main Supervisor:
Madsen, Jan (Intern)
Examiner:
Jensen, Christian D. (Intern)
Jerraya, Ahmed Amine (Ekstern)
Svensson, Bertil (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: DTU-lønnet stipendie
Project: PhD

System-Level Design Methodologies for Platform-based Multiprocessor SoC Designs
Department of Informatics and Mathematical Modeling
Period: 01/06/2004 → 05/11/2008
Number of participants: 5
Phd Student:
Virk, Kashif Munir (Intern)
Main Supervisor:
Madsen, Jan (Intern)
Examiner:
Nannarelli, Alberto (Intern)
Jerraya, Ahmed Amine (Ekstern)
Nurmi, Jari Antero (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: Offentlig finansiering
Project: PhD

Adaptive Computing Architectures
Department of Informatics and Mathematical Modeling
Period: 01/03/2004 → 17/01/2008
Number of participants: 4
Phd Student:
Wu, Kehuai (Intern)
Main Supervisor:
Madsen, Jan (Intern)
Examiner:
Kuchcinski, Krzysztof (Ekstern)
Teich, Jürgen (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: DTU-lønnet stipendie
Project: PhD
Visualisering, opmåling & editering af 3D-medicinske data

Department of Informatics and Mathematical Modeling
Number of participants: 7
Phd Student:
Jakobsen, Bjarke (Ekstern)
Supervisor:
Madsen, Jan (Intern)
Pedersen, Steen (Intern)
Main Supervisor:
Christensen, Niels Jørgen (Intern)
Examiner:
Carstensen, Jens Michael (Intern)
Henriksen, Knud (Ekstern)
Sramek, Milos (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: Programbevilling
Project: PhD

Statisk program analyse af VHDL

Department of Informatics and Mathematical Modeling
Period: 01/04/2003 → 18/04/2007
Number of participants: 6
Phd Student:
Tolstrup, Terkel Kristian (Intern)
Supervisor:
Nielsen, Flemming (Intern)
Main Supervisor:
Nielsen, Hanne Riis (Intern)
Examiner:
Madsen, Jan (Intern)
Banerjee, Anindya (Ekstern)
Sabelfeld, Andrei (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: DTU-lønned stipendie
Project: PhD

Chip Area Interconnection Networks

Department of Informatics and Mathematical Modeling
Period: 01/09/2002 → 18/04/2006
Number of participants: 6
Phd Student:
Mahadevan, Shankar (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Sparsø, Jens (Intern)
Examiner:
Hansen, Michael Reichhardt (Intern)
Kuchcinski, Krzysztof (Ekstern)
Wolf, Wayne Hendrix (Ekstern)
Hig-Level Synthesis of Asynchronous

Department of Informatics and Mathematical Modeling
Period: 01/08/2001 → 06/06/2005
Number of participants: 6
Phd Student:
Nielsen, Sune Fallgaard (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Sparsø, Jens (Intern)
Examiner:
Nannarelli, Alberto (Intern)
Lavagno, Luciano (Ekstern)
Peeters, Ad (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: Anden EU-finansiering
Project: PhD

SoCLab, Proposal for a Danish System-on-Chip Initiative

The objective of the System-on-Chip (SoC) initiative, SoCLab, is to create a Danish virtual centre aimed at driving the future of electronic design. It represents a unique collaboration involving government, industry and academia to create a world-leading centre for the electronic and related design industries of the future. A Danish SoC centre should offer access to a comprehensive range of research and development facilities, covering fully-serviced laboratories, methods, tools, virtual components and employee training support. The initiative will develop Denmark into a world leading location for System-on-Chip design. The initiative consists of: - A Research & Education activity to increase the number of skilled SoC designers and to develop new competences to ease the SoC design process. - A SoCLab established as a design laboratory supporting the above mentioned research and education activity while at the same time providing an environment for interdisciplinary projects carried out jointly by industry and academia (DTU). - A virtual component (IP) exchange function concentrated on the business and legal issues involved with SoC designs. User groups will be formed in order to evaluate and prototype various IP blocks (DELTA). - A continuous training programme to address the shortage of skilled SoC designers in Danish industry. - An overall Programme Management Board will be established in order to monitor, steer and create synergy among the various activities. This should be established as a legal entity. The initiative will be followed by an international co-operation activity aimed at exchanging know-how and IPs with other leading SoC centres. Out of several collaboration partners four centres have been identified for a tighter co-operation.

Department of Information Technology
Period: 01/05/2000 → …
Number of participants: 1
Project Manager, organisational:
Madsen, Jan (Intern)

Low Power Digital Signal Processing

Department of Informatics and Mathematical Modeling
Period: 01/09/1998 → 21/01/2003
Number of participants: 4
Phd Student:
Paker, Ozgun (Intern)
Main Supervisor:
Sparsø, Jens (Intern)
Examiner:
Madsen, Jan (Intern)
Piguet, Christian (Ekstern)
Financing sources
Source: Internal funding (public)
Name of research programme: Ansat eksternt
Project: PhD

Teknikker til 3D visualisering, billedbehandling og simulering
Department of Informatics and Mathematical Modeling
Period: 01/07/1998 → 03/05/2002
Number of participants: 6
Phd Student:
Holten-Lund, Hans Erik (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Pedersen, Steen (Intern)
Examiner:
Christensen, Niels Jørgen (Intern)
Ernst, Rolf (Ekstern)
Slusallek, Philipp (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: Ansat eksternt
Project: PhD

Optimizing system level design of mobile phones
Department of Informatics and Mathematical Modeling
Period: 01/05/1998 → 01/10/2003
Number of participants: 2
Phd Student:
Bjørn-Jørgensen, Peter (Intern)
Main Supervisor:
Madsen, Jan (Intern)

Financing sources
Source: Internal funding (public)
Name of research programme: Samarbejdsaftalefinans
Project: PhD

Optimizing System Level Design of Mobile Phones
Today's mobile phones belong to the class of embedded computer systems which, as opposed to general purpose computer systems, are characterized by realizing well defined sets of system (lem tasks). This allows for system specialization, i.e. targeting the system implementation for the specialized application. As in other areas of engineering, the competitive marketplace and relatively short lifetime of mobile phones requires fast and inexpensive development subject to the constraints of cost, performance, power dissipation, dependability, etc.. Due to the size and complexity of these systems, as well as the many constraints, they are very difficult to analyze and design, even for experts. An optimal product is obtained by selecting the right system components (i.e. number of type of CPUs, ASICs, busses, interfaces, etc.) and selecting the right (lem mapping) of the system tasks onto these components, i.e. should a task be implemented as software on a CPU, which gives higher flexibility, or should it be implemented as dedicated hardware on an ASIC which reduces power dissipation and size of the product. This process is called (lem system level design). The main objective of the project is to develop, test and refine university developed tools for system level design in an industrial environment. The tools will be implemented as software programs.

Department of Information Technology
Nokia Mobile Phones A/S
Nokia Research Center
Period: 01/01/1998 → 30/04/2001
Number of participants: 3
Project participant:
Knudsen, Peter Voigt (Intern)
Bjørn-Jørgensen, Peter (Intern)
Project Manager, organisational:
Madsen, Jan (Intern)

Financing sources
Source: Unknown
Name of research programme: Ukendt
Amount: 1,431,600.00 Danish Kroner
Source: Unknown
Name of research programme: Ukendt
Amount: 1,938,000.00 Danish Kroner

PATMOS'98 workshop

Department of Information Technology
Period: 01/01/1998 → 30/10/1998
Number of participants: 3
Project participant:
Madsen, Jan (Intern)
Stassen, Flemming (Intern)
Project Manager, organisational:
Sparsø, Jens (Intern)

Financing sources
Source: Unknown
Name of research programme: Ukendt
Amount: 37,000.00 Danish Kroner
Source: Unknown
Name of research programme: Ukendt
Amount: 25,000.00 Danish Kroner
Source: Unknown
Name of research programme: Ukendt
Amount: 25,000.00 Danish Kroner

Project

Thomas B. Thrige Center for Microinstruments
The Thomas B. Thrige Centre for Microinstruments is an externally funded research project at DTU. The purpose of the centre is to perform research into methods and technologies for the design of electronic systems which integrate digital, analog and micromechanical components and embedded software in a single chip – a so-called “microinstrument” – which can accomplish signal collection, signal processing, data processing, communication and actuation. The centre was originally set up as a result of a donation of 5 million Danish crowns from the Thomas B. Thrige Foundation and further donations from the companies Oticon, Widex, GN Resound and Microtronic (now Sonion MEMS). Subsequently, a number of companies, institutions, university departments and some research projects have contributed to the co-funding of a series of Ph.D. projects. In addition to those companies already mentioned, the contributors involved have been BK Medical A/S, the Center for Fast Ultrasound Imaging, Ørsted*DTU, Mikroelektronikcentret, 3D Lab, Århus Kommunehospital, the IT University in Copenhagen, the Royal Veterinary and Agricultural University and the Research School in Microelectronics, which has co-funded 5 Ph.D. projects via a grant from the Danish Research Training Council (FUR). In total, the activities of the centre have involved funding and running 8 Ph.D. projects and a series of related activities, and the overall budget has been 10 million Danish crowns. The research has focused on two areas: (1) Digital integrated circuits and computer-based systems with focus on optimization of speed, energy consumption and effective use of resources, and (2) design and manufacturing techniques for micro-electro-mechanical systems (MEMS).

Department of Information Technology
Department of Micro- and Nanotechnology
Period: 01/04/1997 → 31/12/2003
Number of participants: 13
Project participant:
Pedersen, Steen (Intern)
Madsen, Jan (Intern)
Graduate School in Microelectronics
The Graduate School in Microelectronics was started in 1997 and its aim was to enhance (quantitatively and qualitatively) the Ph.d.-education in the area of Microelectronics. The Graduate School was funded by the Danish Research Training Council (in Danish: Forskeruddannelsesrådet) with 1 M kr. per year. The graduate school has co-funded summer schools, visiting professors and Ph.d.-scholarships. In total 8 Ph.d.-projects has been funded jointly by the Graduate School, private companies and research projects. The projects are hosted by MIC, Ørsted*DTU and IMM and the companies involved are: B-K Medical, Dicon, GN ReSound, NOKIA, Oticon, Sensor Technology Center and SonionMEMS.

Department of Information Technology
Department of Informatics and Mathematical Modeling
Department of Electrical Engineering
Department of Micro- and Nanotechnology
Period: 01/01/1997 → 31/12/2001
Number of participants: 15
Project participant:
Paker, Ozgun (Intern)
Holten-Lund, Hans Erik (Intern)
Larsen, Ken (Intern)
Pedersen, Steen (Intern)
Madsen, Jan (Intern)
Jensen, Jørgen Arendt (Intern)
Tomov, Borislaw Gueorgueliev (Intern)
Andreani, Pietro (Intern)
Wang, Xiaoyan (Intern)
Hansen, Ole (Intern)
Yalcinkaya, Arda Deniz (Intern)
Menon, Aric Kumaran (Intern)
Nielsson, Daniel (Ekstern)
Larsen, Kristian Pontoppidan (Intern)
Project Manager, organisational:
Sparsø, Jens (Intern)

Financing sources
Source: Unknown
Name of research programme: Ukendt
Amount: 5,000,000.00 Danish Kroner
Source: Unknown
Name of research programme: Ukendt
Amount: 2,500,000.00 Danish Kroner
Source: Unknown
Name of research programme: Ukendt
Amount: 2,000,000.00 Danish Kroner
3D-Med
The project is carried out together with Assoc. Prof. Jan Madsen at IT, DTU, in collaboration with 3D-Lab, which is situated at the Panum Institute, at the University of Copenhagen. In 1998 the project has been enlarged to include a collaboration with Århus University Hospital, where Prof. Niels Egund has joined the project. In 1999 the project included a collaboration with Prof. Børresen, the Rigshospitalet and Carl Bro A/S, which will produce a report describing the technical and commercial possibilities to continue the project. This activity is supported by Erhversfremmestyrelsen. The project started as a case study in the Codesign project. The main topic in this project, is to design and implement a cost efficient workstation, based on an ordinary PC running MicrOsot Windows, which can be used for 3-dimensional modelling and manipulation of medical objects. The main idea is to bring this functionality from the specialists laboratory to the desk of the physicians in the clinic. In 1998 Hans Holten-Lund has started a Ph.D. study and Mogens Hvidtfeldt was employed as a research assistant within the project. Both activities has been supported financially by the Thomas B. Thriges Center for Microinstruments.

Department of Information Technology
Department of Informatics and Mathematical Modeling
Panum Instituttet
Aarhus University
Carl Bro A/S
University of Copenhagen
Period: 01/01/1996 → ...
Number of participants: 3
Project participant:
Holten-Lund, Hans Erik (Intern)
Madsen, Jan (Intern)
Project Manager, organisational:
Pedersen, Steen (Intern)

Financing sources
Source: Unknown
Name of research programme: Ukendt
Amount: 1,000,000.00 Danish Kroner
Project

Teknikker til Co-syntese
Department of Informatics and Mathematical Modeling
Period: 01/01/1996 → ...
Number of participants: 4
Phd Student:
Knudsen, Peter Voigt (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Sharp, Robin (Intern)
Examiner:
Ernst, Rolf (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: Forskningsrådsstip.-SU, Eksp
Project: PhD

Integriert hardware/software kode-generering i Co-design
Department of Information Technology
LYCOS: Embedded Systems Synthesis
LYCOS is a research group at the Computer Systems Section (DTU) working with CAD supported design methodologies for developing embedded computer systems. LYCOS is also the name of the framework in which all tools developed by the group are integrated. One of the most important problems in hardware/software codesign is the selection of the components that should comprise the target architecture and the mapping of the specification onto those components. Large heterogeneous systems are often composed of several components, such as microprocessors, dedicated hardware, external devices, and memories, interconnected by general or local buses, using a variety of communication protocols. Selecting the best combination of components is a prerequisite for ending up with the best result of the subsequent phases of the design process which include functional partitioning and hardware/software/communication synthesis. The aim of the LYCOS group is to develop CAD tools which support the designer in selecting a suitable target architecture for a given application by allowing the designer to explore the design space. In particular, we focus on: 1) models, establishing a unified model for hardware and software which allows specification and analysis of embedded computer systems at various levels of abstraction. 2) mappings, which allow for quantitative analysis of important properties, such as performance, cost, power dissipation, and resource utilization, all of which are important for the designer to tradeoff different design choices. 3) experiments, to try out the tools and gain feedback by applying them on realistic design examples.
Asynchronous Circuit Design
Asynchronous circuits operate without a global clock signal - the flow of data is controlled by local handshaking between modules and registers. This gives asynchronous circuits some unique characteristics that can be exploited to advantages (higher speed, lower power consumption, modularity and robustness). The research addresses methods and techniques for designing efficient circuits, and in particular circuits with low power consumption. The experimental part of this work is based on industrial applications and involves design and fabrication of various prototype IC's. From 2001 the activities have focused on high-level synthesis of asynchronous circuits and on network-on-chip. The activity represents a long term effort and it is funded through a number of sources including the ACiD working group (IST-1999-29119), the Thomas B. Thrige Foundation and a donation from Nokia.